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T-EMU: GRLIB IrqMp Device Model Manual

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Record of Changes

Author	Description	Rev	Date
Mattias Holm	Initial Version	1.0	2015-07-31

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1. Introduction

The IrqMP is part of the GRLIB device library from Gaisler. It is a multiprocessor capable interrupt controller.

The controller supports among things the routing of interrupts to different processor cores, and also broadcasted interrupts.

2. Configuration

config.nCpu	Number of processors supported.
config.enExtIrq	Enable extended IRQs.
pnp.config	Plug and play configuration word for APB plug-and-play.
cpu	Up to 16 CPUs supported. IfaceRef property should be connected to the different CPUs.

3. Interfaces

IrqClientInterface0 through 15	IRQ acknowledge support for up to 16 CPUs
MemAccessIface	Memory access interface.
ApbIface	The IrqMp model implements the APB plug and play emulation. The APB controller should be connected to this interface.
DeviceIface	Handles resets. Connect to from CPU or machine model to automatically reset the IrqMp device model when the system is reset.

4. Limitations

The following deviations from real hardware are known to exist with this model:

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- Broadcasted interrupts are broadcasted at the current time to all CPUs, if it was triggered by a non-synchronised event, the interrupt is raised at different times on the different cores. Depending on the IRQ frequency and the configured quanta length, this may result in problems.