

T-EMU: GRSPW2 Model Manual



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Record of Changes

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1. Introduction

The GRSPW2 is part of the GRLIB IP library. It is available in libTEMUGrSpw2.so.

2. Configuration

To work correctly, the device should be connected to an interrupt controller, the memory and another SpaceWire device.

There are several configuration parameters in the GrSpw2 device, summarized in the following table:

| Name | Description |
|------------------------------|---|
| config.infiniteSpeed | With this set, messages are sent immediately instead of being scheduled for the future based on the message length. This is the default option. |
| config.transmitter.frequency | Specify the SpaceWire transmitter frequency in Hz. Affects transfer speed when infinite speed is disabled. |
| config.transmitter.dataRate | SpaceWire port datarate: 1=single, 2=double, etc. Affects transfer speed when infinite speed is disabled. |
| config.dma.rxdescnum | Specifies the amount of rx description (0=128, 1=256, 2=512, 3=1024). This affect the regs.dmaRxDescTableAddr |
| config.dma.txdescnum | Specifies the amount of tx descriptors (0=64, 1=128, 2=256, 3=512). This affect the regs.dmaTxDescTableAddr |



| Name | Description |
|---------------------|--|
| config.interrupt | Influences the interrupt that is raised with the IRQ controller (setting this property also updates the APB PnP info). |
| config.realCrcCheck | Set to use real crc check instead of packet crc flags. Real crc costs in terms of performance. |

3. Attributes

3.1. Properties

| Name | Type | Description |
|------------------------------|------------------|---|
| config.dma.rxdescnum | uint8_t | Number of rx descriptors |
| config.dma.txdescnum | uint8_t | Number of tx descriptors |
| config.infiniteSpeed | uint8_t | Set to use infinite speed for transfers. |
| config.interrupt | uint8_t | The interrupt index |
| config.realCrcCheck | uint8_t | Set to use real crc check instead of packet crc flags |
| config.transmitter.dataRate | uint8_t | SpaceWire port datarate: 1=single, 2=double,... |
| config.transmitter.frequency | uint32_t | SpaceWire transmitter frequency in Hz |
| internal.linkState | int32_t | Link state |
| internal.txCurrChan | uint8_t | Channel scheduled for transmission |
| internal.txDAddr | uint32_t | Data address for the scheduled dma engine transfer |
| internal.txDLength | uint32_t | Data length for the scheduled dma engine transfer |
| internal.txFlags | uint32_t | Flags for the scheduled dma engine transfer |
| internal.txHAddr | uint32_t | Header address for the scheduled dma engine transfer |
| internal.txType | uint8_t | Scheduled transmission type (dma engine/rmap) |
| internal.uplinkNsPerByte | uint32_t | Transmitter speed |
| irqCtrl | iref / <unknown> | Irq controller |
| memory | iref / <unknown> | Memory used for DMA accesses |
| object.timeSource | object | Time source object (a cpu or machine object) |



| Name | Type | Description |
|-------------------------|------------------------|---|
| pnnp.bar | uint32_t | Pnp BAR |
| pnnp.config | uint32_t | Pnp configuration |
| regs.clockDiv | uint32_t | Clock Divisor register |
| regs.control | uint32_t | Control register |
| regs.destKey | uint32_t | Destination Key register |
| regs.dmaAddr | [4 x uint32_t] | Dma address registers |
| regs.dmaControl | [4 x uint32_t] | Dma control registers |
| regs.dmaRxDescTableAddr | [4 x uint32_t] | Dma receive descriptor table address registers |
| regs.dmaRxMaxLen | [4 x uint32_t] | Dma rx maximum length registers |
| regs.dmaTxDescTableAddr | [4 x uint32_t] | Dma transmit descriptor table address registers |
| regs.nodeAddress | uint32_t | Node address register |
| regs.statusIrqSrc | uint32_t | Status / Interrupt-source register |
| regs.time | uint32_t | Time register |
| spwUplink | [2 x iref / <unknown>] | SpaceWire devices connected to the port |

3.2. Interfaces

| Name | Type | Description |
|----------------|----------------|----------------------------|
| ApbIface | ApbIface | Apb interface |
| DeviceIface | DeviceIface | Device interface |
| MemAccessIface | MemAccessIface | Memory Access Interface |
| ResetIface | ResetIface | |
| SpwPortIface | SpwPortIface | SpaceWire ports interfaces |

3.3. Ports

| Prop | Iface | Description |
|------|-------|-------------|
| - | - | - |

4. Limitations

The following deviations from real hardware are known to exist with this model:

- Although the device already provides two ports, dual port is not yet implemented. Let us know if you need this feature implemented.



- The link interface currently effectively uses only ErrorReset, Ready, Connecting and Run states. Therefore, those are the only values that will be visible on the status register.
- RMAPEN and PNPEN signals not available

5. Examples

This example shows how to create two Grspw2 devices and connect them.

```
import BusModels
import TEMUGrspw2
object-create class=Grspw2 name=grspw0
object-create class=Grspw2 name=grspw1
spw-connect port1=grspw0:SpwPortIface[0] port2=grspw1:SpwPortIface[0]
```