

TEMU

Machine Class Manual

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Table 1. Record of Changes

| Rev | Date | Author | Note |
|-----|------------|--------|------------------|
| 1.1 | 2016-05-12 | MH | Auto gen tables. |
| 1.0 | 2015-07-01 | MH | Initial version. |

1. Introduction

The machine class is used to assemble and group related processors in machines. The machine class is intended to be used for SMP and multi-core systems. It provides the following capabilities:

1. A multi-CPU scheduler that executes all the CPUs in the machine in sequence (for a fixed time quanta).
2. A synchronised event queue. CPUs can post events in the next time quanta to be executed after all the processors have reached a specific time point.
3. A scheduling interface enabling the machine to be run for a time specified in seconds, not cycles.

Note that the machine class supports the scheduling of different CPUs with different clock frequencies.

Synchronised events are posted on a CPUs event queue by adding the flag `TEMU_EVENT_SYNC` to the posting function, this will bypass the CPU event queue and put it in the machine object's queue.

2. Attributes

2.1. Properties

| Name | Type | Description |
|--------------------------------|------------------------|--|
| <code>cpus</code> | <code>irefarray</code> | Processors in the machine |
| <code>currentCPU</code> | <code>iref</code> | Current CPU |
| <code>currentCPUIdx</code> | <code>int32_t</code> | Current CPU Index |
| <code>devices</code> | <code>irefarray</code> | Devices to reset when machine is reset |
| <code>object.timeSource</code> | <code>object</code> | Time source object (a cpu or machine object) |
| <code>quanta</code> | <code>uint64_t</code> | Quanta length in nanoseconds |
| <code>quantaEnd</code> | <code>uint64_t</code> | End point of current quanta in nanoseconds |
| <code>quantaStart</code> | <code>uint64_t</code> | Quanta start in nanoseconds |
| <code>syncMask</code> | <code>uint64_t</code> | Synchronised CPU mask |

2.2. Interfaces

| Name | Type | Description |
|--------------|--------------|-------------|
| EventIface | EventIface | |
| LegacyIface | LegacyIface | |
| MachineIface | MachineIface | |
| ObjectIface | ObjectIface | |

2.3. Ports

| Prop | Iface | Description |
|------|-------|-------------|
| - | - | - |

3. Limitations

- The machine class cannot have more than 64 CPU cores connected.