TERMA

ALLIES IN INNOVATION

Emulator Performance Study

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Emulation Performance

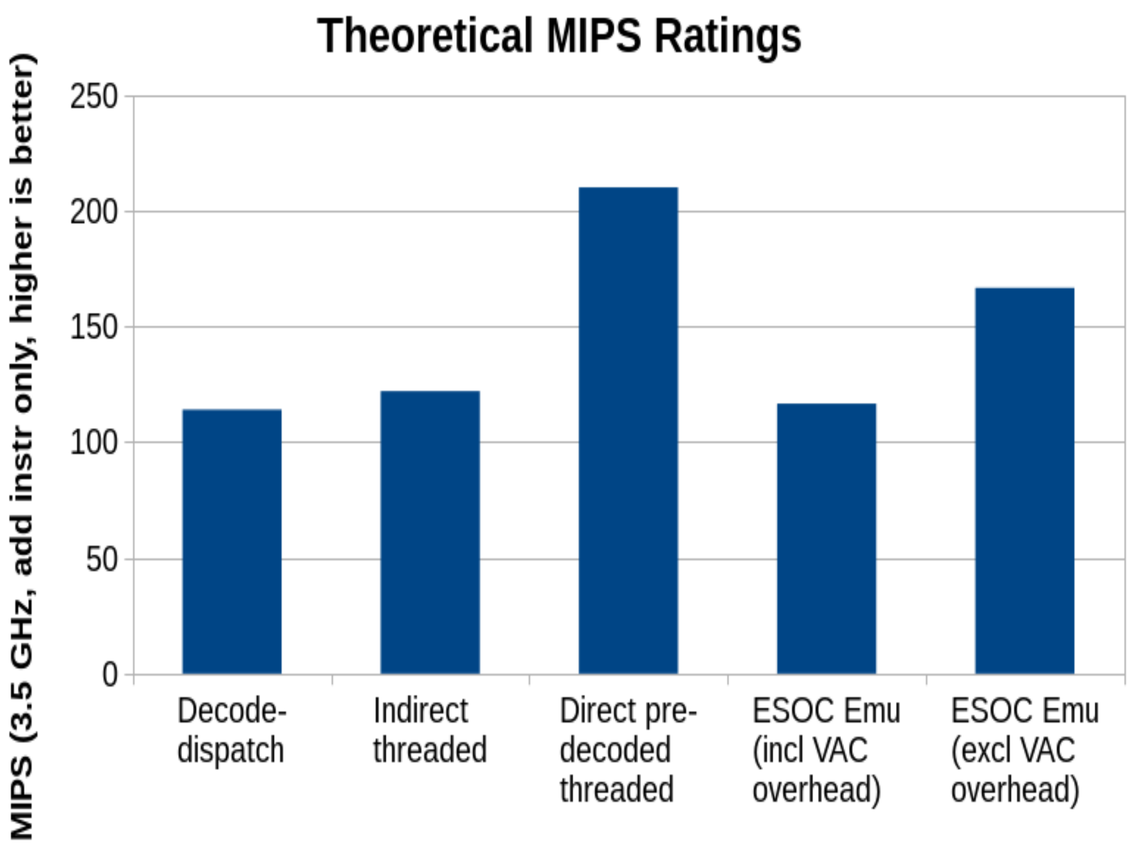
Goals
- Assess performance of existing emulators
- Determine performance bottlenecks
- Gather data for the development of T-EMU 2.0, the Terma Emulator.

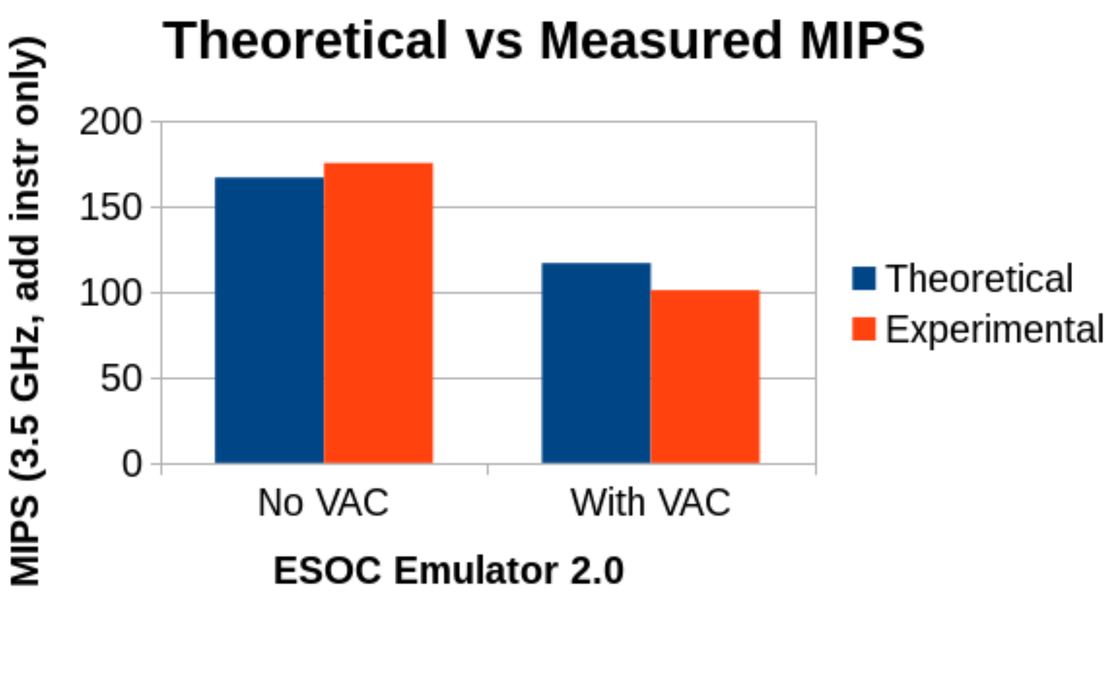
Instruction Count Matters
Emulator performance is optimised by counting and reducing host instructions per target instruction

Measurements
- MIPS (emulated instructions per second)
- Speedup (times real time)
- Slowdown (factor of real time)

Theoretical Model

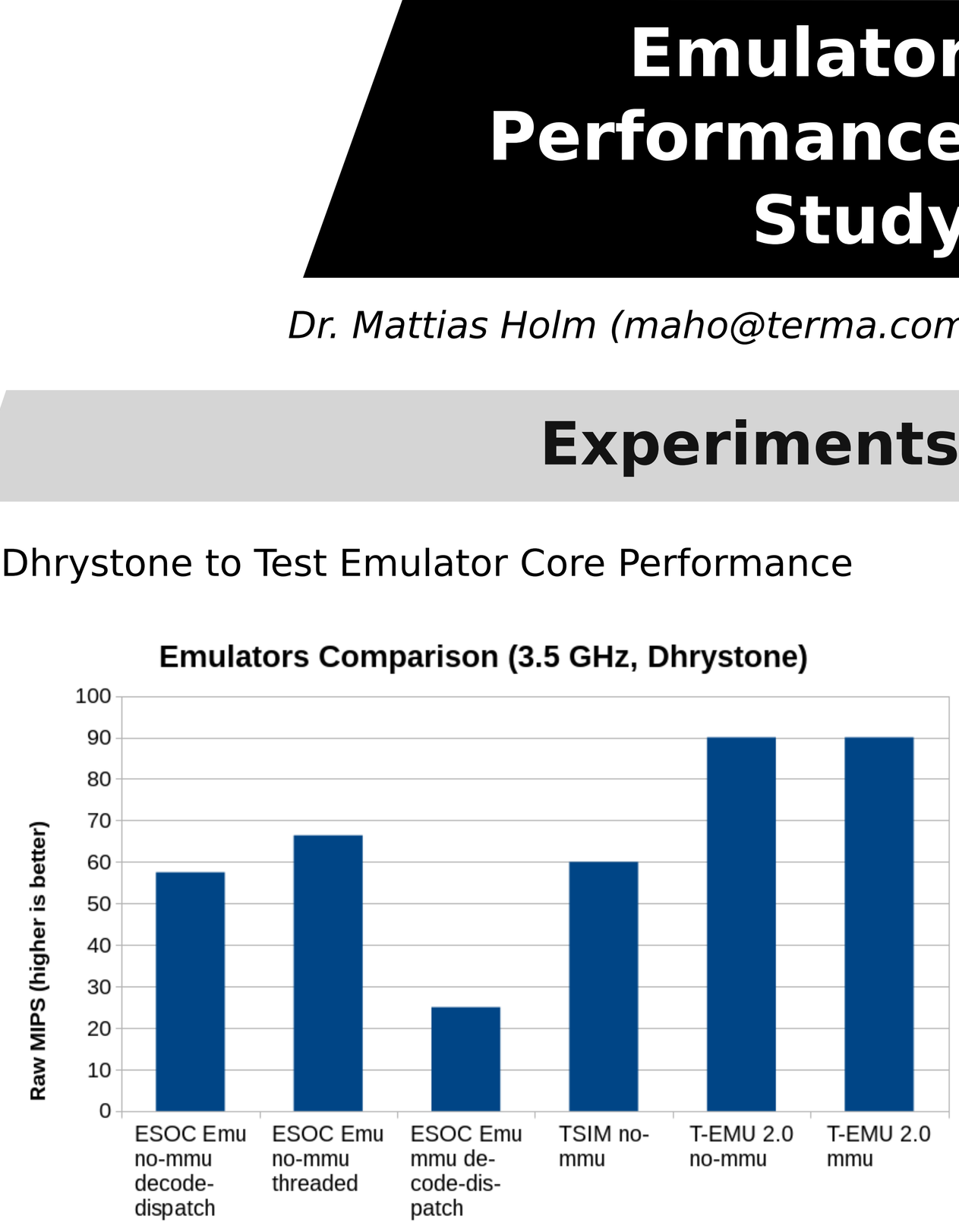
Estimation of emulator performance by counting host instructions in an ideal emulator.
- Different emulation methods.
- Application of model on ESOC Emu



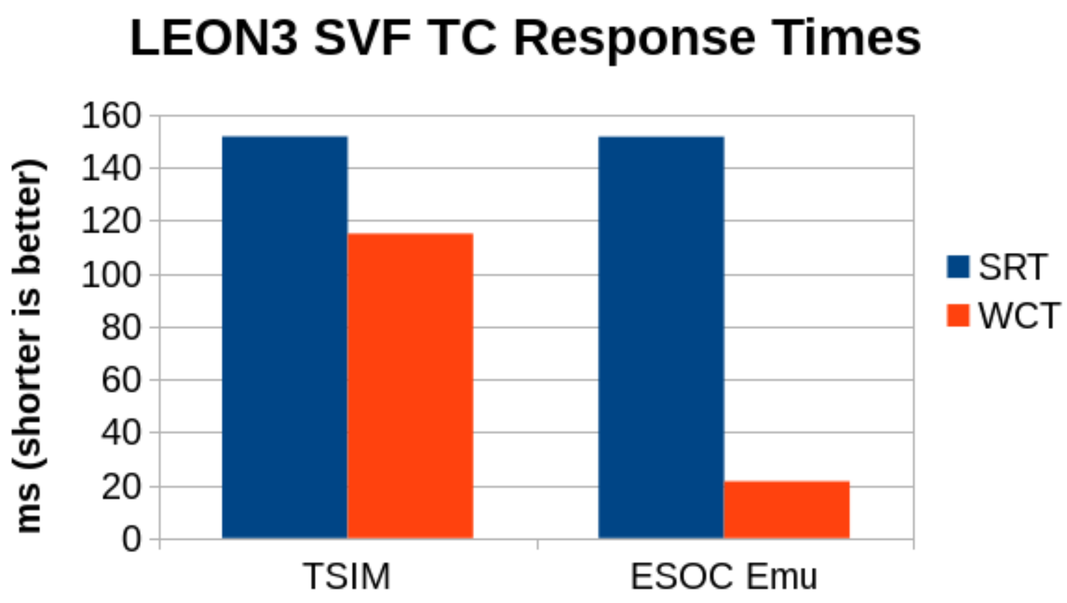


Experiments

Dhrystone to Test Emulator Core Performance



Real-world experiments in an SVF.
Memory as MMIO model responsible for difference.



Conclusions and Results

- Theoretical model represents reality
- Running memory models as external device models is not recommended.
- MMU models can have severe impact, but mechanisms to address MMU performance exist.
- Model used to focus work on T-EMU 2.0
- T-EMU 2.0 design provides high performance

T-EMU 2.0