TEMU

GRLIB IrqMp Device Model Manual

Mattias Holm

Version 1.1, 2016-05-12
Table of Contents

1. Introduction ........................................................................................................... 1
2. Configuration .......................................................................................................... 1
3. Attributes .............................................................................................................. 1
   3.1. Properties ......................................................................................................... 1
   3.2. Interfaces .......................................................................................................... 2
   3.3. Ports .................................................................................................................. 2
4. Limitations ............................................................................................................. 2
1. Introduction

The IrqMP is part of the GRLIB device library from Gaisler. It is a multiprocessor capable interrupt controller.

The controller supports among things the routing of interrupts to different processor cores, and also broadcasted interrupts.

2. Configuration

config.nCpu
   Number of processors supported.

config.enExtIrq
   Enable extended IRQs.

pnp.config
   Plug and play configuration word for APB plug-and-play.

cpu
   Up to 16 CPUs supported. IfaceRef property should be connected to the different CPUs.

3. Attributes

3.1. Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>broadcast</td>
<td>uint32_t</td>
<td></td>
</tr>
<tr>
<td>config.enExtIrq</td>
<td>uint8_t</td>
<td></td>
</tr>
<tr>
<td>config.logInterrupts</td>
<td>uint8_t</td>
<td></td>
</tr>
<tr>
<td>config.nCpu</td>
<td>uint8_t</td>
<td></td>
</tr>
<tr>
<td>config.traceReads</td>
<td>uint8_t</td>
<td></td>
</tr>
<tr>
<td>config.traceWrites</td>
<td>uint8_t</td>
<td></td>
</tr>
<tr>
<td>cpu</td>
<td>[16 x iref / &lt;unknown&gt;]</td>
<td></td>
</tr>
<tr>
<td>extIntAck</td>
<td>[16 x uint32_t]</td>
<td></td>
</tr>
</tbody>
</table>
### Name | Type | Description
--- | --- | ---
force | [16 x uint32_t] | 
irqClear | uint32_t | 
irqCtrl | [16 x iref / <unknown>] | 
irqForce0 | uint32_t | 
irqLevel | uint32_t | 
irqPending | uint32_t | 
mask | [16 x uint32_t] | 
mpStatus | uint32_t | 
object.timeSource | object | Time source object (a cpu or machine object)
pnp.bar | uint32_t | 
pnp.config | uint32_t | 

### Interfaces

### Name | Type | Description
--- | --- | ---
ApbIface | ApbIface | 
DeviceIface | DeviceIface | 
IrqClientIface | IrqClientIface | uptree interrupt handlers (e.g. CPUs)
IrqIface | IrqCtrlIface | 
MemAccessIface | MemAccessIface | 
ResetIface | ResetIface | 

### Ports

### Prop | Iface | Description
--- | --- | ---
irqCtrl | IrqClientIface | irq port

### Limitations

The following deviations from real hardware are known to exist with this model:

- Broadcasted interrupts are broadcasted at the current time to all CPUs, if it was triggered by a non-synchronised event, the interrupt is raised at different times on the different cores. Depending on the IRQ frequency and the configured quanta length, this may result in problems.