TEMU
Model Reference

Version 5.1, 2026-11-20

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Chapter 1. Models

This is the reference manual for the TEMU models.

Each model description is normally structured using the following sections:

- Introduction
- Loading the Plugin
- Configuration
- Limitations

In addition, models have reference content such as properties, interfaces and registers listed.

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Chapter 2. Memory

2.1. Memory Space

The Memory Space manages the physical memory map of the processors. In addition, it manages code caches for both the interpreter and the translator.

2.1.1. @MemorySpace Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @MemorySpace
new	Create new instance of MemorySpace

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create
processor-count	int	no	Number of processors supported by memory space (default = 4)

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2.1.2. MemorySpace Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
absentHandlers	temu_IfaceRef/ <unknown>	Absent handlers invoked on accesses to unmapped memory.
config.attrInitiators	uint32_t	Mask of TEMU_ATTR_CHECK_* - which initiator types have their accesses checked against the upset, faulty and user attributes. Defaults to TEMU_ATTR_CHECK_CPU (1) alone; add TEMU_ATTR_CHECK_DEVICE (2) for a machine whose ECC controllers should also see its bus masters. The break and watchpoint attributes are not affected, they are always handled for processors only.
config.noRemapping	uint8_t	
config.processorCount	uint32_t	Max number of processors.
config.processorHasSync	uint8_t	
config.virtualization	uint8_t	
cpus	temu_IfaceRefArray	

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Name	Type	Description
faultyHandlers	temu_IfaceRef/ <unknown>	Faulty handlers invoked on faulty (uncorrectable error) memory access.
invalidaccess	temu_IfaceRef/ <unknown>	Invalid memory access interface.
postTransaction	temu_IfaceRef/ <unknown>	Post transaction interface invoked after transaction has effect.
preTransaction	temu_IfaceRef/ <unknown>	Pre transaction interface invoked before transaction has effect.
target	temu_IfaceRef/ <unknown>	Target execution interface.
upsetHandlers	temu_IfaceRef/ <unknown>	Upset handlers invoked on upset (correctable error) memory access.
user1Handlers	temu_IfaceRef/ <unknown>	User handlers invoked on User1 flagged memory access.
user2Handlers	temu_IfaceRef/ <unknown>	User handlers invoked on User2 flagged memory access.
user3Handlers	temu_IfaceRef/ <unknown>	User handlers invoked on User3 flagged memory access.

Interfaces

Name	Type	Description
DebuggerAttachIface	temu::DebuggerAttachIface	
MemAccessIface	MemAccessIface	
MemAccessPropertyIface	temu::MemAccessIfaceProperty	
MemMapEntryIface	MemMapEntryIface	
MemorySpaceIface	temu::MemorySpaceIface	
ObjectIface	ObjectIface	
PDCIface	PDCIface	
ResetIface	ResetIface	

Commands

Name	Description
clear-attr	Clear attribute

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Name	Description
delete	Dispose instance of MemorySpace
disable-io-perf	Enable performance collection for I/Os.
disable-remapping-support	Disable support for remapped pages
disable-spinlocks	Disable spinlocks for I/O locks instead of normal mutexes.
dump	Dump memory
enable-experimental-io-perf	Enable performance collection for I/Os.
enable-experimental-spinlocks	Enable spinlocks for I/O locks instead of normal mutexes.
enable-io-perf	Enable performance collection for I/Os.
enable-remapping-support	Enable support for remapped pages (default)
enable-spinlocks	Enable spinlocks for I/O locks instead of normal mutexes.
flush-code	Drop all decoded and translated code.
inject-read	Inject read transaction
inject-write	Inject transaction
io-break	Break on I/O model device accesses
map	Map in device
pstat	Print memory space statistics
set-attr	Set attribute
trace-accesses	Trace I/O model device accesses
unmap	Unmap devices
validate-cfm-crc	Validate Code Fragment CRCs.
write	Write memory

Command clear-attr Arguments

Name	Type	Required	Description
addr	int	yes	Address to write device.
attr	string	yes	Attribute to set
length	int	yes	Length of item to write in bytes (default = 4).

Command dump Arguments

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Name	Type	Required	Description
addr	int	yes	Address to map device.
length	int	no	Length of address mapping in bytes (default = 16).
swap	int	no	Swap bytes value is log size of swap unit (0-3), default = 0

Command inject-read Arguments

Name	Type	Required	Description
pa	int	no	Physical address of transaction.
size	int	no	Transaction unit size (default = 2 (4 bytes)).
va	int	yes	Virtual address of transaction.

Command inject-write Arguments

Name	Type	Required	Description
pa	int	no	Physical address of transaction.
size	int	no	Transaction unit size (default = 2 (4 bytes)).
va	int	yes	Virtual address of transaction.
value	int	no	Value to write (default = 0)

Command io-break Arguments

Name	Type	Required	Description
device	object	yes	Device to break on accesses to.

Command map Arguments

Name	Type	Required	Description
addr	int	yes	Address to map device.

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Name	Type	Required	Description
iface	interface	yes	Memory access interface.
length	int	yes	Length of address mapping in bytes.
reset	int	no	Add to reset vectors.

Command set-attr Arguments

Name	Type	Required	Description
addr	int	yes	Address to write device.
attr	string	yes	Attribute to set
length	int	yes	Length of item to write in bytes (default = 4).

Command trace-accesses Arguments

Name	Type	Required	Description
device	object	yes	Device to trace accesses to.

Command unmap Arguments

Name	Type	Required	Description
addr	int	yes	Address to unmap.
length	int	yes	Length of address mapping to unmap in bytes.

Command write Arguments

Name	Type	Required	Description
addr	int	yes	Address to write device.
length	int	no	Length of item to write in bytes (default = 4).
swap	int	no	Swap bytes value is log size of swap unit (0-3), default = 0
value	int	yes	Value to write

2.2. ROM

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The TEMU ROM model is a basic ROM model. The model does not support writes.

2.2.1. @Rom Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @Rom
new	Create new instance of Rom

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create
size	int	no	size in bytes

2.2.2. Rom Reference

Properties

Name	Type	Description
Class	*void	Class object

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Name	Type	Description
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
size	uint64_t	ROM size
ws	uint16_t	

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	
LittleEndianMemAccessIface	MemAccessIface	
MemAccessIface	MemAccessIface	
MemAccessPropertyIface	temu::MemAccessIfaceProperty	
MemDeltaIface	temu::MemoryDeltaIface	
ObjectIface	ObjectIface	

Commands

Name	Description
delete	Dispose instance of Rom

2.3. RAM

The TEMU RAM model is a basic RAM model.

2.3.1. @Ram Reference

Properties

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @Ram
new	Create new instance of Ram

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create
size	int	no	size in bytes

2.3.2. Ram Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)

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Name	Type	Description
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
size	uint64_t	Ram Size
ws	uint16_t	

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	
LittleEndianMemAccessIface	MemAccessIface	
MemAccessIface	MemAccessIface	
MemAccessPropertyIface	temu::MemAccessIfaceProperty	
MemDeltaIface	temu::MemoryDeltaIface	
ObjectIface	ObjectIface	
ResetIface	ResetIface	

Commands

Name	Description
delete	Dispose instance of Ram

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Chapter 3. AMBA

TEMU provides support for AMBA plug-and-play as used in the Gaisler GRLIB. The AMBA bus support and interfaces are defined in `temu-c/Bus/Amba.h`. In addition to the interfaces implemented by device models, the `AhbCtrl` and `ApbCtrl` classes are provided.

3.1. Interfaces

The interfaces are defined in the `temu-c/Bus/Amba.h` header. This header provides support constants and helper functions, used to work with the PnP info structs.

Listing 1. AMBA PnP API

```
typedef struct {
  uint32_t IdentReg;
  uint32_t UserDef[3];
  uint32_t Bar[4];
} temu_AhbPnpInfo;

typedef struct temu_AhbIface {
  temu_AhbPnpInfo* (*getAhbPnp)(void *Obj);
} temu_AhbIface;

typedef struct {
  uint32_t ConfigWord;
  uint32_t Bar;
} temu_ApbPnpInfo;

typedef struct temu_ApbIface {
  temu_ApbPnpInfo* (*getApbPnp)(void *Obj);
} temu_ApbIface;
```

3.2. Classes

There are two important classes provided, the AhbCtrl and ApbCtrl classes. These are available in `libTEMUAhbCtrl.so` and `libTEMUApbCtrl.so`.

When configuring a non-standard LEON3 / LEON4 based processor, the AHB and APB controllers must be instantiated and connected to devices implementing the plug and play interfaces. For the `AhbCtrl` class, connections is done using the `masters` and `slaves` array properties. For the `ApbCtrl` class, only the `slaves` property exist.

3.2.1. @AhbCtrl Reference

Properties

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Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @AhbCtrl
new	Create new instance of AhbCtrl

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

3.2.2. AhbCtrl Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags

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Name	Type	Description
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
config.SoCID	uint32_t	SoCID to return at offset 0xff0 if enabled.
config.enableSoCID	uint8_t	Enable SoCID at offset 0xff0.
config.littleEndian	uint8_t	Endianess of memory interface.
masters	[temu_IfaceRef; 64]/ <unknown>	AHB master devices.
slaves	[temu_IfaceRef; 64]/ <unknown>	AHB slave devices.

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
ObjectIface	ObjectIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Commands

Name	Description
delete	Dispose instance of AhbCtrl

3.2.3. @ApbCtrl Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component

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Name	Type	Description
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @ApbCtrl
new	Create new instance of ApbCtrl

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

3.2.4. ApbCtrl Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.

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Name	Type	Description
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
config.littleEndian	uint8_t	Endianess of memory interface.
pnp.bar	[uint32_t; 4]	
pnp.identReg	uint32_t	
pnp.userDef	[uint32_t; 3]	
slaves	[temu_IfaceRef; 512]/ <unknown>	APB slaves.

Interfaces

Name	Type	Description
AhbIface	AhbIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
ObjectIface	ObjectIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Commands

Name	Description
delete	Dispose instance of ApbCtrl

3.2.5. @AHB2AHB Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags

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Name	Type	Description
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @AHB2AHB
new	Create new instance of AHB2AHB

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

3.2.6. AHB2AHB Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

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Name	Type	Description
masterPnp.bar	[uint32_t; 4]	AMBA plug and play base address register
masterPnp.ident	uint32_t	AMBA plug and play config word
masterPnp.user	[uint32_t; 3]	AMBA plug and play user words
slavePnp.bar	[uint32_t; 4]	AMBA plug and play base address register
slavePnp.ident	uint32_t	AMBA plug and play config word
slavePnp.user	[uint32_t; 3]	AMBA plug and play user words

Interfaces

Name	Type	Description
MasterAhbIface	AhbIface	
ResetIface	ResetIface	
SlaveAhbIface	AhbIface	

Commands

Name	Description
delete	Dispose instance of AHB2AHB

3.2.7. @AhbStat Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.

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Name	Type	Description
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @AhbStat
new	Create new instance of AhbStat

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

3.2.8. AhbStat Reference

Properties

Name	Type	Description
AHBFAR2ColdResetValue	uint32_t	AHB Failing address register
AHBFAR2ForcedBits	uint32_t	AHB Failing address register
AHBFAR2ForcedFlippedBits	uint32_t	AHB Failing address register
AHBFAR2ReadMask	uint32_t	AHB Failing address register
AHBFAR2ResetMask	uint32_t	AHB Failing address register
AHBFAR2ResetValue	uint32_t	AHB Failing address register
AHBFAR2WriteMask	uint32_t	AHB Failing address register
AHBFARColdResetValue	uint32_t	AHB Failing address register
AHBFARForcedBits	uint32_t	AHB Failing address register
AHBFARForcedFlippedBits	uint32_t	AHB Failing address register
AHBFARReadMask	uint32_t	AHB Failing address register
AHBFARResetMask	uint32_t	AHB Failing address register
AHBFARResetValue	uint32_t	AHB Failing address register
AHBFARWriteMask	uint32_t	AHB Failing address register
AHBS2ColdResetValue	uint32_t	AHB Status register
AHBS2ForcedBits	uint32_t	AHB Status register

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Name	Type	Description
AHBS2ForcedFlippedBits	uint32_t	AHB Status register
AHBS2ReadMask	uint32_t	AHB Status register
AHBS2ResetMask	uint32_t	AHB Status register
AHBS2ResetValue	uint32_t	AHB Status register
AHBS2WriteMask	uint32_t	AHB Status register
AHBSColdResetValue	uint32_t	AHB Status register
AHBSForcedBits	uint32_t	AHB Status register
AHBSForcedFlippedBits	uint32_t	AHB Status register
AHBSReadMask	uint32_t	AHB Status register
AHBSResetMask	uint32_t	AHB Status register
AHBSResetValue	uint32_t	AHB Status register
AHBSWriteMask	uint32_t	AHB Status register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
config.interrupt	uint8_t	
config.littleEndian	uint8_t	Endianess of memory interface.
failingAddrReg	uint32_t	AHB Failing address register
failingAddrReg2	uint32_t	AHB Failing address register
irqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller.
pnp.bar	uint32_t	
pnp.config	uint32_t	
statusReg	uint32_t	AHB Status register

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Name	Type	Description
statusReg2	uint32_t	AHB Status register

Interfaces

Name	Type	Description
AbsentMemoryIface	MemAccessIface	
ApbIface	ApbIface	
CorrectableErrorIface	MemAccessIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	
UncorrectableErrorIface	MemAccessIface	

Commands

Name	Description
delete	Dispose instance of AhbStat

3.3. Examples

The first example shows how to create and connect the AHB and APB bus controllers.

Listing 2. Connecting AHB and APB Controllers

```
import AhbCtrl
import ApbCtrl

# Create two bus objects
AhbCtrl.new name=ahbctrl0
ApbCtrl.new name=apbctrl0

# Map to the normal addresses
memory-map memspace=mem0 addr=0x800ff000 length=0x1000 object=apbctrl0
memory-map memspace=mem0 addr=0xfffff000 length=0x1000 object=ahbctrl0

# Connect various APB devices to the APB controller
connect a=apbctrl0.slaves b=ftmctrl0:ApbIface
connect a=apbctrl0.slaves b=apbuart0:ApbIface
connect a=apbctrl0.slaves b=irqMp0:ApbIface
connect a=apbctrl0.slaves b=gpTimer0:ApbIface
```

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```
connect a=apbctrl0.slaves b=ahbstat0:ApbIface

# Connect various AHB devices to the AHB controller
connect a=ahbctrl0.masters b=cpu0:AhbIface
connect a=ahbctrl0.slaves b=ftmctrl0:AhbIface
connect a=ahbctrl0.slaves b=apbctrl0:AhbIface
```

The next example shows how to implement a simple APB device.

Listing 3. Simple Device with APB PNP Support

```
#include "temu-c/Bus/Amba.h"

// This is the model type, we need to add the Pnp info.
typedef struct MyDevice {
  temu_ApbPnpInfo Pnp;
  // ...
} MyDevice;


// Implement the APB PNP interface
temu_ApbPnpInfo*
getApbPnp(void *Obj)
{
   MyDevice *Dev = (MyDevice*)Obj;

   return &Dev->Pnp;
}

temu_ApbIface ApbIface = {
  .getApbPnp = getApbPnp
};


// Define functions to allocate and destroy the object
void*
create(int Argc, const temu_CreateArg *Argv)
{
  MyDevice *Dev = malloc(sizeof(MyDevice));
  memset(Dev, 0, sizeof(MyDevice));

  // PNP init
  temu_apbSetVendorId(&MyDevice->Pnp, 0x99);
  temu_apbSetDeviceId(&MyDevice->Pnp, 0x001);
  temu_apbSetVersion(&MyDevice->Pnp, 1);

  temu_apbSetAddr(&MyDevice->Pnp, 0);
  temu_apbSetCP(&MyDevice->Pnp, 0);
  temu_apbSetMask(&MyDevice->Pnp, 0xfff);
```

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```
  temu_apbSetType(&MyDevice->Pnp, 1); // APB I/O space

  return MyDevice;
}

void
dispose(void *Obj)
{
  MyDevice *Dev = (MyDevice*)Obj;
  free(Irq);
}

// Define the device interface
void
reset(void *Obj, int ResetKind)
{
}

void
mapDevice(void *Obj, uint64_t Addr, uint64_t Len)
{
  MyDevice *Dev = (MyDevice*)Obj;
  temu_apbSetAddr(&Dev->Pnp, Addr);
}


temu_DeviceIface DeviceIface = {
  reset, // Called on resets
  mapDevice, // Called when a device is mapped to a memory location.
};



TEMU_PLUGIN_INIT
{
  temu_Class *cls = temu_registerClass("MyClass", create, dispose);

  temu_addInterface(cls, "ApbIface", "ApbIface", &ApbIface);
  temu_addInterface(cls, "DeviceIface", "DeviceIface", &DeviceIface);

}
```

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Chapter 4. Bus Models

4.1. CAN

TEMU provides support for CAN bus based devices. The bus model interfaces are available in: `temu-c/Bus/Can.h`. In addition to the interfaces one CAN bus model is provided. Since TEMU 5, this bus model also supports CAN-FD (Flexible Data Rate), which has a different frame format than classic CAN but is typically transmitted over the same physical wires, with CAN-FD devices beeing able to understand classic CAN messages, but classic CAN devices ignoring CAN-FD messages.

As CAN is a multi-node bus, a bus model object is needed to route messages to the relevant destination.

There are two types of CAN classes that can be created, firstly bus models and secondly device models. A bus model is responsible for routing messages to the device models, and the device models implement CAN message reception logic. Classic CAN and CAN-FD devices use the same interface. CAN-FD devices may simply implement additional functions that classic CAN devices may initialize with `NULL`.

The standard `SimpleCANBus` bus model, provides fairly simple logic. It routes a sent message to all devices connected to the CAN bus (except the sender device). However, CAN devices often implements filtering of message IDs in hardware, and this filtering (which is typically based on a mask and code pair) can be used to define a smart CAN bus model. Such a model would route frames using internal routing tables.



A smart CAN bus model will by definition be system specific. It's routing will depend on the system specific allocation of message IDs.

4.1.1. Interfaces

The interesting interfaces are defined in the `temu-c/Bus/Can.h` header. This header also define inline functions to help construct CAN frames.

```
typedef struct {
  uint8_t Data[8];
  uint32_t Flags;
  uint8_t Length;
  uint8_t Error;
} temu_CanFrame;

typedef struct {
  uint32_t ID;
  uint32_t Flags;
  uint8_t Length;
  uint8_t Data[64];
} temu_CanFDFrame;
```

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```
struct temu_CanDevIface {
  void (*connected)(void *Dev, temu_CanBusIfaceRef Bus);
  void (*disconnected)(void *Dev);
  void (*receive)(void *Dev, temu_CanFrame *Frame);
  void (*receiveFD)(void *Dev, temu_CanFDFrame *Frame);
};

struct temu_CanBusIface {
  void (*connect)(void *Bus, temu_CanDevIfaceRef Dev);
  void (*send)(void *Bus, void *Sender, temu_CanFrame *Frame);
  void (*enableSendEvents)(void *Bus);
  void (*disableSendEvents)(void *Bus);
  void (*reportStats)(void *Bus);
  void (*setFilter)(void *Bus, temu_CanDevIfaceRef Dev, int FilterID,
                    uint32_t Mask, uint32_t Code);
  void (*sendFD)(void *Bus, void *Sender, temu_CanFDFrame *Frame);
};
```

The CAN frame is central to the transmission of CAN data. It is not a bit by bit representation of the CAN protocol, rather it is a simplified format that omit bits that are implicit and ensures that relevant bits such as RTR is fixed in location.

If a real CAN frame is needed, the frame struct need to be transformed to the needed representation. Note that the struct is optimised for performance (e.g. Data is first and can be bitcopied as a uint64).

Device models are typically simple, they implement the `connected`, `disconnected` and `receive` functions. If the device needs registers and MMIO handling, it tends to get more complex.

The device and bus interface support `connect` and `disconnect` events. The purpose of these are to support hot-plugging of CAN devices. As these `connect` and `disconnect` events are supported, the normal `connect` command should not be used when connecting a CAN device, rather the `can-connect` command is to be used.

Classic CAN and CAN-FD

Classic CAN devices do not need to implement the `receiveFD` function, and bus models to which only classic can devices are connected do not need to implement the `sendFD` function. It is the responsability of the bus model to convert between `temu_CanFrame` and `temu_CanFDFrame` where necessary and possible.

4.1.2. Commands

Two CAN bus related commands are provided:

Name	Description
can-connect	Connect a CAN device to a CAN bus.

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Name	Description
can-disconnect	Disconnect CAN device from a CAN bus.

4.1.3. Classes

The SimpleCAN bus class provides a CAN bus model. In the `SimpleCANBus` class, messages are forwarded to all connected devices (except the sending one). If this results in performance issues, it is possible to write a filtering CAN bus model.

4.1.4. SimpleCANBus Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
devices	temu_IfaceRefArray	CAN devices attached to bus
stats.lastReportSentBits	uint64_t	Statistics
stats.sentBits	uint64_t	Statistics

Interfaces

Name	Type	Description
CanBusIface	CanBusIface	CAN Bus Interface

Commands

Name	Description
delete	Dispose instance of SimpleCANBus

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Classic CAN and CAN-FD

The `SimpleCANBus` will convert classic CAN struct frames into CAN-FD frames only if another device on the bus does not implement the `receive` function. Similarly, it will only try to convert CAN-FD frame structs into classic CAN frame structs if another device on the bus does not impelemnt the `receiveFD` function. Not every CAN-FD frame can be converted into a classic CAN frame, in which case it is not forwarded to that device, which mimics what happens in hardware where classic CAN devices will automatically ignore CAN-FD frames.

4.1.5. Fault Injection

The CAN bus is multi-node bus and modification of traffic can be done using notifications.

The `SimpleCANBus` model emits a notification named `temu.canSend` for classic CAN frames and `temu.canSendFDFrame` for CAN-FD ones. The, notification receives a pointer to the `temu_CanFrame` /`temu_CanFDFrame` as the notification info. Unlike for devices connected to the bus, there is no automatic conversion even if possible.

Fault injection can thus be done by modifying the `Error` field in the frame. Or by modifying the data content directly.

The notifications are emitted before the frame is forwarded to the receivers.

Another way of injecting faults is to have a custom model injecting frames when a scheduled event is triggered.

To be able to drop frames in transit, a *man-in-the-middle* model is needed between the bus and the receiving device model.

4.1.6. Examples

This example shows how to create a simple CAN device and connect it to a bus model.

Listing 4. Connecting CAN Devices

```
exec ut700.temu
import MyCanDevice
# Create a can bus
create class=SimpleCANBus name=canbus0
create class=MyCANClass name=mycan0

can-connect bus=canbus0:CanBusIface dev=occan0:CanDevIface # From ut700
can-connect bus=canbus0:CanBusIface dev=mycan0:CanDevIface
```

The next example shows how to implement a simple CAN device

Listing 5. Simple CAN Device Example

```
#include "temu-c/Bus/Can.h"
```

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```c
#include "temu-c/Support/Objsys.h"

// This is a device / RTU model, it needs to know about its CAN bus
typedef struct MyCanDevice {
  temu_Object Super;
  temu_CanBusIfaceRef Bus;
} MyCanDevice;


void*
create(const char *Name, int Argc, const temu_CreateArg *Argv)
{
  MyCanDevice *Dev = malloc(sizeof(MyCanDevice));
  memset(Dev, 0, sizeof(MyCanDevice);
  return Dev;
}

void
dispose(void *Obj)
{
  MyCanDevice *Dev = (MyCanDevice*)Obj;
  free(Dev);
}

// Implement the CAN Device interface

void
connected(void *Obj, temu_CanBusIfaceRef Bus)
{
  MyCanDevice *Dev = (MyCanDevice*)Obj;
  Dev->Bus = Bus;
  temu_logInfo(Dev, "connected to CAN bus");
}

void
disconnected(void *Obj)
{
  MyCanDevice *Dev = (MyCanDevice*)Obj;
  Dev->Bus = {NULL, NULL};
  // NOTE: This should also stop any pending events related to
  // message transmissions
  temu_logInfo(Dev, "disconnected from CAN bus");
}

void
receive(void *Dev, temu_CanFrame *Frame)
{
  temu_logInfo(Dev, "received CAN message with msg id %u",
               temu_canGetIdent(Frame));
```

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```
}

temu_CanDevIface CanIface = {
  connected,
  disconnected,
  receive,
  // receiveFD is NULL initialized, and so the bus will
  // convert temu_CanFDFrames into temu_CanFrame if possible,
  // or just not forward the CAN-FD frame at all if not.
};

TEMU_PLUGIN_INIT
{
  temu_Class *cls = temu_registerClass("MyCANClass", create, dispose);

  temu_addProperty(cls, "CANBus", teTY_IfaceRef, 1);
  temu_addInterface(cls, "CanDevIface", "CanDevIface", &CanIface);

}
```

4.2. Ethernet

TEMU provides support for Ethernet bus based devices. To support the development of custom MAC controllers, TEMU provides three generic models.

The `MDIOBus` model implements MDIO routing. As multiple MDIO devices can be connected to the same bus, a bus model is needed.

A `GenericPHY` model is implemented to expose the MDIO interface to the MAC models.

The `GenericPHY` model can be attached to the `EthernetLink` model. `EthernetLink` is responsible for routing EthernetFrames between registered nodes. It has two routing lists. Firstly, a list of *promiscuous* nodes that will receive all messages. Secondly, a routing map for non-promiscuous nodes.

When the `EthernetLink` model receives a frame, it forwards the frame to all the promiscous nodes. Then, it routes it to the destination MAC.

The `EthernetLink` assumes unique MACs, thus it will emit a warning in the case of a MAC address collission.

4.2.1. Connecting Devices

An ethernet link must be connected to its attached PHYs. Connection is done using the `connect` command.

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Example 1. Connect Syntax

```
ethlink0.connect device=phy0:PHYIface
```

Example 2. Disconnect Syntax

```
ethlink0.connect device=phy0:PHYIface
```

4.2.2. Checksums

Ethernet frames typically have a checksum that is generated and checked by hardware. To optimise the bus model, it is expected that MAC models supports opt in control on checksum generation and checking. This applies to all checksums, including Ethernet frame CRCs and IP header, TCP, UDP checksums. Since the Ethernet link is fully virtual, data cannot normally be corrupted in transit. Thus checksum checking and generation would be a waste of cycles.

There are still several usecases where one want to enable checksums:

- When viewing capture files with *Wireshark*, the tool will complain if ethernet CRCs are invalid.
- When receiving frames in a device which do not have hardware assisted CRC checking.

Thus, normally Ethernet CRC generation and checking will be disabled, while TCP/UDP/IP checksum generation (but not hardware checking) will be enabled.

4.2.3. Auto Negotiation

The ethernet model supports autonegotiation for transfer speed capabilities.

The process is based on issuing an auto-negotiation request to the ethernet link model. The link will then issue auto-negotiation requests to each attached PHY, and finally call `autonegotiateDone` for all attached PHYs.

Each PHY will be called with the current known capabilities. It should return the same capabilities with potentially some of them cleared.

The actual final capabilities are reported with `autonegotiateDone`.

There, a PHY will select the highest priority common mode. Which by the standard is:

1. 40GBASE T FD
2. 25GBASE T FD
3. 10GBASE T FD
4. 5GBASE T FD
5. 2.5GBASE T FD
6. 1000BASE T FD

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7. 1000BASE T HD
8. 100BASE T2 FD
9. 100BASE TX FD
10. 100BASE T2 HD
11. 100BASE T4
12. 100BASE TX HD
13. 10BASE T FD
14. 10BASE T HD



TEMU does not support emulation of 2.5 GBASE and above at this moment.

4.2.4. Ethernet Frames

Ethernet frames in TEMU are structs containing a flag field, data and an optional preamble.

The data field is a COW buffer which contains the level 2 ethernet frame data.

The preamble will typically be ignored and not set for most MACs. However if it is set to somthing non-standard, a device can indicate this by setting the flag `TEMU_ETH_NON_STANDARD_PREAMBLE`.

4.2.5. Ethernet Link

Frame Capture

The ethernet link can be instructed to dump all traffic to a PCAPNG file.



Wireshark may flag frames as having invalid CRCs. To avoid this you can enable CRC generation in the MAC, or turn off checking in Wireshark.

To enable capture execute the enableCapture command ont he ethernet link.

Example 3. TEMU 3 Command Syntax

```
ethlink0.enableCapture file="foo.pcap"
```

Example 4. Legacy Global Command (TEMU 2) Syntax

```
ethernet-link-enable-capture link=ethlink0 file="foo.pcap"
```

Live Monitoring

TEMU 4.5 added the option to monitor Ethernet traffic live. This is done using:

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Example 5. Live Network Capturing

```
ethlink0.enableCapture file="foo.pcap" named-pipe=1
```

When adding the named pipe option, the command will block until Wireshark connects to the pipe. For more information on how to connect Wireshark to a named pipe see the Wireshark Wiki (external link).

4.2.6. @EthernetLink Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @EthernetLink
new	Create new instance of EthernetLink

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

4.2.7. EthernetLink Reference

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Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
bitRate	uint64_t	Bit rate in bit/s
bytesSent	uint64_t	Total bytes sent on link
bytesSentInLastReport	uint64_t	Last reported data
framesSent	uint64_t	Number of frames sent
replayStorageIfaceRef	temu_IfaceRef/ <unknown>	Interface for replaying data after rollback.

Interfaces

Name	Type	Description
EthernetIface	temu::EthernetIface	
ReplayPlaybackIface	ReplayPlaybackIface	

Ports

Prop	Iface	Description
replayStorageIfaceRef	ReplayPlaybackIface	Data replay system

Commands

Name	Description
add-delay	Add delay and/or replay for a device with given MAC

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Name	Description
connect	Connect device to ethernet link
delete	Dispose instance of EthernetLink
disconnect	Disconnect device from ethernet link
down	Bring link down
enableCapture	Enable capture to PCAPNG file
inject	Inject frame with given paramteres MAC
plink	Print link info
up	Bring link up

Command add-delay Arguments

Name	Type	Required	Description
delayReceive	int	no	Delay value in cycles for messages sent by the device
delaySend	int	no	Delay value in cycles for messages received by the device
mac	string	yes	Mac of the device to delay or replay
replay	double	no	Replay transmissions sent by the device

Command connect Arguments

Name	Type	Required	Description
device	interface	yes	Device to connect

Command disconnect Arguments

Name	Type	Required	Description
device	interface	yes	Device to connect

Command down Arguments

Name	Type	Required	Description
device	interface	yes	Device to take down

Command enableCapture Arguments

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Name	Type	Required	Description
file	path	yes	Name of capure file.
named-pipe	int	no	Capture to named pipe for wireshark live capture.

Command inject Arguments

Name	Type	Required	Description
data	string	yes	Data in HEX
destination	string	yes	Destination MAC
source	string	yes	Source MAC

Command up Arguments

Name	Type	Required	Description
device	interface	yes	Device to take up

4.2.8. Generic PHY

The `GenericPHY` is a PHY / MII device which supports both the MDIO interface and the PHY interface for sending/receiving ethernet frames.

The `GenericPHY` device class by default enables support for BASE10, BASE100 and BASE1000 transfers. To only enable specific speed modes, the constructor accepts arguments:

- base10:1
- base100:1
- base1000:1

If any of these are set, the unset ones will be disabled.

Thus by default a PHY supports all BASE10, BASE100 and BASE1000 modes. By setting the base10 argument, only BASE10 modes will be supported. By setting base10 and base 100 arguments, only BASE10 and BASE100 will be supported.

At present it is not possible to control the support on a lower level.

4.2.9. @GenericPHY Reference

Properties

Name	Type	Description
Class	*void	Class object

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Name	Type	Description
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GenericPHY
new	Create new instance of GenericPHY

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

4.2.10. GenericPHY Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
autoNegAdvertisment	uint16_t	Auto negotiation advertisment register
autoNegotiationExpansion	uint16_t	Auto negotiation expansion register
basicModeConfig	uint16_t	Basic mode config register
basicModeStatus	uint16_t	Basic mode status register
config.address	uint8_t	PHY address reported in the vendor specific registers
config.vendor	uint8_t	Vendor specific registers: 0 none, 1 DP83848, 2 LAN8742A
ethernetLink	temu_IfaceRef/ <unknown>	Ethernet link.
linkPartnerAbility	uint16_t	Link partner ability register
macDevice	temu_IfaceRef/ <unknown>	MAC device.
phyID	[uint16_t; 2]	Physical ID registers

Interfaces

Name	Type	Description
MDIOIface	temu::MDIOIface	
PHYIface	temu::PHYIface	

Commands

Name	Description
delete	Dispose instance of GenericPHY

4.2.11. MDIO Bus

The MDIO bus distributes MDIO control messages and supports routing of them. The MDIO bus use the same interface as an MDIO device. Thus, if only one MDIO device (e.g. GenericPHY) is available no MDIO bus instance is needed.

4.2.12. @MDIOBus Reference

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @MDIOBus
new	Create new instance of MDIOBus

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

4.2.13. MDIOBus Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
macDevice	temu_IfaceRef/ <unknown>	MAC controller.
phyDevices	[temu_IfaceRef; 32]/ <unknown>	MDIO interface of PHYs.

Interfaces

Name	Type	Description
MDIOIface	temu::MDIOIface	

Commands

Name	Description
delete	Dispose instance of MDIOBus

4.2.14. Implementing a MAC Model

TEMU comes with some bundled MAC models. In some cases it will be needed to implement additional project specific MAC models.

Consult the `eth-device` example for more info.

4.2.15. Host Network Integration

The NAT bridge supports the routing of network packets between an external real network and the simulated Ethernet link.

This enables for example Telnet or custom network applications to be used for testing target software. A target OS supporting GDB RSP could provide direct intrusive debugging support via the GDB RSP protocol, DAP or TCF.

Currently the NAT bridge only support IPv4 and TCP, it does not support IPv6 and/or UDP.

4.2.16. @NATBridge Reference

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @NATBridge
new	Create new instance of NATBridge

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

4.2.17. NATBridge Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
config.frameDelay	uint64_t	Delay for each frame in nanoseconds.
config.ipv4.nat.externalSegmentSize	uint32_t	Max size of data read from external ports and forwarded in single frames.
config.ipv4.tcp.ackDelay	uint32_t	ACK delay (how many packets between acks): 0 = immediate (every packet is acked)
config.ipv4.tcp.ackDelayTimeout	uint32_t	ACK delay timeout in ms, if ACKs are not sent immediately, a timeout is set to ensure acks within a maximum time window
config.ipv4.tcp.finTimeout	uint32_t	2 Maximum Segment Lifetime in seconds. Controls waiting after FIN reception.
config.ipv4.tcp.maxRetransmissions	uint32_t	Number of retransmissions to do before giving up.
config.ipv4.tcp.retransmissionTimeout	uint32_t	Retransmission timeout in ms
config.ipv4.tcp.roundTripTime	uint32_t	Measured round-trip time.
config.ipv4.tcp.windowSize	uint16_t	Base TCP window size
ethernetLink	temu_IfaceRef/ <unknown>	Ethernet link.

Interfaces

Name	Type	Description
PHYIface	temu::PHYIface	PHY interface for Ethernet frames
StreamIface	temu::streamIface	TCP stream interface

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Commands

Name	Description
add-nat	Add NAT mapping
delete	Dispose instance of NATBridge
do-arp-request	Send an ARP request message
enable-arp-dumps	Enable ARP frame dumps
enable-crlf-substitution	Enable CRLF substitution on incoming packets, replaces CRLF sequences with '\0' which can simplify protocol debugging using Telnet
parp	Print ARP resolutions
pmap	Print port maps
set-ip	Set IP address
set-mac	Set MAC address
start-nat	Create stat NAT server
stop-nat	Stop the NAT server: closes the open connections towards the target, releases the sockets and joins the server threads. start-nat can be used again afterwards

Command add-nat Arguments

Name	Type	Required	Description
external-port	int	yes	External port (real network)
internal-addr	string	yes	IP address of target
internal-port	int	yes	Internal port (TEMU network)
name	string	yes	Name of TAP device

Command do-arp-request Arguments

Name	Type	Required	Description
ip	string	yes	IP address to query MAC address for

Command set-ip Arguments

Name	Type	Required	Description
ip	string	yes	IP address to set

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Command set-mac Arguments

Name	Type	Required	Description
mac	string	yes	MAC address to set

4.3. MIL-STD-1553

This document describes the TEMU MIL-STD-1553 bus model and its interfaces. The MIL-STD-1553 standard is often referred to as simply milbus or 1553.

The 1553 protocol is described in detail in the well known "MIL-STD-1553 Tutorial" document from AIM GmbH (formerly published by Condor). It is recommended that persons involved with modelling bus controllers and remote terminals keep a copy of that document at close hand.

The TEMU support for the 1553 protocol consist of a bus interface (`Mil1553BusIface`), a bus model (`MilStd1553Bus`) and a bus client interface (`Mil1553DevIface`).

This approach enables the user to not only implement remote terminal models, but also to implement their own bus models. The latter is of interest if the bundled model is found not suitable.

Most users will be interested in implementing remote terminal models, but bus controllers are also possible as they use the same interface.

4.3.1. Bus Model

The 1553 bus model is available as a class with the name `MilStd1553Bus` in the TEMU "BusModels" plugin.

4.3.2. Configuration

The bus model is configured using the `Mil1553BusIface`. This is done by calling the connect function in order to attach remote terminal at given subaddress.

`SetBusController` should be called to set the current bus controller



It is possible to set the current bus controller at runtime, this is useful for handovers.

The construction of a network with 1553 devices is simplified by using the following commands in the command line interface:

- mil-std-1553-connect bus=b rt=rt addr=1
- mil-std-1553-disconnect bus=b addr=1
- mil-std-1553-setbc bus=b bc=bc

4.3.3. @MilStd1553Bus Reference

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @MilStd1553Bus
new	Create new instance of MilStd1553Bus

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

4.3.4. MilStd1553Bus Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
bc	temu_IfaceRef/ <unknown>	Bus controller.
devices	[temu_IfaceRef; 32]/ <unknown>	Remote terminals.
inhibitChA	uint8_t	
inhibitChB	uint8_t	
lastCmd	uint16_t	
receiverRT	int8_t	
stats.lastReportSentWords	uint64_t	
stats.sentWords	uint64_t	
transmitterRT	int8_t	

Interfaces

Name	Type	Description
Mil1553BusIface	Mil1553BusIface	

Commands

Name	Description
connect	Connect device to 1553 bus.
delete	Dispose instance of MilStd1553Bus
disconnect	Disconnect device from 1553 bus.
setBC	Set bus controller for 1553 bus.

Command connect Arguments

Name	Type	Required	Description
addr	int	yes	RT address.

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Name	Type	Required	Description
rt	object	yes	Connect RT to bus.

Command disconnect Arguments

Name	Type	Required	Description
addr	int	yes	RT address.

Command setBC Arguments

Name	Type	Required	Description
bc	object	yes	Bus controller object.

4.3.5. @MilStd1553BusLogger Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @MilStd1553BusLogger
new	Create new instance of MilStd1553BusLogger

Command new Arguments

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Name	Type	Required	Description
bus	object	no	Bus object to attach to (see also attach/detach commands).
fmt	string	yes	Format (csv
pcap	pcapng	log).	name

4.3.6. MilStd1553BusLogger Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
bus	*void	Bus object to monitor.
statPeriod	double	Statistics report period in seconds, set to positive enables reports.

Commands

Name	Description
attach	Attach to bus.
delete	Dispose instance of MilStd1553BusLogger
detach	Detach from bus.

Command attach Arguments

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Name	Type	Required	Description
bus	object	yes	Bus object to attach to.

4.3.7. Notifications

The default TEMU milbus model issues the following notifications:

Name	Description	Param Type
temu.mil1553Stat	Statistics notification.	temu_Mil1553Stats*
temu.mil1553Send	Valid message in transit.	temu_Mil1553Msg*

The statistics notification is issued when calling the `reportStats` function in the bus interface. The user can call this function from a timed event handler if needed. It would be possible to force statistics reporting at a PPS tick, i.e. by having the a PPS device issue the call. This way the stat event can be used to monitor whether the system keeps the milbus budget.

The send notification receives a pointer with the actual message in transit. Before it has been delivered to the remote terminal, but after the bus object has rejected any messages transmitted illegally. The notification handler is free to modify the message. For example it is possible to set the Err field in the message struct to inject a transfer error. The RT can then set the message error bit in the status word.

4.3.8. Limitations

The bus object does not support bus monitors in the normal sense. However, it is possible to turn on the `temu.mil1553Send` notification and listen in on all traffic using this notification interface.

For the command line support, only models with one and only one device interface with the name `Mil1553DevIface` is supported. This may change in the future.

4.3.9. API

Interfaces

Listing 6. MIL-STD-1553B Bus Interface

```
typedef struct temu_Mil1553BusIface {
  void (*connect)(void *Bus, int Subaddr, temu_Mil1553DevIfaceRef Device);
  void (*disconnect)(void *Bus, int Subaddr);
  void (*reportStats)(void *Bus);
  void (*send)(void *Bus, void *Sender, temu_Mil1553Msg *Msg);

  // Controls whether events should be issued at send calls
  void (*enableSendEvents)(void *Bus);
  void (*disableSendEvents)(void *Bus);
  void (*setBusController)(void *Bus, temu_Mil1553DevIfaceRef Device);
```

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```
} temu_Mil1553BusIface;
```

Listing 7. MIL-STD-1553B Device Interface

```
typedef struct temu_Mil1553DevIface {
  void (*connected)(void *Device, temu_Mil1553BusIfaceRef Bus, int SubAddr);
  void (*disconnected)(void *Device, temu_Mil1553BusIfaceRef Bus, int SubAddr);
  void (*receive)(void *Device, temu_Mil1553Msg *Msg);
} temu_Mil1553DevIface;
```

4.3.10. Writing Clients

Bus Controllers and Remote Terminals

Bus controllers and remote terminals can be implemented using the `Mil1553BusIface` interface. This interface is defined in `temu-c/Bus/MilStd1553.h`.

The interface consist of the connected, disconnected and receive functions. These are all mandatory and they are called whenever a virtual cable is connected and disconnected, or when a 1553 bus message is received.

A remote terminal needs to know about the bus it is connected to so it can use the send function in the Mil1553BusIface interface.



Do not call the bus send function from the device receive function, doing so will result in undefined behaviour. If a response is to be issued due to handling of a receive, ensure that an event is posted on the model's event queue source.

The 1553 API follows the standard and subdivides transactions in phases. The phases are: command, data, status and mode command phases. To send a receive command, the bus controller will first send a message of the type `teMT_Cmd`, followed by a `teMT_Data` message. The remote terminal is then expected to respond with a `teMT_Stat` message. The RT and BC models are responsible for issuing the different messages with delays. Delays can be computed using the `temu_mil1553TransferTime()` function.

Messages should be sent in whole when they are supposed to arrive. This means that the bus controller model can immediately raise any needed interrupts when a message is complete.



The TEMU default 1553 bus model will print error messages if an RT does not follow the 1553 protocol phases correctly. E.g. sending a status response to a broadcast message, will trigger a message.

Listing 8. Remote Terminal Example

```
void
receive(void *Device, temu_Mil1553Msg *Msg)
{
  MyRT *RT = (MyRT*)Device;
```

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```
  //...
  // Start sending response
  temu_eventPostNanos(RT->Super.TimeSource, RT->TransferCompleteEvent,
                      temu_mil1553TransferTime(1), // One word for status message
                      teSE_Cpu);
}

void
transferComplete(temu_Event *Ev)
{
   MyRT *RT = (MyRT*)Ev->Obj;

   uint16_t Stat = computeStatWord(RT);
   temu_Mil1553Msg Msg = temu_mil1553CreateStatMsg(&Stat);

   RT->Bus.Iface->send(RT->Bus.Obj, RT, &Msg); // Send the message
}
```

4.3.11. Bus Monitors

The 1553 bus interface does not support the implementation of bus monitors directly. The reason for this is that, the notifications already allows the simulator to inspect all the bus traffic. The notification interface can also be used to modify traffic in flight (e.g. to flip the error flags in the message object).

Terma appreciates that there may be need for some users to support modelling of bus monitors, please contact Terma if this is needed.

4.3.12. Capture Device

TEMU is bundled with a MILBUS capture device that enables capturing of the bus traffic. There are three supported options for message capture:

- Logging command words issued to the TEMU log with partial decoding
- CSV output with command words and partial decodes of them
- PCAPNG file with all data transferred. File can be loaded in Wireshark if needed.

To create a logging capture device, create the bus capture instance using:

For logging:

Listing 9. Logging Traffic

```
MilStd1553BusCapturer.new name=milbus-cap0 fmt=log bus=milbus0
```

For CSV output (into milbus0.csv):

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Listing 10. Capture to CSV

```
MilStd1553BusCapturer.new name=milbus-cap0 fmt=csv bus=milbus0
```

For PCAPNG output (into milbus0.pcapng):

Listing 11. Capture to PCAPNG

```
MilStd1553BusCapturer.new name=milbus-cap0 fmt=pcapng bus=milbus0
```

Do not forget to set the time source for the capture device:

Example 6. Setting The Time Source

```
connect-timesource obj=milbus-cap0 ts=cpu0
```

While the logging and CSV modes should be clear enough, there are some notes to be providede regarding the PCAPNG format.

Firstly, the capture model captures logical units in the protocol. That is, command words are captured by themselves, as is status messages and data messages.

Secondly, the capture model use the flags in the frame block to mark where the data came from. That is, it flags unicast, and broadcast messages as such, and it also flags the direction as outbound for frames emitted by the BC (e.g. command words, mode codes, data sent to RTs etc) and inbound for data sent from RTs.

Thirdly, `LINKTYPE_USER0` is used for the device type (there is no standardised milbus link type). This linktype is not supported directly by Wireshark, and a dissector needs to be implemented to make frames more human readable.

4.4. PCI



PCI emulation is experimental.

TEMU provides support for PCI bus based devices. This is based on a split between bridges, devices and buses.

A generic `PCIBus` class exists to provide bus connectivity. Devices of this class maintains the configuration space object.

When a BAR is written the memory and I/O spaces are updated automatically.

Normally the IO and memory spaces can be mapped directly into target memory. That said, som bridges may remap addresses. In that case the bridge should provide memory interfaces much like an MMU.

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4.4.1. Bridge Modelling

TBW

4.4.2. Device Modelling

While it is sometimes necessary to implement PCI bridges (e.g. GRPCI2), the more common task is to implement PCI devices.

A PCI device in TEMU must support the following interfaces:

- PCIDevIface implementing the PCI device interface. Used for for accessing config info about the PCI device.
- MemAccessIface[6] implementing the PCI memory access functions for each BAR.
- ExpROMAccessIface implementing accesses to PCI expansion ROM.
- ConfigAccessIface implementing the memory access interface for the configuration space.

That means that MemAccessIface may be either IO or PCI mem. This depends on the hard coded value in the bar.

4.4.3. Examples

An example of a PCI device is provided in `share/temu/examples/pci-device/`.

4.5. Serial / UART

Serial ports are emulated using the `SerialIface`.

4.5.1. Console

The serial console is a simple endpoint for serial traffic. It echos received data to `stdout`, and optionally logs the data in an unbounded log.

Loading the Plugin

```
import Console
```

Configuration

Creation

The Console class is defined in `libTEMUConsole.so`. The constructor takes no parameters.

Options

`config.caretControl` can be used to eliminate some VT100 characters that are printed to the console

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otherwise.

`config.recordTraffic` can be set to enable data recording in the console model, this data can then be extracted with the API.

4.5.2. @Console Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @Console
new	Create new instance of Console

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

4.5.3. Console Reference

Properties

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
config.caretControl	uint8_t	
config.outFile	*char	File name to write TTY log to.
config.recordTraffic	uint8_t	
config.reformatNonPrintable	uint8_t	
injectedIndex	uint32_t	
injectedSize	uint32_t	
injectedString	*char	
lastByte	uint8_t	
outByte	uint8_t	
serial	temu_IfaceRef/ <unknown>	Serial connection.

Interfaces

Name	Type	Description
LineDataLoggerIface	LineDataLoggerIface	
SerialIface	SerialIface	

Ports

Prop	Iface	Description
serial	SerialIface	serial port

Commands

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Name	Description
delete	Dispose instance of Console
dump-traffic	Return console/UART traffic captured since config.recordTraffic was enabled.
inject	Inject string

Command dump-traffic Arguments

Name	Type	Required	Description
from	int	no	Starting line index

Command inject Arguments

Name	Type	Required	Description
string	string	yes	String to inject

Limitations

- The record buffer cannot be cleaned without deleting the console object.
- Caret control only omits caret sequences from being put on stdout (especially nice when booting Linux). It doesn't act on the sequences in any way at the moment e.g. a delete character will be ignored and not actually delete anything.
- The record buffer will not be snapshotted.

4.5.4. Console Graphical User Interface

The serial console ui is a simple graphical endpoint for serial traffic. It forks of a separate process which display a new window with the serial port output. This window also handles interactive input, meaning that you can for example type commands to a command line interface provided by the software running in the emulated environment.

The console window supports limited VT100 emulation.

Loading the Plugin

```
import ConsoleUI
```

Configuration

No specific configuration needed.

Creation

The ConsoleUI class is defined in `libTEMUConsoleUI.so`. The constructor takes no parameters.

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4.5.5. @ConsoleUI Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @ConsoleUI
new	Create new instance of ConsoleUI

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

4.5.6. ConsoleUI Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)

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Name	Type	Description
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
config.appendOutFile	uint8_t	
config.outFile	*char	File name to write TTY log to.
serial	temu_IfaceRef/ <unknown>	Serial connection.

Interfaces

Name	Type	Description
ObjectIface	ObjectIface	
SerialIface	SerialIface	

Ports

Prop	Iface	Description
serial	SerialIface	serial port

Commands

Name	Description
delete	Dispose instance of ConsoleUI

Limitations

As with all other models, problems not listed here should be reported to Terma as they may indicate bugs in the software.

- The Console UI requires QT 4 to be installed (e.g. with your package manager) and any needed support libraries for QT. Thus the console in particular has a lot of extra dependencies over the rest of the emulator. If you are running this on specific systems and the console does not work, please report this to Terma.
- The console always do VT100 emulation, the emulation cannot be disabled.
- Only partial VT100 support exists. The supported CSIs include colors and cursor movements. Some CSIs may be missing.

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- The console does not echo input back automatically, this is typically done by the remote serial end. Consequently, you will not see any characters if you type them in the console and the remote does not echo back.

4.6. Signal

The signal interface represents a single bit signal.

The interface can be used to implement GPIO and other pin based interfaces.

4.7. SpaceWire

TEMU provides support for SpaceWire based devices. It also provides helpful functions for RMAP commands decoding. The bus model interfaces are available in: `temu-c/Bus/Spacewire.h`. In addition to the interfaces a simple SpaceWire Router model is provided.

Spacewire is a point to point bus. Two devices can be connected directly while multiple devices can be connected through a router. A SpaceWire Route receives a packet on a port and forward it to another, where the destination device is connected.

Spacewire uses wormhole routing. The sender device provides the list of addresses (each address is an 8-bit value) required to reach the destination. Each node in the path is supposed to strip the first byte and use it to select the port used to forward the packet.

4.7.1. Interfaces

The interesting interfaces are defined in the `temu-c/Bus/Spacewire.h` header.

Listing 12. SpaceWire Interfaces

```
typedef enum {
  teSMT_Data = 1,
  teSMT_Err = 2,
  teSMT_Time = 3,
} temu_SpwPacketType;

typedef struct temu_SpwPacket {
  temu_SpwPacketType MsgType;
  temu_Buff PktData;
  uint8_t Flags;
} temu_SpwPacket;

typedef enum {
  teSPWLS_ErrorReset = 1,
  teSPWLS_Ready = 2,
  teSPWLS_Started = 3,
  teSPWLS_Connecting = 4,
  teSPWLS_Run = 5,
```

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```
  // Not to be used by normal devices:
  teSPWLS_FIFO = 6
} temu_SpwLinkState;

struct temu_SpwPortIface {
  void (*receive)(void *Device, void *Sender, temu_SpwPacket *Pkt);
  void (*signalLinkStateChange)(void* Device, temu_SpwLinkState LinkState);
  temu_SpwLinkState (*getOtherSideLinkState)(void* Device);
  void (*connect)(void *Device, temu_SpwPortIfaceRef Dest);
  void (*disconnect)(void *Device);
  uint64_t (*timeToSendPacketNs)(void* Device, uint64_t PacketLength);
};
```

While the SpaceWire protocol is character based, to have better performances TEMU transfers full messages with a single call on the port interface. Example of messages are a data packet, an RMAP packet and a time code. Control characters like FCT (flow control) are abstracted away.

The SpaceWire packet structure is used to pass a packet between nodes. The MsgType field identifies if the packet is a timecode, a complete data packet (ending with EOP) or an incomplete data packet (ending with EEP). The PktData field contains the packet data or the time code value.

A TEMU buffer is used to hold the data. This data structure has been implemented to handle SpaceWire packets in a performant way. It allows to acquire a reference to a part of the original data so that a copy of data is not required for each node due to wormhole routing stripping. It also free the memory used to store the original message when no more references are active. This way, destination devices can maintain the data as long as needed without coping it.

SpaceWire links are full-duplex. The SpaceWire link is modeled by simply having each device implementing a port interface and holding a reference to other end port. This allows comunication in both directions simultaneously.

SpaceWire devices often have several connections port. The SpwPortIface is meant to be implement for each port a device intends to provide.

`temu-c/Bus/Spacewire.h` header also define functions to help decode RMAP packets:

Name	Description
temu_spwRmapDecodePacket	Provided a SpaceWire Rmap packet attempts to decode it.
temu_spwRmapDecodeBuffer	Provided a buffer containing a SpaceWire Rmap packet attempts to decode it.
temu_spwRmapHeaderReplySize	Returns the total packet-size required to reply to the command.
temu_spwRmapEncodeReadReplyHeaderForPacket	Encodes the reply for a read command.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Description
temu_spwRmapEncodeRmwHeaderForPacket	Encodes the reply for a rmw command.
temu_spwRmapEncodeWriteReplyHeaderForPacket	Encodes the reply for a write command.
temu_spwRmapCRCNextCode	Provided the previous calculated crc and a the current byte returns the next CRC value.
temu_spwRmapCRC	Calculates the CRC over the specified data.

The `teSPWLS_FIFO` link state should not be used by normal SpaceWire devices. It is intended for ports used to transfer SpaceWire packets without actually using the SpaceWire protocol. As an example, this is used for the bridge between GrLibs GRSPFI SpaceFibre controller and the GRSPWROUTER on the same SoC.

4.7.2. Limitations

The following deviations from real hardware are known to exist with this model:

- When two different devices try to access the same device the two accesses will happend simultaneously. This should not be the case, the accesses should be sequential (the second device should wait for the bus to be free). This issue will be solved in the future when bus-reservation feature will be implemented.

4.7.3. Commands

The following commands are provided:

Name	Description
spw-connect	Connect the two SpaceWire port interfaces provided as parameters
spw-disconnect	Disconnect the two SpaceWire port interfaces provided as parameters

4.7.4. Classes

SpwRouter

The SpwRouter class provides a simple SpaceWire Router that lets the user configure the mapping between the packet-address and the port that will be used to forward the packet. More advanced features like Group Adaptive Routing or Packet Distribution are not implemented.

4.7.5. @SpwRouter Reference

Properties

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @SpwRouter
new	Create new instance of SpwRouter

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

4.7.6. SpwRouter Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
internal.linkState	[int32_t; 32]	Holds the link state of the ports
ports	[temu_IfaceRef; 32]/ <unknown>	Connected SpaceWire devices.
routingTable	[uint8_t; 256]	Configure packet-address/forwarding-port mapping

Interfaces

Name	Type	Description
SpwPortIface	SpwPortIface	Input spacewire ports interfaces

Commands

Name	Description
delete	Dispose instance of SpwRouter

4.7.7. @SpwCcsdsAdapter Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @SpwCcsdsAdapter
new	Create new instance of SpwCcsdsAdapter

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

4.7.8. SpwCcsdsAdapter Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
config.ecssHeader	uint8_t	Add reserved and user application bytes (ECSS-E-ST-50-53C, option removed in TEMU 6).

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
count.Rx	uint32_t	Counter for received messages.
count.Tx	uint32_t	Counter for received messages.
enabled	uint8_t	Enable/Disable UDP. Required to change properties.
internal.linkState	int32_t	Holds the link state of the port
port	temu_IfaceRef/ <unknown>	Connected SpaceWire device.
protocolId	uint8_t	Protocol ID to be used.
rxUdpPort	uint16_t	Udp port used to receive.
targetAddr	[uint8_t; 16]	Addresses to use to forard a packet received via UDP.
targetAddrLength	uint8_t	Number of valid addresses in targetAddr array.
txHost	*char	File name to write TTY log to.
txUdpPort	uint16_t	Udp port used to send.
userApplication	uint8_t	User application byte of the CCSDS header.

Interfaces

Name	Type	Description
SpwPortIface	SpwPortIface	Input spacewire port interfaces

Commands

Name	Description
delete	Dispose instance of SpwCcsdsAdapter

4.7.9. Fault Injection

SpaceWire supports fault injection via custom *man-in-the-middle* models. These models can inject packets using events or modify packets in-flight.

For example, it is possible to construct EEP packet markers using the `teSMT_Err` message type.

The `temu_SpwPacket` type also allows for symbolic CRC errors on RMAP packets to be injected setting one of `TEMU_SPW_FLAG_RMAP_HCRC_ERROR` or `TEMU_SPW_FLAG_RMAP_DCRC_ERROR` in the `Flags` field.

Since the custom model acts as *man-in-the-middle*, it can also drop packets in transit.

4.7.10. Examples

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

This example shows how to create a simple SpaceWire Router and a Grspw2 device and connect them.

Listing 13. Creating and Connecting SpaceWire Router

```
import BusModels
import TEMUGrspw2
Grspw2.new name=grspw0
SpwRouter.new name=spwRouter
spw-connect port1=grspw0:SpwPortIface[0] port2=spwRouter:SpwPortIface[0]
```

The next example shows how to implement a simple SpaceWire device

Listing 14. SpaceWire Device Example

```
#include <stdint.h>
#include <stdio.h>
#include <string.h>

#include "temu-c/Support/Objsys.h"
#include "temu-c/Support/Attributes.h"
#include "temu-c/Support/Logging.h"
#include "temu-c/Bus/Spacewire.h"

typedef struct {
  temu_Object Super;

  int TransmitterDataRate;
  temu_SpwLinkState LinkState;
  temu_SpwPortIfaceRef Uplink;
} SpwDevice;

void*
create(const char *Name,
       int Argc TEMU_UNUSED,
       const temu_CreateArg *Argv TEMU_UNUSED)
{
  void *Obj = malloc(sizeof(SpwDevice));
  memset(Obj, 0, sizeof(SpwDevice));

  printf("Creating Object '%s'\n", Name);

  return Obj;
}

void
destroy(void *Obj)
{
  free(Obj);
```

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```
}

static void
spwDeviceChangeLinkState(SpwDevice *Device, temu_SpwLinkState LinkState)
{
  Device->LinkState = LinkState;
  if ((Device->Uplink.Iface != NULL) && (Device->Uplink.Obj != NULL)) {
      Device->Uplink.Iface->signalLinkStateChange(
        Device->Uplink.Obj, LinkState);
  }
}

////////////////////////////////////////////////////////////////////////////
// SpwPortIface 0 implementation
////////////////////////////////////////////////////////////////////////////

static void
spwPortIfaceReceive0(void *Obj, void *Sender, temu_SpwPacket *Pkt)
{
  // Handle packet received.
  SpwDevice *Dev = (SpwDevice*)(Obj);
  temu_logInfo(Dev, "Received SpaceWire packet");
}

static void
spwPortIfaceSignalLinkStateChange0(void *Obj, temu_SpwLinkState LinkState)
{
  // The other side notified us that its link state changed.
  SpwDevice *Dev = (SpwDevice*)(Obj);
  temu_logInfo(Dev, "Other side link state changed");

  // Depending on the other side link state change update this
  // device link state.
}

static temu_SpwLinkState
spwPortIfaceGetOtherSideLinkState0(void *Obj)
{
  // Other side request this device state.
  SpwDevice *Dev = (SpwDevice*)(Obj);
  return (temu_SpwLinkState)Dev->LinkState;
}

static void
spwPortIfaceConnect0(void *Obj, temu_SpwPortIfaceRef PortIf)
{
  SpwDevice *Dev = (SpwDevice*)(Obj);
  Dev->Uplink = PortIf;
```

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

```
  // When two ports are connected the device goes to ready state.
  spwDeviceChangeLinkState(Dev, teSPWLS_Ready);
}

static void
spwPortIfaceDisconnect0(void *Obj)
{
  SpwDevice *Dev = (SpwDevice*)(Obj);
  Dev->Uplink.Iface = NULL;
  Dev->Uplink.Obj = NULL;

  // When two ports are diconnected the device goes to error reset state.
  spwDeviceChangeLinkState(Dev, teSPWLS_ErrorReset);
}

static uint64_t
spwPortIfaceTimeToSendPacketNs0(void* Obj, uint64_t PacketSize)
{
  SpwDevice *Dev = (SpwDevice*)(Obj);
  // Return the time required to transmit the packet through this port.
  return PacketSize / Dev->TransmitterDataRate;
}

temu_SpwPortIface SpwPortIface0 = {
  spwPortIfaceReceive0,
  spwPortIfaceSignalLinkStateChange0,
  spwPortIfaceGetOtherSideLinkState0,
  spwPortIfaceConnect0,
  spwPortIfaceDisconnect0,
  spwPortIfaceTimeToSendPacketNs0
};

TEMU_PLUGIN_INIT
{
  temu_Class *Cls = temu_registerClass("SpwDevice", create, destroy);

  // Reference to the port interface of the other end.
  temu_addProperty(Cls, "Uplink",
                   offsetof(SpwDevice, Uplink),
                   teTY_IfaceRef,
                   1, // Number of elements (1 = scalar)
                   NULL, NULL,
                   "Other end port interface");

  // Port interface.
  temu_addInterface(Cls, "SpwPortIface", "SpwPortIface", &SpwPortIface0,
                    0, "SpaceWire port interface");
}
```

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4.8. SpaceFibre

TEMU provides support for SpaceFibre based devices. SpaceFibre is a successor to SpaceWire, and parts of the emulator infrastructure builds on top of it (e.g. RMAP command interpretation, which are encoded identically). The port interface is available in: `temu-c/Bus/SpaceFibre.h`.

SpaceFibre is a point to point bus. Two devices can be connected to each other directly. Routers can be used to connect multiple devices.

On a packet level, the biggest difference between SpaceWire and SpaceFibre is that SpaceFibre has virtual channels (up to 256 per link). The SpaceWire interface documentation goes into more detail on how routing works.

4.8.1. Interfaces

The interface `temu_SpfiPortIface` is defined in the `temu-c/Bus/SpaceFibre.h` header.

Listing 15. SpaceFibre Interface

```
typedef enum {
  teSPFILS_Illegal,
  teSPFILS_Offline,
  teSPFILS_Init,
  teSPFILS_StartUp,
  teSPFILS_Ready,
  teSPFILS_Run,
} temu_SpfiLinkState;

typedef enum {
  teSPFIFL_DataPacket = (1 << 0),
  teSPFIFL_Broadcast = (1 << 1),
  teSPFIFL_ErrorEndOfPacket = (1 << 2),
  teSPFIFL_TimeDistribution = (1 << 3),
  teSPFIFL_FlowControl = (1 << 4),
  teSPFIFL_DataCRCError = (1 << 5),
  teSPFIFL_HeaderCRCError = (1 << 6),
  teSPFIFL_SeqNumWrong = (1 << 7),
  teSPFIFL_Full = (1 << 8),
  teSPFIFL_Retry = (1 << 9),
  teSPFIFL_ACK = (1 << 10),
  teSPFIFL_NACK = (1 << 11),
  teSPFIFL_BroadcastLate = (1 << 12),
  teSPFIFL_BroadcastDelayed = (1 << 13),
} temu_SpfiFlags;

typedef struct temu_SpfiPacket {
  uint32_t Flags;
  uint8_t Channel;
  uint8_t SeqNum;
```

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```
  uint8_t Type;
  temu_Buff PktData;
} temu_SpfiPacket;

typedef struct temu_SpfiControlWord {
  uint32_t Flags;
  uint8_t Channel;
  uint8_t SeqNum;
  uint8_t Value;
} temu_SpfiControlWord;

struct temu_SpfiPortIface {
  void (*connect)(temu_Object *Dev, temu_SpfiPortIfaceRef OtherSide);
  void (*disconnect)(temu_Object *Dev);
  void (*signalLinkStateChange)(temu_Object *Dev, temu_SpfiLinkState LinkState);
  temu_SpfiLinkState (*getOtherSideLinkState)(temu_Object *Dev);
  void (*sendControlWord)(temu_Object *Dev, temu_Object *Sender,
                          temu_SpfiControlWord *ControlWord);
  void (*sendPacket)(temu_Object *Dev, temu_Object *Sender,
                     temu_SpfiPacket *Pkt);
};
```

While the SpaceFibre protocol is character based, supports multiple lanes per link, and may split packets into multiple frames for QoS, TEMU transfers full packets at a time for performance reasons. The `temu_SpfiPacket` type is used for broadcast messages as well (most often used for time codes). Control Words (such as Flow Control Tokens) are modeled in the interface and can be represented, but not used by any device model shipped as part of TEMU 5.0.0 at the moment.

The SpaceFibre packet structure is used to pass a packet between nodes. The `Flags` field will mark it as a broadcast or normal data packet. Additional flags can be present to indicate e.g. a error end of packet. Sequence numbers in SpaceFibre are assigned per virtual channel frame, and not per packet. They are only exposed in the interface to allow for error injection in the future (or by user defined devices) and currently unused. As for the SpaceWire packet, a reference-counted TEMU buffer is used to store the payload. Functions defined in `temu-c/Bus/Spacewire.h` can be used to decode RMAP commands transfered via SpaceFibre packets.

SpaceFibre links are full-duplex. A link (no matter how many lanes) is modeled by having both sides implement the `temu_SpfiPortIface` interface and holding a reference to the other side.

For link initialization, the `temu_SpfiLinkState` enum and `signalLinkStateChange` / `getOtherSideLinkState` functions are used instead of control words. Idle frames are not modeled either.

Flow Control

According to the SpaceFibre protocol, every device/link must send flow control tokens to its peer, indicating how many bytes are guaranteed to be accepted per VC. A sender should not send any data for a VC if it did not receive flow control tokens first. Flow control tokens flow from the

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receiver to the sender! This can be modeled using the interface. The `Value` field of the `temu_SpfiControlWord` structure contains the multiplier value contained in flow control tokens.



The models currently shipped with TEMU 5.0.0 do not do this! They will ignore received FTCs and never send ones out themselves.

4.8.2. Fault Injection

SpaceFibre supports fault injection via custom *man-in-the-middle* models. These models can inject packets using events or modify packets in-flight.

For example, a mismatch in the SpaceFibre control word CRC values can be emulated using the `teSPFIFL_DataCRCError` flag. The CRC value itself that is part of the SpaceFibre frame end control word is not modeled.

Since the custom model acts as *man-in-the-middle*, it can also drop packets in transit. This could then be detected by the other side based on the sequence numbers.

4.8.3. Examples

The example below shows how to use the SpaceFibre interface.



The example below sends a response without checking how many and what kind of flow control tokens have been received.

Listing 16. SpaceFibre Device Example

```
#include <stdint.h>
#include <stdio.h>
#include <string.h>
#include <assert.h>

#include "temu-c/Support/Objsys.h"
#include "temu-c/Support/Attributes.h"
#include "temu-c/Support/Logging.h"
#include "temu-c/Bus/SpaceFibre.h"

typedef struct {
  temu_Object Super;

  temu_SpwLinkState LinkState;
  temu_SpfiPortIfaceRef Uplink;
} SpfiDevice;

static void*
create(const char *Name,
       int Argc TEMU_UNUSED,
       const temu_CreateArg *Argv TEMU_UNUSED)
{
```

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```
  SpfiDevice *Dev = malloc(sizeof(SpfiDevice));
  memset(Dev, 0, sizeof(SpfiDevice));
  Dev->LinkState = teSPFILS_Offline;
  return Dev;
}

static void
destroy(void *Obj)
{
  free(Obj);
}

static void
connect(temu_Object *Obj, temu_SpfiPortIfaceRef OtherSide)
{
  SpfiDevice *Dev = (SpfiDevice*)Obj;
  Dev->Uplink = OtherSide;
}

static void
disconnect(temu_Object *Obj)
{
  SpfiDevice *Dev = (SpfiDevice*)Obj;
  Dev->Uplink = {nullptr, nullptr};
}

static void
linkStateChangeSignaled(temu_Object *Obj, temu_SpfiLinkState LinkState)
{
  SpfiDevice *Dev = (SpfiDevice*)Obj;
  if (Dev->LinkState == teSPFILS_Offline && LinkState == teSPFILS_Init) {
    Dev->LinkState = teSPFILS_Init;
  } else if (Dev->LinkState == teSPFILS_Init && LinkState == teSPFILS_StartUp) {
    Dev->LinkState = teSPFILS_StartUp;
  } else if (Dev->LinkState == teSPFILS_StartUp && LinkState == teSPFILS_Ready) {
    Dev->LinkState = teSPFILS_Ready;
  } else if (Dev->LinkState == teSPFILS_Ready && LinkState == teSPFILS_Run) {
    Dev->LinkState = teSPFILS_Run;
  } else {
    temu_logSimError(Dev, "Link state transition unhandled");
    return;
  }

  Dev->Uplink.Iface->signalLinkStateChange(Dev->Uplink.Obj, Dev->LinkState);
}

static temu_SpfiLinkState
getLinkState(temu_Object *Obj)
{
```

```
  SpfiDevice *Dev = (SpfiDevice*)Obj;
  return Dev->LinkState;
}

static void
receiveControlWord(temu_Object *Obj, temu_Object *Sender,
                   temu_SpfiControlWord *ControlWord)
{
  SpfiDevice *Dev = (SpfiDevice*)Obj;
  temu_logInfo(Dev, "Received SpaceFibre control word...");

  // Otherwise unused...
}

static void
receivePacket(temu_Object *Obj, temu_Object *Sender, temu_SpfiPacket *Pkt)
{
  SpfiDevice *Dev = (SpfiDevice*)Obj;

  // NOTE: A real model should avoid calling back into the other side directly!
  // It should use events to delay the response!
  char Buf[1024];
  size_t Len = snprintf(&Buf, sizeof(Buf),
      "Hello! I received you packet on virtual channel %d of %d bytes.",
      Pkt->Channel, temu_buffLen(&Pkt->PktData));

  temu_SpfiPacket Response = {
    .Flags = teSPFIFL_DataPacket,
    .Channel = Pkt->Channel,
    .PktData = temu_buffCreate(Len)
  };
  memcpy(temu_buffReadableData(&Response.PktData), Buf, Len);
  Dev->Uplink.Iface->sendPacket(Dev->Uplink.Obj, &Dev.Super, &Response);
  temu_buffDispose(Response.PktData);
}

TEMU_PLUGIN_INIT
{
  temu_Class *C = temu_registerClass("SpfiDevice", create, destroy);

  temu_addInterfaceReference(C, "SpfiPort", offsetof(SpfiDevice, Uplink),
                             TEMU_SPFI_PORT_IFACE_TYPE, 1, 0, nullptr, nullptr,
                             "SpaceFibre port to the other side of the link.");

  static temu_SpfiPortIface SpfiPortIface = {
    .connect = connect,
    .disconnect = disconnect,
    .signalLinkStateChange = linkStateChangeSignaled,
    .getOtherSideLinkState = getLinkState,
```

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```
    .sendControlWord = receiveControlWord,
    .receivePacket = receivePacket
  };
  temu_addInterface(C, "SpfiPortIface", TEMU_SPFI_PORT_IFACE_TYPE,
                    &SpfiPortIface, 0, "SpaceFibre port interface");
}
```

4.9. SPI

SPI device behaviour is emulated using the `temu_SpiBus2` bus model. The `temu_SpiBus` bus model has been deprecated as of TEMU 5.0.0, it should not be used for new models and existing models should be migrated to the new bus model.

4.9.1. SpiBus2Interface

Transmissions are performed through the `temu_SpiBus2Iface` interface provided by an instanced object of the bus model.

Connecting

To create a connection through an SPI bus an "SpiBus2" object needs to be instantiated. This manages the slave and master connections.

Connecting a master to the bus works as with any other model. The master is connected to the bus object's `temu_SpiBus2Iface` and stores it as a `temu_SpiBus2IfaceRef`.

Listing 17. Connecting a master via the API

```
temu_connect(spiMaster, "spiBus", spiBus, "SpiBus2Iface")
```

Listing 18. Connecting a master via Command Line

```
connect a=spiMaster.spiBus b=spiBus:SpiBus2Iface
```

For slave devices a special procedure is required. The `temu_SpiBus2Iface` provides connect and disconnect functions which register a slave device with it's corresponding chip number `chipNum`. This number is used to relate the chipSelect raising and lowering to a specific device. These should be used in favour or the typical connect functions. When connecting or disconnecting a device the slave's `connected` or `disconnected` functions will be called respectively. The slaves should use these to store the interface reference to the `temu_SpiBus2`. Minimal implementations might look like this:

```
void
connected(temu_Object *Obj, uint8_t chipNum, temu_SpiBus2IfaceRef Device)
{
  SPICTRL *spi = reinterpret_cast<SPICTRL *>(Obj);
  spi->Super.ChipNum = chipNum;
```

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```
  spi->Bus = Device;
}

void
disconnected(temu_Object *Obj, uint8_t chipNum)
{
  SPICTRL *spi = reinterpret_cast<SPICTRL *>(Obj);
  spi->Bus.Iface = nullptr;
  spi->Bus.Obj = nullptr;
}
```

Listing 19. Connecting a slave via the command line

```
connect-spi-slave slave=spidev0:SpiSlaveDevice2Iface chipNum=0 bus=spiBus:SpiBus2Iface
```

Listing 20. Connecting a slave via the API

```
// Using the API directly
auto spiBusIf = reinterpret_cast<temu_SpiBus2Iface*>(
        temu_getInterface(spiBus, "SpiBus2Iface", 0));
temu_SpiSlaveDevice2IfaceRef deviceRef = {(temu_Object *)spiDevice,
                                          &spiSlaveDevIface};
uint8_t chipNum = 0;
spiBusIf->connect(spiBus, chipNum, deviceRef);

// or Calling the connect command
temu_execCommand("connect-spi-slave slave=spidev0:SpiSlaveDevice2Iface "
                     "chipNum=0 bus=spiBus:SpiBus2Iface");
```

Modelling

SPI-Slave models should expose their chip select number as a property to allow assigning distinct numbers to all devices in accordance to the real wire layout being emulated. To simplify this a model may use a struct of type `temu_SpiSlaveDevice2` as its first data member in place of the typical temu_Object. During the registration of the model a call to `temu_spiDevice2Register` will register the property.



Most SPI slave device behaviour can be modelled nicely as a state machine starting when the chip select is raised, resetting when it is lowered and operating on each incoming character separately.

Transmitting

A transmissions starts with raising the chip select signal of a slave using the `raiseChipSelect` function of the interface. This may be done by the SPI Controller used as the bus master or through any other means such as an IO pin model which raises and lowers the chip select signal. Using the `transfer` function of the bus allows the master to initiate the transfer of data with the currently

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selected slave.

The contents of the `temu_SpiTransaction` being transferred allow for the modeling of various SPI transmission setups. When initiating the transfer the master should have filled out all relevant values in the `temu_SpiTransaction` struct. If the transmission was bi-directional the slave should immediately reply by storing the requested ammount of data into the provided buffer.

4.9.2. @SpiBus2 Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @SpiBus2
new	Create new instance of SpiBus2

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

4.9.3. SpiBus2 Reference

Properties

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ChipSelectActive	uint8_t	State of chip select signal
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
currentChipNumber	uint8_t	Last chosen chip
spiSlaveDevices	temu_IfaceRefArray	SPI slave devices

Interfaces

Name	Type	Description
SpiBus2Iface	temu::SpiBus2Iface	Bus interface.

Commands

Name	Description
delete	Dispose instance of SpiBus2

4.9.4. Limitations

Only one chip select signal may be active at the same time.

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Chapter 5. GPIO Bus



This bus model is deprecated. Users should migrate to the `SignalIface`.

The bus model maintains the values of 64 GPIO pins and a notification list, where pin updates can be forwarded to an arbitrary number of models when pin values have changed.

This does place a limitation, in that a model must know which pin it is connected to.

5.1. Configuration

The `GpioBus` model can be configured by connecting GPIO clients to the `Clients` property. No other configuration capabilities are provided.

5.2. Class Info

5.2.1. @GpioBus Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GpioBus
new	Create new instance of GpioBus

Command new Arguments

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Required	Description
name	string	yes	Name of object to create

5.2.2. GpioBus Reference

Properties

Name	Type	Description
Bits	uint64_t	
Class	*void	Class object
Clients	temu_IfaceRefArray	
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Interfaces

Name	Type	Description
GpioBusIface	GpioBusIface	

Commands

Name	Description
delete	Dispose instance of GpioBus

5.3. Limitations

Pin updates using the `GpioBusIface` will be distributed to all connected `GpioClients`.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Chapter 6. Generic Cache

TEMU supports the use of cache models. However, cache models, at least when they are non-statistical, a significant impact on performance. Therefore cache models are not normally used when running the emulator.

For the cases where a cache model is needed, the *generic cache model* can be used (see limitations for more info). The generic cache model is a highly configurable cache model and supports being used, both as Harward style caches (separate I- and D-caches) and as a unified cache.



When connecting the generic cache model in the memory hierarchy, it will intercept every memory transaction, and disable the ATC for any memory access. This means that performance is significantly impacted, especially in systems with an MMU due to forced table walks.

The cache model will handle memory accesses with the `TEMU\_MT\_CACHEABLE` flag set. This flag can be set when mapping in a device (e.g. RAM or ROM).

6.1. Configuration

6.1.1. @GenericCache Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Description
delete	Dispose instance of @GenericCache
new	Create new instance of GenericCache

Command new Arguments

Name	Type	Required	Description
dataLineSize	int	no	Data cache line size
dataSize	int	no	Data cache size
dataWays	int	no	Data cache ways
instrLineSize	int	no	Instruction cache line size
instrSize	int	no	Instruction cache size
instrWays	int	no	Instruction cache ways
lineSize	int	no	Unified cache line size
name	string	yes	Name of object to create
separate	int	no	Separate instruction and data caches
size	int	no	Unified cache size
ways	int	no	Unified cache ways
wordSize	int	no	Word size

6.1.2. GenericCache Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.

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Name	Type	Description
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
data.lineBits	uint32_t	
data.lineMask	uint32_t	
data.lineSize	uint32_t	line size in bytes
data.lineWordSizeLg2	uint32_t	log 2 of line-size in words
data.replacementPolicy	int32_t	data cache replacement policy (0=none, 1=lru, 2=lrr, 3=rnd)
data.rndReplaceWay	int32_t	
data.setBits	uint32_t	
data.setMask	uint32_t	
data.setShift	uint32_t	
data.sets	uint32_t	number of sets
data.status	uint32_t	status of data cache
data.ways	uint32_t	number of ways in the cache
dcacheCtrl	temu_IfaceRef/ <unknown>	data cache controller
fetchHits	uint64_t	
fetchMisses	uint64_t	
fetchPenalty	int32_t	
icacheCtrl	temu_IfaceRef/ <unknown>	instruction cache controller
instr.lineBits	uint32_t	
instr.lineMask	uint32_t	
instr.lineSize	uint32_t	line size in bytes
instr.lineWordSizeLg2	uint32_t	log 2 of line-size in words
instr.replacementPolicy	int32_t	instruction cache replacement policy (0=none, 1=lru, 2=lrr, 3=rnd)
instr.rndReplaceWay	int32_t	
instr.setBits	uint32_t	
instr.setMask	uint32_t	
instr.setShift	uint32_t	
instr.sets	uint32_t	number of sets

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Name	Type	Description
instr.status	uint32_t	status of instruction cache
instr.ways	uint32_t	number of ways in the cache
isSplitCache	int32_t	
isWriteAllocate	int32_t	
isWriteBack	int32_t	
postTransaction	temu_IfaceRef/ <unknown>	Post transaction interface for chaining
preTransaction	temu_IfaceRef/ <unknown>	Pre transaction interface for chaining
readHits	uint64_t	
readMisses	uint64_t	
readPenalty	int32_t	
wordSize	int32_t	
writeHits	uint64_t	
writeMisses	uint64_t	
writePenalty	int32_t	

Interfaces

Name	Type	Description
DCacheIface	temu::CacheIface	
ICacheIface	temu::CacheIface	
ObjectIface	ObjectIface	
PostAccessIface	MemAccessIface	
PreAccessIface	MemAccessIface	

Commands

Name	Description
delete	Dispose instance of GenericCache

6.1.3. Arguments

size

Unified cache size in bytes.

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instrSize

Instruction cache size in bytes.

dataSize

Data cache size in bytes.

ways

Number of ways in a unified cache (must be power of 2)

instrWays

Number of ways in instruction cache (must be power of 2)

dataWays

Number of ways in data cache (must be power of 2)

lineSize

Line size for unified cache

dataLineSize

Line size for data cache

instrLineSize

Line size for instruction cache

wordSize

Size of a word in bytes (defaults to 4)

separate

Set to 1 to turn the cache model to separate I- and D-caches. Set to 0 to make the cache a unified cache. This option affects the interpretation of the size, ways and lineSize arguments (see above).

6.1.4. Interfaces

The following interfaces can be used to connect the generic cache model:

PreAccessIface

A MemAccessIface that receives memory access events before they reach the target device.

PostAccessIface

A MemAccessIface that handles memory access events after they reach the target device.

6.1.5. Properties

The following properties are used for configuring the cache model and to connect the model in the object graph.

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preTransaction

Memory access interface reference for next pre-access handler.

postTransaction

Memory access interface reference for next post-access handler.

icacheCtrl

Optional interface reference for a instruction cache controller object.

dcacheCtrl

Optional interface reference for a data cache controller object.

instr.replacementPolicy

Replacement policy used when fetching instructions. Set to 0 = NONE (or directly mapped / 1-way set associative cache). 1 = LRU, 2 = LRR and 3 = RND. Automatically set to 0 when ways is set to 1.

data.replacementPolicy

Replacement policy used when accessing data. Set to 0 = NONE (or directly mapped / 1-way set associative cache). 1 = LRU, 2 = LRR and 3 = RND. Automatically set to 0 when ways is set to 1.

isSplitCache

Cache is split and has separate instruction and data caches.

isWriteBack

Cache is write-back cache, not supported at the moment.

isWriteAllocate

Set to non-zero to have the cache allocate a line in case of a write miss. Set to zero to avoid line allocation.

fetchPenalty

Cost for fetching from a cached line.

readPenalty

Cost for reading from a cached line.

writePenalty

Cost for writing to a cached line.

wordSize

Word size for cache (defaults to 4, do not modify unless connecting to 64-bit processor architectures).

instr.sets

Number of sets in the instruction cache.

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instr.ways

Number of ways in the instruction cache.

instr.lineSize

Instruction line size in bytes.

data.sets

Number of sets in the data cache.

data.ways

Number of ways in the data cache.

data.lineSize

Data line size in bytes.

6.2. Properties

The generic cache model contains the following counters that can be inspected to get an idea of hit and miss-rates.

fetchHits

Number of cache hits when fetching instructions.

fetchMisses

Number of cache misses when fetching instructions.

readHits

Number of cache hits when reading data.

readMisses

Number of cache misses when reading data.

writeHits

Number of cache hits when writing data.

writeMisses

Number of cache misses when writing data.

6.3. Limitations

- The cache does not emulate write-back penalties for write-back caches at present. This means that the evict functions will behave as the invalidate functions.
- Number of ways must be a power of 2. That means that 1- 2- and 4- way set associative caches are fine, but 3-way set associative caches are not emulated by the generic cache model.

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Chapter 7. LEON2 SoC

The Leon2SoC class implements a model of the LEON2 on chip devices (i.e. memory controller, interrupt controller, UARTs and timers). The model must be combined with a LEON2 CPU to be really useful.

7.1. Loading the Plugin

```
import Leon2SoC
```

7.2. Configuration

7.2.1. Interrupt Delivery

Set the irqControl property to point out the processor's irq interface. The model will deliver normal SPARC interrupts (1 up to 15). The LEON2 also exports the IrqCtrlIface as IrqIface. IrqClientIface should be wired from the CPU the LEON2 model is connected to.

The IrqIface enables the use of external interrupts using the raise and lower functions. The LEON2 has 8 external IRQs mapped according to the following table (the mappings cannot be customised at present):

Table 1. External to Internal IRQ Mapping

External	Internal (Sparc IRL)
0	4
1	5
2	6
3	7
4	10
5	12
6	13
7	15

The rules for IRQ raising is controlled by the GPIO IRQ config registers (it is also possible to raise IRQs by setting and lowering GPIO pins).

7.2.2. UART Connections

The UARTs are connected to the destination using the uarta and uartb properties. For the remote end points, these should be connected to UartAIface and UartBIface.

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7.2.3. Infinite UART Speed

The UARTs can run either at infinite speed, or at simulated real-time speed. This can be configured using the infiniteUartSpeed property. Set this property to non-zero to enable infinite UART speed.

Note that this controls the speed of both UARTs.

When infinite speed is enabled, bytes are emitted to the destination serial device as soon as they have been written by the OBSW.

7.2.4. GPIO

The GPIO support in the LEON2 model supports interrupt generation using the GPIO interface instead of the IRQ controller interface. Model implements both the GpioClientIface and a property with a GpioBusIface reference (called gpioBus). The GPIO bus connection is not mandatory to set. If it is set, writes to the GPIO data register's out bits will be forwarded over the GPIO port. Note that the LEON2 only have 16 GPIO pins.

Both the legacy multipin GpioBusIface and the new single pin SignalIface are supported. The model will prioritise the legacy interface for backwards compatibility. If you wish to use the SignalIface interface you should not set the gpioBus property.

7.2.5. Caches

The LEON2 SoC can act as a cache controller. That means that a cache model can notify the SoC about when it starts an evict/flush operation. The controller will also notify any connected caches about enabling, disabling and freezing events happening.

The cache parameters in the cache control register and the product configuration register are set automatically when connecting the dCache and iCache interface references to conforming objects.



When connecting the cache references, make sure the caches are configured before they are connected.

The caches that these interface references are connected to should normally be compliant with the supported LEON2 cache parameters. That is, there is a limitation on the sizes, lines and ways.

While the model does a best effort in trying to report errors when a miss-configured cache model is supplied, take care to ensure that the model is correctly configured.

7.2.6. @Leon2SoC Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component

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Name	Type	Description
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @Leon2SoC
new	Create new instance of Leon2SoC

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

7.2.7. Leon2SoC Reference

Properties

Name	Type	Description
CCRColdResetValue	uint32_t	Cache Control Register
CCRForcedBits	uint32_t	Cache Control Register
CCRForcedFlippedBits	uint32_t	Cache Control Register
CCRReadMask	uint32_t	Cache Control Register
CCRResetMask	uint32_t	Cache Control Register
CCRResetValue	uint32_t	Cache Control Register
CCRWriteMask	uint32_t	Cache Control Register
Class	*void	Class object

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Name	Type	Description
Component	*void	Pointer to component object if part of component
FAILARColdResetValue	uint32_t	Fail Address Register
FAILARForcedBits	uint32_t	Fail Address Register
FAILARForcedFlippedBits	uint32_t	Fail Address Register
FAILARReadMask	uint32_t	Fail Address Register
FAILARResetMask	uint32_t	Fail Address Register
FAILARResetValue	uint32_t	Fail Address Register
FAILARWriteMask	uint32_t	Fail Address Register
FAILSRColdResetValue	uint32_t	Fail Status Register
FAILSRForcedBits	uint32_t	Fail Status Register
FAILSRForcedFlippedBits	uint32_t	Fail Status Register
FAILSRReadMask	uint32_t	Fail Status Register
FAILSRResetMask	uint32_t	Fail Status Register
FAILSRResetValue	uint32_t	Fail Status Register
FAILSRWriteMask	uint32_t	Fail Status Register
IDLEColdResetValue	uint32_t	Idle Register
IDLEForcedBits	uint32_t	Idle Register
IDLEForcedFlippedBits	uint32_t	Idle Register
IDLEReadMask	uint32_t	Idle Register
IDLEResetMask	uint32_t	Idle Register
IDLEResetValue	uint32_t	Idle Register
IDLEWriteMask	uint32_t	Idle Register
IODATColdResetValue	uint32_t	I/O Port Data Register
IODATForcedBits	uint32_t	I/O Port Data Register
IODATForcedFlippedBits	uint32_t	I/O Port Data Register
IODATReadMask	uint32_t	I/O Port Data Register
IODATResetMask	uint32_t	I/O Port Data Register
IODATResetValue	uint32_t	I/O Port Data Register
IODATWriteMask	uint32_t	I/O Port Data Register
IODIRColdResetValue	uint32_t	I/O Port Direction Register
IODIRForcedBits	uint32_t	I/O Port Direction Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
IODIRForcedFlippedBits	uint32_t	I/O Port Direction Register
IODIRReadMask	uint32_t	I/O Port Direction Register
IODIRResetMask	uint32_t	I/O Port Direction Register
IODIRResetValue	uint32_t	I/O Port Direction Register
IODIRWriteMask	uint32_t	I/O Port Direction Register
IOIT1ColdResetValue	uint32_t	I/O Port Interrupt Register 1
IOIT1ForcedBits	uint32_t	I/O Port Interrupt Register 1
IOIT1ForcedFlippedBits	uint32_t	I/O Port Interrupt Register 1
IOIT1ReadMask	uint32_t	I/O Port Interrupt Register 1
IOIT1ResetMask	uint32_t	I/O Port Interrupt Register 1
IOIT1ResetValue	uint32_t	I/O Port Interrupt Register 1
IOIT1WriteMask	uint32_t	I/O Port Interrupt Register 1
IOIT2ColdResetValue	uint32_t	I/O Port Interrupt Register 2
IOIT2ForcedBits	uint32_t	I/O Port Interrupt Register 2
IOIT2ForcedFlippedBits	uint32_t	I/O Port Interrupt Register 2
IOIT2ReadMask	uint32_t	I/O Port Interrupt Register 2
IOIT2ResetMask	uint32_t	I/O Port Interrupt Register 2
IOIT2ResetValue	uint32_t	I/O Port Interrupt Register 2
IOIT2WriteMask	uint32_t	I/O Port Interrupt Register 2
ITCColdResetValue	uint32_t	Interrupt Clear Register
ITCForcedBits	uint32_t	Interrupt Clear Register
ITCForcedFlippedBits	uint32_t	Interrupt Clear Register
ITCReadMask	uint32_t	Interrupt Clear Register
ITCResetMask	uint32_t	Interrupt Clear Register
ITCResetValue	uint32_t	Interrupt Clear Register
ITCWriteMask	uint32_t	Interrupt Clear Register
ITFColdResetValue	uint32_t	Interrupt Force Register
ITFForcedBits	uint32_t	Interrupt Force Register
ITFForcedFlippedBits	uint32_t	Interrupt Force Register
ITFReadMask	uint32_t	Interrupt Force Register
ITFResetMask	uint32_t	Interrupt Force Register
ITFResetValue	uint32_t	Interrupt Force Register

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Name	Type	Description
ITFWriteMask	uint32_t	Interrupt Force Register
ITMPColdResetValue	uint32_t	Interrupt Mask and Priority Register
ITMPForcedBits	uint32_t	Interrupt Mask and Priority Register
ITMPForcedFlippedBits	uint32_t	Interrupt Mask and Priority Register
ITMPReadMask	uint32_t	Interrupt Mask and Priority Register
ITMPResetMask	uint32_t	Interrupt Mask and Priority Register
ITMPResetValue	uint32_t	Interrupt Mask and Priority Register
ITMPWriteMask	uint32_t	Interrupt Mask and Priority Register
ITPColdResetValue	uint32_t	Interrupt Pending Register
ITPForcedBits	uint32_t	Interrupt Pending Register
ITPForcedFlippedBits	uint32_t	Interrupt Pending Register
ITPReadMask	uint32_t	Interrupt Pending Register
ITPResetMask	uint32_t	Interrupt Pending Register
ITPResetValue	uint32_t	Interrupt Pending Register
ITPWriteMask	uint32_t	Interrupt Pending Register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
MCFG1ColdResetValue	uint32_t	Memory Configuration Register 1
MCFG1ForcedBits	uint32_t	Memory Configuration Register 1
MCFG1ForcedFlippedBits	uint32_t	Memory Configuration Register 1
MCFG1ReadMask	uint32_t	Memory Configuration Register 1

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Name	Type	Description
MCFG1ResetMask	uint32_t	Memory Configuration Register 1
MCFG1ResetValue	uint32_t	Memory Configuration Register 1
MCFG1WriteMask	uint32_t	Memory Configuration Register 1
MCFG2ColdResetValue	uint32_t	Memory Configuration Register 2
MCFG2ForcedBits	uint32_t	Memory Configuration Register 2
MCFG2ForcedFlippedBits	uint32_t	Memory Configuration Register 2
MCFG2ReadMask	uint32_t	Memory Configuration Register 2
MCFG2ResetMask	uint32_t	Memory Configuration Register 2
MCFG2ResetValue	uint32_t	Memory Configuration Register 2
MCFG2WriteMask	uint32_t	Memory Configuration Register 2
MCFG3ColdResetValue	uint32_t	Memory Configuration Register 3
MCFG3ForcedBits	uint32_t	Memory Configuration Register 3
MCFG3ForcedFlippedBits	uint32_t	Memory Configuration Register 3
MCFG3ReadMask	uint32_t	Memory Configuration Register 3
MCFG3ResetMask	uint32_t	Memory Configuration Register 3
MCFG3ResetValue	uint32_t	Memory Configuration Register 3
MCFG3WriteMask	uint32_t	Memory Configuration Register 3
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
PCRColdResetValue	uint32_t	Product Configuration Register

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Name	Type	Description
PCRForcedBits	uint32_t	Product Configuration Register
PCRForcedFlippedBits	uint32_t	Product Configuration Register
PCRReadMask	uint32_t	Product Configuration Register
PCRResetMask	uint32_t	Product Configuration Register
PCRResetValue	uint32_t	Product Configuration Register
PCRWriteMask	uint32_t	Product Configuration Register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
SCACColdResetValue	uint32_t	Prescaler Counter Register
SCACForcedBits	uint32_t	Prescaler Counter Register
SCACForcedFlippedBits	uint32_t	Prescaler Counter Register
SCACReadMask	uint32_t	Prescaler Counter Register
SCACResetMask	uint32_t	Prescaler Counter Register
SCACResetValue	uint32_t	Prescaler Counter Register
SCACWriteMask	uint32_t	Prescaler Counter Register
SCARColdResetValue	uint32_t	Prescaler Reload Register
SCARForcedBits	uint32_t	Prescaler Reload Register
SCARForcedFlippedBits	uint32_t	Prescaler Reload Register
SCARReadMask	uint32_t	Prescaler Reload Register
SCARResetMask	uint32_t	Prescaler Reload Register
SCARResetValue	uint32_t	Prescaler Reload Register
SCARWriteMask	uint32_t	Prescaler Reload Register
TIMC1ColdResetValue	uint32_t	Timer 1 Counter Register
TIMC1ForcedBits	uint32_t	Timer 1 Counter Register
TIMC1ForcedFlippedBits	uint32_t	Timer 1 Counter Register
TIMC1ReadMask	uint32_t	Timer 1 Counter Register
TIMC1ResetMask	uint32_t	Timer 1 Counter Register
TIMC1ResetValue	uint32_t	Timer 1 Counter Register
TIMC1WriteMask	uint32_t	Timer 1 Counter Register
TIMC2ColdResetValue	uint32_t	Timer 2 Counter Register
TIMC2ForcedBits	uint32_t	Timer 2 Counter Register
TIMC2ForcedFlippedBits	uint32_t	Timer 2 Counter Register

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Name	Type	Description
TIMC2ReadMask	uint32_t	Timer 2 Counter Register
TIMC2ResetMask	uint32_t	Timer 2 Counter Register
TIMC2ResetValue	uint32_t	Timer 2 Counter Register
TIMC2WriteMask	uint32_t	Timer 2 Counter Register
TIMCTR1ColdResetValue	uint32_t	Timer 1 Control Register
TIMCTR1ForcedBits	uint32_t	Timer 1 Control Register
TIMCTR1ForcedFlippedBits	uint32_t	Timer 1 Control Register
TIMCTR1ReadMask	uint32_t	Timer 1 Control Register
TIMCTR1ResetMask	uint32_t	Timer 1 Control Register
TIMCTR1ResetValue	uint32_t	Timer 1 Control Register
TIMCTR1WriteMask	uint32_t	Timer 1 Control Register
TIMCTR2ColdResetValue	uint32_t	Timer 2 Control Register
TIMCTR2ForcedBits	uint32_t	Timer 2 Control Register
TIMCTR2ForcedFlippedBits	uint32_t	Timer 2 Control Register
TIMCTR2ReadMask	uint32_t	Timer 2 Control Register
TIMCTR2ResetMask	uint32_t	Timer 2 Control Register
TIMCTR2ResetValue	uint32_t	Timer 2 Control Register
TIMCTR2WriteMask	uint32_t	Timer 2 Control Register
TIMR1ColdResetValue	uint32_t	Timer 1 Reload Register
TIMR1ForcedBits	uint32_t	Timer 1 Reload Register
TIMR1ForcedFlippedBits	uint32_t	Timer 1 Reload Register
TIMR1ReadMask	uint32_t	Timer 1 Reload Register
TIMR1ResetMask	uint32_t	Timer 1 Reload Register
TIMR1ResetValue	uint32_t	Timer 1 Reload Register
TIMR1WriteMask	uint32_t	Timer 1 Reload Register
TIMR2ColdResetValue	uint32_t	Timer 2 Reload Register
TIMR2ForcedBits	uint32_t	Timer 2 Reload Register
TIMR2ForcedFlippedBits	uint32_t	Timer 2 Reload Register
TIMR2ReadMask	uint32_t	Timer 2 Reload Register
TIMR2ResetMask	uint32_t	Timer 2 Reload Register
TIMR2ResetValue	uint32_t	Timer 2 Reload Register
TIMR2WriteMask	uint32_t	Timer 2 Reload Register

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Name	Type	Description
TimeSource	*void	Time source object
UAC1ColdResetValue	uint32_t	UART 1 Control Register
UAC1ForcedBits	uint32_t	UART 1 Control Register
UAC1ForcedFlippedBits	uint32_t	UART 1 Control Register
UAC1ReadMask	uint32_t	UART 1 Control Register
UAC1ResetMask	uint32_t	UART 1 Control Register
UAC1ResetValue	uint32_t	UART 1 Control Register
UAC1WriteMask	uint32_t	UART 1 Control Register
UAC2ColdResetValue	uint32_t	UART 2 Control Register
UAC2ForcedBits	uint32_t	UART 2 Control Register
UAC2ForcedFlippedBits	uint32_t	UART 2 Control Register
UAC2ReadMask	uint32_t	UART 2 Control Register
UAC2ResetMask	uint32_t	UART 2 Control Register
UAC2ResetValue	uint32_t	UART 2 Control Register
UAC2WriteMask	uint32_t	UART 2 Control Register
UAD1ColdResetValue	uint32_t	UART 1 Data Register
UAD1ForcedBits	uint32_t	UART 1 Data Register
UAD1ForcedFlippedBits	uint32_t	UART 1 Data Register
UAD1ReadMask	uint32_t	UART 1 Data Register
UAD1ResetMask	uint32_t	UART 1 Data Register
UAD1ResetValue	uint32_t	UART 1 Data Register
UAD1WriteMask	uint32_t	UART 1 Data Register
UAD2ColdResetValue	uint32_t	UART 2 Data Register
UAD2ForcedBits	uint32_t	UART 2 Data Register
UAD2ForcedFlippedBits	uint32_t	UART 2 Data Register
UAD2ReadMask	uint32_t	UART 2 Data Register
UAD2ResetMask	uint32_t	UART 2 Data Register
UAD2ResetValue	uint32_t	UART 2 Data Register
UAD2WriteMask	uint32_t	UART 2 Data Register
UAS1ColdResetValue	uint32_t	UART 1 Status Register
UAS1ForcedBits	uint32_t	UART 1 Status Register
UAS1ForcedFlippedBits	uint32_t	UART 1 Status Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
UAS1ReadMask	uint32_t	UART 1 Status Register
UAS1ResetMask	uint32_t	UART 1 Status Register
UAS1ResetValue	uint32_t	UART 1 Status Register
UAS1WriteMask	uint32_t	UART 1 Status Register
UAS2ColdResetValue	uint32_t	UART 2 Status Register
UAS2ForcedBits	uint32_t	UART 2 Status Register
UAS2ForcedFlippedBits	uint32_t	UART 2 Status Register
UAS2ReadMask	uint32_t	UART 2 Status Register
UAS2ResetMask	uint32_t	UART 2 Status Register
UAS2ResetValue	uint32_t	UART 2 Status Register
UAS2WriteMask	uint32_t	UART 2 Status Register
UASCA1ColdResetValue	uint32_t	UART 1 Scaler Register
UASCA1ForcedBits	uint32_t	UART 1 Scaler Register
UASCA1ForcedFlippedBits	uint32_t	UART 1 Scaler Register
UASCA1ReadMask	uint32_t	UART 1 Scaler Register
UASCA1ResetMask	uint32_t	UART 1 Scaler Register
UASCA1ResetValue	uint32_t	UART 1 Scaler Register
UASCA1WriteMask	uint32_t	UART 1 Scaler Register
UASCA2ColdResetValue	uint32_t	UART 2 Scaler Register
UASCA2ForcedBits	uint32_t	UART 2 Scaler Register
UASCA2ForcedFlippedBits	uint32_t	UART 2 Scaler Register
UASCA2ReadMask	uint32_t	UART 2 Scaler Register
UASCA2ResetMask	uint32_t	UART 2 Scaler Register
UASCA2ResetValue	uint32_t	UART 2 Scaler Register
UASCA2WriteMask	uint32_t	UART 2 Scaler Register
WDGColdResetValue	uint32_t	Watchdog Register
WDGForcedBits	uint32_t	Watchdog Register
WDGForcedFlippedBits	uint32_t	Watchdog Register
WDGReadMask	uint32_t	Watchdog Register
WDGResetMask	uint32_t	Watchdog Register
WDGResetValue	uint32_t	Watchdog Register
WDGWriteMask	uint32_t	Watchdog Register

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Name	Type	Description
WPR1ColdResetValue	uint32_t	Write Protection Register 1
WPR1ForcedBits	uint32_t	Write Protection Register 1
WPR1ForcedFlippedBits	uint32_t	Write Protection Register 1
WPR1ReadMask	uint32_t	Write Protection Register 1
WPR1ResetMask	uint32_t	Write Protection Register 1
WPR1ResetValue	uint32_t	Write Protection Register 1
WPR1WriteMask	uint32_t	Write Protection Register 1
WPR2ColdResetValue	uint32_t	Write Protection Register 2
WPR2ForcedBits	uint32_t	Write Protection Register 2
WPR2ForcedFlippedBits	uint32_t	Write Protection Register 2
WPR2ReadMask	uint32_t	Write Protection Register 2
WPR2ResetMask	uint32_t	Write Protection Register 2
WPR2ResetValue	uint32_t	Write Protection Register 2
WPR2WriteMask	uint32_t	Write Protection Register 2
WPSTA1ColdResetValue	uint32_t	Write Protection Start Address 1
WPSTA1ForcedBits	uint32_t	Write Protection Start Address 1
WPSTA1ForcedFlippedBits	uint32_t	Write Protection Start Address 1
WPSTA1ReadMask	uint32_t	Write Protection Start Address 1
WPSTA1ResetMask	uint32_t	Write Protection Start Address 1
WPSTA1ResetValue	uint32_t	Write Protection Start Address 1
WPSTA1WriteMask	uint32_t	Write Protection Start Address 1
WPSTA2ColdResetValue	uint32_t	Write Protection Start Address 2
WPSTA2ForcedBits	uint32_t	Write Protection Start Address 2
WPSTA2ForcedFlippedBits	uint32_t	Write Protection Start Address 2
WPSTA2ReadMask	uint32_t	Write Protection Start Address 2
WPSTA2ResetMask	uint32_t	Write Protection Start Address 2
WPSTA2ResetValue	uint32_t	Write Protection Start Address 2
WPSTA2WriteMask	uint32_t	Write Protection Start Address 2
WPSTO1ColdResetValue	uint32_t	Write Protection End Address 1
WPSTO1ForcedBits	uint32_t	Write Protection End Address 1
WPSTO1ForcedFlippedBits	uint32_t	Write Protection End Address 1
WPSTO1ReadMask	uint32_t	Write Protection End Address 1

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Name	Type	Description
WPSTO1ResetMask	uint32_t	Write Protection End Address 1
WPSTO1ResetValue	uint32_t	Write Protection End Address 1
WPSTO1WriteMask	uint32_t	Write Protection End Address 1
WPSTO2ColdResetValue	uint32_t	Write Protection End Address 2
WPSTO2ForcedBits	uint32_t	Write Protection End Address 2
WPSTO2ForcedFlippedBits	uint32_t	Write Protection End Address 2
WPSTO2ReadMask	uint32_t	Write Protection End Address 2
WPSTO2ResetMask	uint32_t	Write Protection End Address 2
WPSTO2ResetValue	uint32_t	Write Protection End Address 2
WPSTO2WriteMask	uint32_t	Write Protection End Address 2
ahbfailaddr	uint32_t	Fail Address Register
ahbstat	uint32_t	Fail Status Register
behaviour	uint8_t	Set to 1 for COLE mode
cachectrl	uint32_t	Cache Control Register
config.levelMask	uint32_t	Level triggered internal interrupts (mask)
config.logInterrupts	uint8_t	Enable interrupt logging
cpu	temu_IfaceRef/ <unknown>	CPU to control with powerdown
dCache	temu_IfaceRef/ <unknown>	Data cache (optional)
gpioBus	temu_IfaceRef/ <unknown>	GPIO bus (deprecated, use signal interface instead)
gpioIrqLevel	uint32_t	
gpioIrqMask	uint32_t	
gpioIrqPolarity	uint32_t	
gpiodir	uint32_t	I/O Port Direction Register
gpioinout	uint32_t	I/O Port Data Register
gpioirqcfg	uint32_t	I/O Port Interrupt Register 1
gpioirqcfg2	uint32_t	I/O Port Interrupt Register 2
iCache	temu_IfaceRef/ <unknown>	Instruction cache (optional)
infiniteUartSpeed	uint32_t	
inputBits	uint32_t	Input signals
irqControl	temu_IfaceRef/ <unknown>	Next level IRQ controller object (e.g. CPU)

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Name	Type	Description
irqSignalStatus	uint16_t	Interrupt signal status (should be the same as pending in CPU)
irqclear	uint32_t	Interrupt Clear Register
irqforce	uint32_t	Interrupt Force Register
irqmask	uint32_t	Interrupt Mask and Priority Register
irqpend	uint32_t	Interrupt Pending Register
leoncfg	uint32_t	Product Configuration Register
memcfg1	uint32_t	Memory Configuration Register 1
memcfg2	uint32_t	Memory Configuration Register 2
memcfg3	uint32_t	Memory Configuration Register 3
memcfg4	uint32_t	Memory configuration 4 (COLE)
memcfg5	uint32_t	Memory configuration 5 (COLE)
mr	uint32_t	Map register (COLE)
outSignals	[temu_IfaceRef; 16]/ <unknown>	Outgoing GPIO signals
powerdown	uint32_t	Idle Register
presccntr	uint32_t	Prescaler Counter Register
prescrld	uint32_t	Prescaler Reload Register
timer1cntr	uint32_t	Timer 1 Counter Register
timer1ctrl	uint32_t	Timer 1 Control Register
timer1rld	uint32_t	Timer 1 Reload Register
timer2cntr	uint32_t	Timer 2 Counter Register
timer2ctrl	uint32_t	Timer 2 Control Register
timer2rld	uint32_t	Timer 2 Reload Register
uart1ctrl	uint32_t	UART 1 Control Register
uart1datrx	uint32_t	UART 1 Data Register
uart1scal	uint32_t	UART 1 Scaler Register
uart1stat	uint32_t	UART 1 Status Register
uart2ctrl	uint32_t	UART 2 Control Register
uart2datrx	uint32_t	UART 2 Data Register

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Name	Type	Description
uart2scal	uint32_t	UART 2 Scaler Register
uart2stat	uint32_t	UART 2 Status Register
uarta	temu_IfaceRef/ <unknown>	Serial port A
uartb	temu_IfaceRef/ <unknown>	Serial port B
watchdog	uint32_t	Watchdog Register
writeprot1	uint32_t	Write Protection Register 1
writeprot2	uint32_t	Write Protection Register 2
writeprotstart1	uint32_t	Write Protection Start Address 1
writeprotstart2	uint32_t	Write Protection Start Address 2
writeprotstop1	uint32_t	Write Protection End Address 1
writeprotstop2	uint32_t	Write Protection End Address 2

Interfaces

Name	Type	Description
DCacheCtrlIface	temu::CacheCtrlIface	D-cache to control
DeviceIface	DeviceIface	
GpioClientIface	GpioClientIface	
ICacheCtrlIface	temu::CacheCtrlIface	I-cache to control
InternalIrqIface	IrqCtrlIface	Internal IRQ controller (native LEON numbering), post your IRQs here.
IrqClientIface	IrqClientIface	IRQ acknowledgement (from CPU)
IrqIface	IrqCtrlIface	External IRQ controller, post your IRQs here.
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	
SignalIface	SignalIface	Incomming signals
UartAIface	SerialIface	UART A
UartBIface	SerialIface	UART B

Ports

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Prop	Iface	Description
irqControl	IrqClientIface	Interrupt
uarta	UartAIface	uart a
uartb	UartBIface	uart b

Registers



Register support is currently experimental!

Register Bank Regs

Register MCFG1

Description

Memory Configuration Register 1

Reset value

0x000000ff

Warm reset mask

0x7ef80bff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	pbrdy	abrdy	iowdh		iobrdy	bexc	-	iows				ioen	-							prwen	-	prwdh		prwws				prrws			
-	rw	rw	rw		rw	rw	-	rw				rw	-							rw	-	rw		rw				rw			
-	0	0	0		0	0	-	0				0	-							0	-	0		15				15			

Field	Mask	Reset	Description
pbrdy	0x40000000	0x0	PROM area bus-ready enable
abrdy	0x20000000	0x0	Asynchronous bus ready
iowdh	0x18000000	0x0	I/O bus width
iobrdy	0x04000000	0x0	I/O area bus ready enable
bexc	0x02000000	0x0	Bus error enable for RAM, PROM and I/O access
iows	0x00f00000	0x0	I/O waitstates
ioen	0x00080000	0x0	I/O area enable
prwen	0x00000800	0x0	PROM write enable
prwdh	0x00000300	0x0	PROM width
prwws	0x000000f0	0xf	PROM write waitstates
prrws	0x0000000f	0xf	PROM read waitstates

Register MCFG2

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Description

Memory Configuration Register 2

Reset value

0x7c400000

Warm reset mask

0xfff87eff

31	30	29 28 27	26	25 24 23	22 21	20 19	18 17 16 15	14	13	12 11 10 9	8	7	6	5 4	3 2	1 0
sdrref	trp	trfc	sdrcas	sdrbs	sdrcls	sdrcmd	-	se	si	rambs	-	rambrdy	ramrmw	ramwdh	ramwws	ramrws
rw	rw	rw	rw	rw	rw	rw	-	rw	rw	rw	-	rw	rw	rw	rw	rw
0	1	7	1	0	2	0	-	0	0	0	-	0	0	0	0	0

Field	Mask	Reset	Description
sdrref	0x80000000	0x0	SDRAM refresh
trp	0x40000000	0x1	SDRAM tRP timing
trfc	0x38000000	0x7	SDRAM tRFC timing
sdrcas	0x04000000	0x1	SDRAM CAS delay
sdrbs	0x03800000	0x0	SDRAM bank size
sdrcls	0x00600000	0x2	SDRAM column size
sdrcmd	0x00180000	0x0	SDRAM command
se	0x00004000	0x0	SDRAM enable
si	0x00002000	0x0	SRAM disable
rambs	0x00001e00	0x0	SRAM bank size
rambrdy	0x00000080	0x0	SRAM area bus ready enable
ramrmw	0x00000040	0x0	Read-modify-write on the SRAM
ramwdh	0x00000030	0x0	SRAM bus width
ramwws	0x0000000c	0x0	SRAM write waitstates
ramrws	0x00000003	0x0	SRAM read waitstates

Register MCFG3

Description

Memory Configuration Register 3

Reset value

0xc8000000

Warm reset mask

0xc8000c00

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rfc			-	me	srcrv															wb	rb	re	pe	tcb							
ro			-	ro	rw															rw	rw	rw	rw	rw							
3			-	1	-															0	0	-	-	-							

Field	Mask	Reset	Description
rfc	0xc0000000	0x3	Register file check bits
me	0x08000000	0x1	Memory EDAC
srcrv	0x07fff000	-	SDRAM refresh counter reload value
wb	0x00000800	0x0	EDAC diagnostic write bypass
rb	0x00000400	0x0	EDAC diagnostic read
re	0x00000200	-	RAM EDAC enable
pe	0x00000100	-	PROM EDAC enable
tcb	0x000000ff	-	Test checkbits

Register FAILAR

Description

Fail Address Register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
hea																															
rw																															
-																															

Field	Mask	Reset	Description
hea	0xffffffff	-	Hardware error address

Register FAILSR

Description

Fail Status Register

Reset value

0x00000000

Warm reset mask

0x00000100

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																						eed	hed	het	hem				hes		
-																						rw	rw	rw	rw				rw		
-																						-	0	-	-				-		

Field	Mask	Reset	Description
eed	0x00000200	-	EDAC-correctable error detected
hed	0x00000100	0x0	Hardware error detected
het	0x00000080	-	Hardware error type
hem	0x00000078	-	Hardware error module
hes	0x00000007	-	Hardware error size

Register CCR

Description

Cache Control Register

Reset value

0xfd100000

Warm reset mask

0xff99c00f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
drepl		irepl		isets		dsets		ds	fd	fi	cpc		cptb		ib	ip	dp	ite		ide		dte		dde		df	if	dcs		ics	
ro		ro		ro		ro		rw	wo	wo	ro		rw		rw	ro	ro	rw		rw		rw		rw		rw	rw	rw		rw	
3		3		3		1		0	-	-	2		-		0	0	0	-		-		-		-		-	-	0		0	

Field	Mask	Reset	Description
drepl	0xc0000000	0x3	Data cache replacement policy
irepl	0x30000000	0x3	Instruction cache replacement policy
isets	0x0c000000	0x3	Instruction cache associativity
dsets	0x03000000	0x1	Data cache associativity
ds	0x00800000	0x0	Data cache snoop enable
fd	0x00400000	-	Flush data cache
fi	0x00200000	-	Flush instruction cache
cpc	0x00180000	0x2	Cache parity bits
cptb	0x00060000	-	Cache parity test bits
ib	0x00010000	0x0	Instruction burst fetch
ip	0x00008000	0x0	Instruction cache flush pending
dp	0x00004000	0x0	Data cache flush pending
ite	0x00003000	-	Instruction cache tag error counter

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Field	Mask	Reset	Description
ide	0x00000c00	-	Instruction cache data error counter
dte	0x00000300	-	Data cache tag error counter
dde	0x000000c0	-	Data cache data error counter
df	0x00000020	-	Data cache freeze on interrupt
if	0x00000010	-	Instruction cache freeze on interrupt
dcs	0x0000000c	0x0	Data cache state
ics	0x00000003	0x0	Instruction cache state

Register IDLE

Description

Idle Register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
idle																															
wo																															
-																															

Field	Mask	Reset	Description
idle	0xffffffff	-	Idle mode trigger

Register WPR1

Description

Write Protection Register 1

Reset value

0x00000000

Warm reset mask

0x80000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
en	bp	tag															mask														
rw	rw	rw															rw														
0	-	-															-														

Field	Mask	Reset	Description
en	0x80000000	0x0	Enable

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Field	Mask	Reset	Description
bp	0x40000000	-	Block protect
tag	0x3fff8000	-	Address tag
mask	0x00007fff	-	Address mask

Register WPR2

Description

Write Protection Register 2

Reset value

0x00000000

Warm reset mask

0x80000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
en	bp	tag															mask														
rw	rw	rw															rw														
0	-	-															-														

Field	Mask	Reset	Description
en	0x80000000	0x0	Enable
bp	0x40000000	-	Block protect
tag	0x3fff8000	-	Address tag
mask	0x00007fff	-	Address mask

Register PCR

Description

Product Configuration Register

Reset value

0x7077bbd5

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
mmu	dsu	drctr	wtpnt			imac	nwin					icsz			ilsz		dcsz			dlsz		divins	mulins	wdog	memstat		fpu		pci		wprt
ro	ro	ro	ro			ro	ro					ro			ro		ro			ro		ro	ro	ro	ro		ro		ro		ro
0	1	1	4			0	7					3			3		3			2		1	1	1	1		1		1		1

Field	Mask	Reset	Description
mmu	0x80000000	0x0	Memory management unit
dsu	0x40000000	0x1	Debug support unit

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Field	Mask	Reset	Description
sdrctrl	0x20000000	0x1	SDRAM controller
wtpnt	0x1c000000	0x4	IU watchpoints
imac	0x02000000	0x0	UMAC/SMAC instructions
nwin	0x01f00000	0x7	IU register file windows
icsz	0x000e0000	0x3	Instruction cache set size
ilsz	0x00018000	0x3	Instruction cache line size
dcsz	0x00007000	0x3	Data cache set size
dlsz	0x00000c00	0x2	Data cache line size
divinst	0x00000200	0x1	UDIV/SDIV instructions
mulinst	0x00000100	0x1	UMUL/SMUL instructions
wdog	0x00000080	0x1	Watchdog
memstat	0x00000040	0x1	Memory status and address failing register
fpu	0x00000030	0x1	FPU type
pci	0x0000000c	0x1	PCI core type
wprt	0x00000003	0x1	Write protection

Register TIMC1

Description

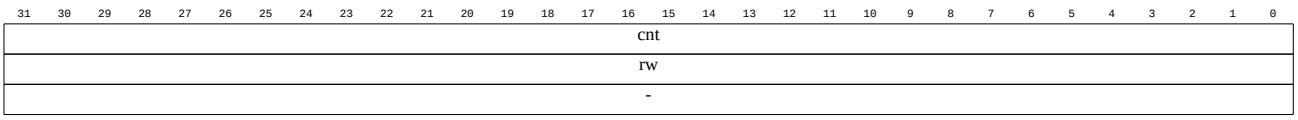
Timer 1 Counter Register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
cnt	0xffffffff	-	Timer 1 counter value

Register TIMR1

Description

Timer 1 Reload Register

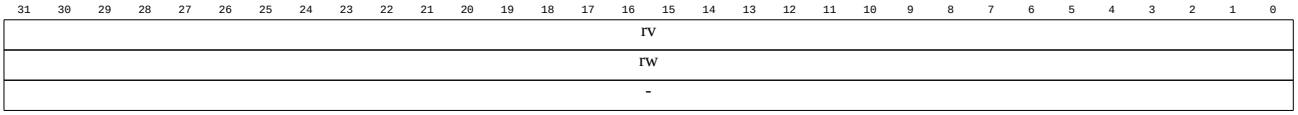
The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
rv	0xffffffff	-	Timer 1 reload value

Register TIMCTR1

Description

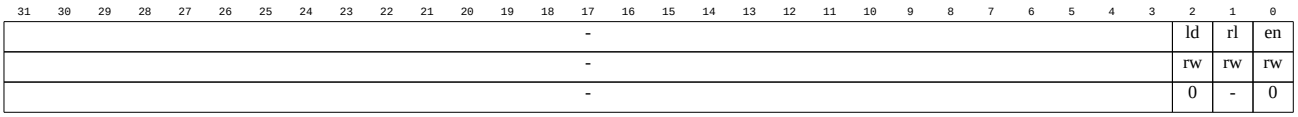
Timer 1 Control Register

Reset value

0x00000000

Warm reset mask

0x00000005



Field	Mask	Reset	Description
ld	0x00000004	0x0	Load counter
rl	0x00000002	-	Reload counter
en	0x00000001	0x0	Enable counter

Register WDG

Description

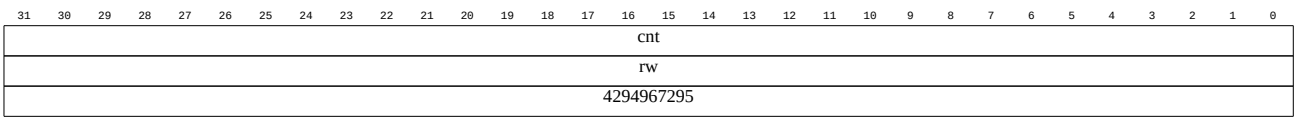
Watchdog Register

Reset value

0xffffffff

Warm reset mask

0xffffffff



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Field	Mask	Reset	Description
cnt	0xffffffff	0xffffffff	Watchdog counter value

Register TIMC2

Description

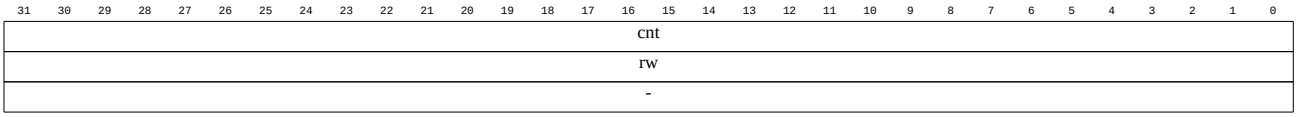
Timer 2 Counter Register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
cnt	0xffffffff	-	Timer 2 counter value

Register TIMR2

Description

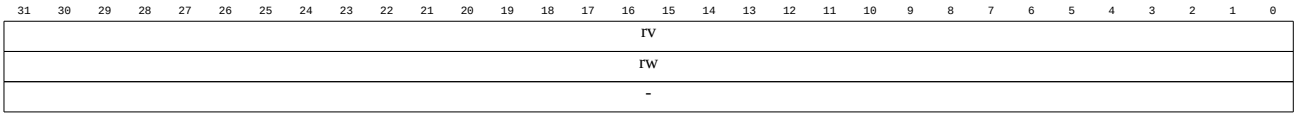
Timer 2 Reload Register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
rv	0xffffffff	-	Timer 2 reload value

Register TIMCTR2

Description

Timer 2 Control Register

Reset value

0x00000000

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Warm reset mask

0x00000005

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																													ld	rl	en
-																													rw	rw	rw
-																													0	-	0

Field	Mask	Reset	Description
ld	0x00000004	0x0	Load counter
rl	0x00000002	-	Reload counter
en	0x00000001	0x0	Enable counter

Register SCAC

Description

Prescaler Counter Register

Reset value

0x00000000

Warm reset mask

0x000003ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																						cnt									
-																						rw									
-																						0									

Field	Mask	Reset	Description
cnt	0x000003ff	0x0	Prescaler counter value

Register SCAR

Description

Prescaler Reload Register

Reset value

0x00000000

Warm reset mask

0x000003ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																						rv									
-																						rw									
-																						0									

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
rv	0x000003ff	0x0	Prescaler reload value

Register UAD1

Description

UART 1 Data Register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																									rtd						
-																									rw						
-																									-						

Field	Mask	Reset	Description
rtd	0x000000ff	-	Received/transmit data on UART 1

Register UAS1

Description

UART 1 Status Register

Reset value

0x00000006

Warm reset mask

0x0000007f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																									fe	pe	ov	br	th	ts	dr
-																									rw	rw	rw	rw	ro	ro	ro
-																									0	0	0	0	1	1	0

Field	Mask	Reset	Description
fe	0x00000040	0x0	Framing error
pe	0x00000020	0x0	Parity error
ov	0x00000010	0x0	Overrun
br	0x00000008	0x0	Break received
th	0x00000004	0x1	Transmitter hold register empty
ts	0x00000002	0x1	Transmitter shift register empty
dr	0x00000001	0x0	Data ready

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register UAC1

Description

UART 1 Control Register

Reset value

0x00000000

Warm reset mask

0x00000143

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																							ec	lb	fl	pe	ps	ti	ri	te	re
-																							rw	rw	rw	rw	rw	rw	rw	rw	rw
-																							0	-	0	-	-	-	-	0	0

Field	Mask	Reset	Description
ec	0x00000100	0x0	External clock
lb	0x00000080	-	Loop back
fl	0x00000040	0x0	Flow control
pe	0x00000020	-	Parity enable
ps	0x00000010	-	Parity select
ti	0x00000008	-	Transmitter interrupt enable
ri	0x00000004	-	Receiver interrupt enable
te	0x00000002	0x0	Transmitter enable
re	0x00000001	0x0	Receiver enable

Register UASCA1

Description

UART 1 Scaler Register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								rv							
-																								rw							
-																								-							

Field	Mask	Reset	Description
rv	0x000000ff	-	UART 1 scaler reload value

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register UAD2

Description

UART 2 Data Register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																									rtd						
-																									rw						
-																									-						

Field	Mask	Reset	Description
rtd	0x000000ff	-	Received/transmit data on UART 2

Register UAS2

Description

UART 2 Status Register

Reset value

0x00000006

Warm reset mask

0x0000007f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																									fe	pe	ov	br	th	ts	dr
-																									rw	rw	rw	rw	ro	ro	ro
-																									0	0	0	0	1	1	0

Field	Mask	Reset	Description
fe	0x00000040	0x0	Framing error
pe	0x00000020	0x0	Parity error
ov	0x00000010	0x0	Overrun
br	0x00000008	0x0	Break received
th	0x00000004	0x1	Transmitter hold register empty
ts	0x00000002	0x1	Transmitter shift register empty
dr	0x00000001	0x0	Data ready

Register UAC2

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

UART 2 Control Register

Reset value

0x00000000

Warm reset mask

0x00000143

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																							ec	lb	fl	pe	ps	ti	ri	te	re
-																							rw	rw	rw	rw	rw	rw	rw	rw	rw
-																							0	-	0	-	-	-	-	0	0

Field	Mask	Reset	Description
ec	0x00000100	0x0	External clock
lb	0x00000080	-	Loop back
fl	0x00000040	0x0	Flow control
pe	0x00000020	-	Parity enable
ps	0x00000010	-	Parity select
ti	0x00000008	-	Transmitter interrupt enable
ri	0x00000004	-	Receiver interrupt enable
te	0x00000002	0x0	Transmitter enable
re	0x00000001	0x0	Receiver enable

Register UASCA2

Description

UART 2 Scaler Register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								rv							
-																								rw							
-																								-							

Field	Mask	Reset	Description
rv	0x000000ff	-	UART 2 scaler reload value

Register ITMP

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

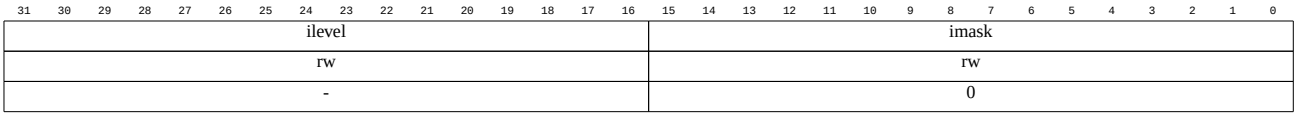
Interrupt Mask and Priority Register

Reset value

0x00000000

Warm reset mask

0x0000ffff



Field	Mask	Reset	Description
ilevel	0xffff0000	-	Interrupt level
imask	0x0000ffff	0x0	Interrupt mask

Register ITP

Description

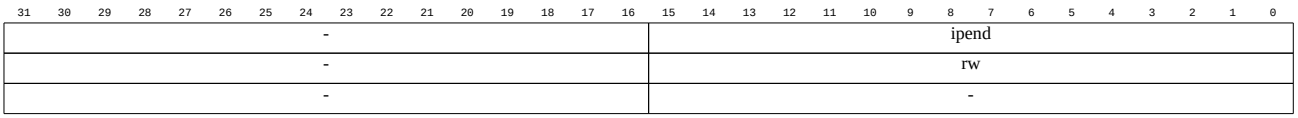
Interrupt Pending Register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
ipend	0x0000ffff	-	Interrupt pending

Register ITF

Description

Interrupt Force Register

Reset value

0x00000000

Warm reset mask

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																iforce															
-																rw															
-																-															

Field	Mask	Reset	Description
iforce	0x0000ffff	-	Interrupt force

Register ITC

Description

Interrupt Clear Register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																iclear															
-																wo															
-																-															

Field	Mask	Reset	Description
iclear	0x0000ffff	-	Interrupt clear

Register IODAT

Description

I/O Port Data Register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
meddat								lowdat								piodat															
rw								rw								rw															
-								-								-															

Field	Mask	Reset	Description
meddat	0xff000000	-	D[15:8] bus value
lowdat	0x00ff0000	-	D[7:0] bus value
piodat	0x0000ffff	-	PIO[15:0] port value

Register IODIR

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

I/O Port Direction Register

Reset value

0x00000000

Warm reset mask

0x0003ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-														meddir	lowdir	piodir															
-														rw	rw	rw															
-														0	0	0															

Field	Mask	Reset	Description
meddir	0x00020000	0x0	D[15:8] port direction
lowdir	0x00010000	0x0	D[7:0] port direction
piodir	0x0000ffff	0x0	PIO[15:0] port direction

Register IOIT1

Description

I/O Port Interrupt Register 1

Reset value

0x00000000

Warm reset mask

0x80808080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
en3	le3	pl3	isel3					en2	le2	pl2	isel2					en1	le1	pl1	isel1					en0	le0	pl0	isel0				
rw	rw	rw	rw					rw	rw	rw	rw					rw	rw	rw	rw					rw	rw	rw	rw				
0	-	-	-					0	-	-	-					0	-	-	-					0	-	-	-				

Field	Mask	Reset	Description
en3	0x80000000	0x0	Interrupt 3 enable
le3	0x40000000	-	Interrupt 3 level/edge trigger
pl3	0x20000000	-	Interrupt 3 polarity
isel3	0x1f000000	-	Interrupt 3 I/O port select
en2	0x00800000	0x0	Interrupt 2 enable
le2	0x00400000	-	Interrupt 2 level/edge trigger
pl2	0x00200000	-	Interrupt 2 polarity
isel2	0x001f0000	-	Interrupt 2 I/O port select
en1	0x00008000	0x0	Interrupt 1 enable

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
le1	0x00004000	-	Interrupt 1 level/edge trigger
pl1	0x00002000	-	Interrupt 1 polarity
isel1	0x00001f00	-	Interrupt 1 I/O port select
en0	0x00000080	0x0	Interrupt 0 enable
le0	0x00000040	-	Interrupt 0 level/edge trigger
pl0	0x00000020	-	Interrupt 0 polarity
isel0	0x0000001f	-	Interrupt 0 I/O port select

Register IOIT2

Description

I/O Port Interrupt Register 2

Reset value

0x00000000

Warm reset mask

0x80808080

31	30	29	28 27 26 25 24	23	22	21	20 19 18 17 16	15	14	13	12 11 10 9 8	7	6	5	4 3 2 1 0
en7	le7	pl7	isel7	en6	le6	pl6	isel6	en5	le5	pl5	isel5	en4	le4	pl4	isel4
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	-	-	-	0	-	-	-	0	-	-	-	0	-	-	-

Field	Mask	Reset	Description
en7	0x80000000	0x0	Interrupt 7 enable
le7	0x40000000	-	Interrupt 7 level/edge trigger
pl7	0x20000000	-	Interrupt 7 polarity
isel7	0x1f000000	-	Interrupt 7 I/O port select
en6	0x00800000	0x0	Interrupt 6 enable
le6	0x00400000	-	Interrupt 6 level/edge trigger
pl6	0x00200000	-	Interrupt 6 polarity
isel6	0x001f0000	-	Interrupt 6 I/O port select
en5	0x00008000	0x0	Interrupt 5 enable
le5	0x00004000	-	Interrupt 5 level/edge trigger
pl5	0x00002000	-	Interrupt 5 polarity
isel5	0x00001f00	-	Interrupt 5 I/O port select
en4	0x00000080	0x0	Interrupt 4 enable

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
le4	0x00000040	-	Interrupt 4 level/edge trigger
pl4	0x00000020	-	Interrupt 4 polarity
isel4	0x0000001f	-	Interrupt 4 I/O port select

Register WPSTA1

Description

Write Protection Start Address 1

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	start																													bp	-
-	rw																													rw	-
-	-																													-	-

Field	Mask	Reset	Description
start	0x3ffffffc	-	Start address
bp	0x00000002	-	Block protect

Register WPSTO1

Description

Write Protection End Address 1

Reset value

0x00000000

Warm reset mask

0x00000003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	end																													us	su
-	rw																													rw	rw
-	-																													0	0

Field	Mask	Reset	Description
end	0x3ffffffc	-	End address
us	0x00000002	0x0	User mode
su	0x00000001	0x0	Supervisor mode

Register WPSTA2

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Description

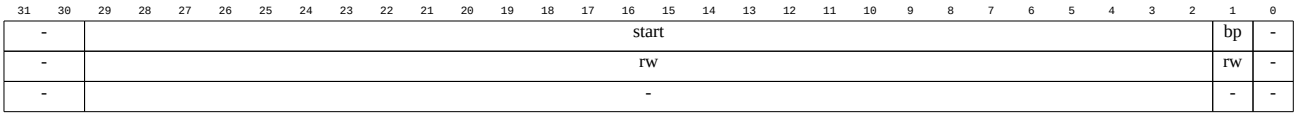
Write Protection Start Address 2

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
start	0x3ffffffc	-	Start address
bp	0x00000002	-	Block protect

Register WPSTO2

Description

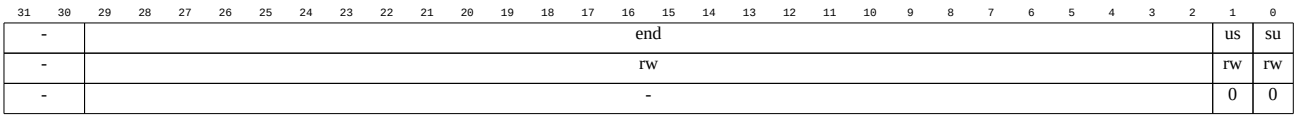
Write Protection End Address 2

Reset value

0x00000000

Warm reset mask

0x00000003



Field	Mask	Reset	Description
end	0x3ffffffc	-	End address
us	0x00000002	0x0	User mode
su	0x00000001	0x0	Supervisor mode

Commands

Name	Description
delete	Dispose instance of Leon2SoC
lowerInternalIrq	Lower internally numbered interrupts
raiseExternalIrq	Raise externally numbered interrupts
raiseInternalIrq	Raise internally numbered interrupts

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Command lowerInternalIrq Arguments

Name	Type	Required	Description
irq	int	yes	Interrupt number

Command raiseExternalIrq Arguments

Name	Type	Required	Description
irq	int	yes	Interrupt number

Command raiseInternalIrq Arguments

Name	Type	Required	Description
irq	int	yes	Interrupt number

7.3. Limitations

The Leon2 Device model simulates the AT697F chip. There are some deviations to the AT697E chip (e.g. the size of the counters). If you need the AT697E behaviour, please contact us for more info.

The following deviations from real hardware are known to exist, if you need the correct behaviour (or simulation of it, contact us for more info):

- No support for Ethernet at present
- No support for PCI at present
- The UARTs do not support external clocks.
- The UARTs do not support parity, framing errors and break signals.
- GPIO pin configurations are ignored for UARTs, the UARTs are assumed to be on separate dedicated I/O pins. However, a warning will be issued if the UART pins do not have the correct GPIO configuration.
- GPIO databus control is not supported (i.e. meddat and lowdat fields).
- Write protection registers have no effect
- Timer values are lazily computed on reads, the content in the case a timer is disabled is estimated on disabling time. This is in principle correct. However, the prescaler counter write has no effect, only the reload value has an effect when written. This may cause an offset of 1024 cycles when re-enabling a timer.
- In general the MEMCFG registers are ignored

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Chapter 8. MEC

The MEC (Memory Controller) device is used with the ERC32 processor. The device provides two UARTs, two timers and an interrupt interface. The interrupt interface allows for the raising and lowering of the 5 external interrupts provided by the ERC32 (IRQ 0 through (including) 4). The device model takes care of converting these to the relevant internal interrupts (i.e. SPARC IRQs 2,3,10,11 and 14).

When raising (or lowering) a MEC interrupt you need to use numbers 0-4.

8.1. Loading the Plugin

```
import Mec
```

8.2. Configuration

8.2.1. Interrupt Delivery

The property irqControl should be connected to the device which the MEC raises interrupts on, this is normally a CPU object. The connection should be made to the CPU-object's interface of type IrqIface. Note that the CPU must support interrupts 1 through 15, this is in general case correct for SPARC based processors, but other CPUs may not be compatible.

8.2.2. UART Connections

Two serial interfaces exist, the UartAIface and the UartBIface, these can be connected to in order to receive data from remote serial port terminals (i.e. this is the RX direction). The uarta and uartb properties can be used to connect the TX direction of the UARTs.

8.2.3. Infinite UART Speed

Set config.infiniteUartSpeed to nonzero to enable infinite speed on the Tx channels. With infinite speed, a written byte is immediately forwarded to the destination device, with limited UART speed (the variable being zero) the timing due to UART scaler bits (upper 8 bits of the MecCtrlReg) will be simulated, leading to realistic byte rates over the serial port device. Note that individual bits are not transmitted only the bytes.

8.2.4. @Mec Reference

Properties

Name	Type	Description
Class	*void	Class object

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @Mec
new	Create new instance of Mec

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

8.2.5. Mec Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
accessProtSegment1Base	uint32_t	Access protection segment 1 base register
accessProtSegment1BaseColdResetValue	uint32_t	Access protection segment 1 base register
accessProtSegment1BaseForcedBits	uint32_t	Access protection segment 1 base register
accessProtSegment1BaseForcedFlippedBits	uint32_t	Access protection segment 1 base register
accessProtSegment1BaseReadMask	uint32_t	Access protection segment 1 base register
accessProtSegment1BaseResetMask	uint32_t	Access protection segment 1 base register
accessProtSegment1BaseResetValue	uint32_t	Access protection segment 1 base register
accessProtSegment1BaseWriteMask	uint32_t	Access protection segment 1 base register
accessProtSegment1End	uint32_t	Access protection segment 1 end register
accessProtSegment1EndColdResetValue	uint32_t	Access protection segment 1 end register
accessProtSegment1EndForcedBits	uint32_t	Access protection segment 1 end register
accessProtSegment1EndForcedFlippedBits	uint32_t	Access protection segment 1 end register
accessProtSegment1EndReadMask	uint32_t	Access protection segment 1 end register
accessProtSegment1EndResetMask	uint32_t	Access protection segment 1 end register
accessProtSegment1EndResetValue	uint32_t	Access protection segment 1 end register
accessProtSegment1EndWriteMask	uint32_t	Access protection segment 1 end register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
accessProtSegment2Base	uint32_t	Access protection segment 2 base register
accessProtSegment2BaseColdResetValue	uint32_t	Access protection segment 2 base register
accessProtSegment2BaseForcedBits	uint32_t	Access protection segment 2 base register
accessProtSegment2BaseForcedFlippedBits	uint32_t	Access protection segment 2 base register
accessProtSegment2BaseReadMask	uint32_t	Access protection segment 2 base register
accessProtSegment2BaseResetMask	uint32_t	Access protection segment 2 base register
accessProtSegment2BaseResetValue	uint32_t	Access protection segment 2 base register
accessProtSegment2BaseWriteMask	uint32_t	Access protection segment 2 base register
accessProtSegment2End	uint32_t	Access protection segment 2 end register
accessProtSegment2EndColdResetValue	uint32_t	Access protection segment 2 end register
accessProtSegment2EndForcedBits	uint32_t	Access protection segment 2 end register
accessProtSegment2EndForcedFlippedBits	uint32_t	Access protection segment 2 end register
accessProtSegment2EndReadMask	uint32_t	Access protection segment 2 end register
accessProtSegment2EndResetMask	uint32_t	Access protection segment 2 end register
accessProtSegment2EndResetValue	uint32_t	Access protection segment 2 end register
accessProtSegment2EndWriteMask	uint32_t	Access protection segment 2 end register
config.infiniteUartSpeed	uint32_t	
cpu	temu_IfaceRef/ <unknown>	Processor
errorAndResetStatus	uint32_t	Error and reset status register
errorAndResetStatusColdResetValue	uint32_t	Error and reset status register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
errorAndResetStatusForcedBits	uint32_t	Error and reset status register
errorAndResetStatusForcedFlippedBits	uint32_t	Error and reset status register
errorAndResetStatusReadMask	uint32_t	Error and reset status register
errorAndResetStatusResetMask	uint32_t	Error and reset status register
errorAndResetStatusResetValue	uint32_t	Error and reset status register
errorAndResetStatusWriteMask	uint32_t	Error and reset status register
failingAddr	uint32_t	Failing address register
failingAddrColdResetValue	uint32_t	Failing address register
failingAddrForcedBits	uint32_t	Failing address register
failingAddrForcedFlippedBits	uint32_t	Failing address register
failingAddrReadMask	uint32_t	Failing address register
failingAddrResetMask	uint32_t	Failing address register
failingAddrResetValue	uint32_t	Failing address register
failingAddrWriteMask	uint32_t	Failing address register
gpiConfig	uint32_t	GPIO configuration register
gpiConfigColdResetValue	uint32_t	GPIO configuration register
gpiConfigForcedBits	uint32_t	GPIO configuration register
gpiConfigForcedFlippedBits	uint32_t	GPIO configuration register
gpiConfigReadMask	uint32_t	GPIO configuration register
gpiConfigResetMask	uint32_t	GPIO configuration register
gpiConfigResetValue	uint32_t	GPIO configuration register
gpiConfigWriteMask	uint32_t	GPIO configuration register
gpiData	uint32_t	GPIO data register
gpiDataColdResetValue	uint32_t	GPIO data register
gpiDataForcedBits	uint32_t	GPIO data register
gpiDataForcedFlippedBits	uint32_t	GPIO data register
gpiDataReadMask	uint32_t	GPIO data register
gpiDataResetMask	uint32_t	GPIO data register
gpiDataResetValue	uint32_t	GPIO data register
gpiDataWriteMask	uint32_t	GPIO data register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
gptCounter	uint32_t	General purpose timer counter register
gptCounterColdResetValue	uint32_t	General purpose timer counter register
gptCounterForcedBits	uint32_t	General purpose timer counter register
gptCounterForcedFlippedBits	uint32_t	General purpose timer counter register
gptCounterProgramReg	uint32_t	
gptCounterReadMask	uint32_t	General purpose timer counter register
gptCounterResetMask	uint32_t	General purpose timer counter register
gptCounterResetValue	uint32_t	General purpose timer counter register
gptCounterWriteMask	uint32_t	General purpose timer counter register
gptScaler	uint32_t	General purpose timer scaler register
gptScalerColdResetValue	uint32_t	General purpose timer scaler register
gptScalerForcedBits	uint32_t	General purpose timer scaler register
gptScalerForcedFlippedBits	uint32_t	General purpose timer scaler register
gptScalerProgramReg	uint32_t	
gptScalerReadMask	uint32_t	General purpose timer scaler register
gptScalerResetMask	uint32_t	General purpose timer scaler register
gptScalerResetValue	uint32_t	General purpose timer scaler register
gptScalerWriteMask	uint32_t	General purpose timer scaler register
ioConfig	uint32_t	I/O configuration register
ioConfigColdResetValue	uint32_t	I/O configuration register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ioConfigForcedBits	uint32_t	I/O configuration register
ioConfigForcedFlippedBits	uint32_t	I/O configuration register
ioConfigReadMask	uint32_t	I/O configuration register
ioConfigResetMask	uint32_t	I/O configuration register
ioConfigResetValue	uint32_t	I/O configuration register
ioConfigWriteMask	uint32_t	I/O configuration register
irqClear	uint32_t	Interrupt clear register
irqClearColdResetValue	uint32_t	Interrupt clear register
irqClearForcedBits	uint32_t	Interrupt clear register
irqClearForcedFlippedBits	uint32_t	Interrupt clear register
irqClearReadMask	uint32_t	Interrupt clear register
irqClearResetMask	uint32_t	Interrupt clear register
irqClearResetValue	uint32_t	Interrupt clear register
irqClearWriteMask	uint32_t	Interrupt clear register
irqControl	temu_IfaceRef/ <unknown>	Upstream interrupt controller (e.g. CPU)
irqForce	uint32_t	Interrupt force register
irqForceColdResetValue	uint32_t	Interrupt force register
irqForceForcedBits	uint32_t	Interrupt force register
irqForceForcedFlippedBits	uint32_t	Interrupt force register
irqForceReadMask	uint32_t	Interrupt force register
irqForceResetMask	uint32_t	Interrupt force register
irqForceResetValue	uint32_t	Interrupt force register
irqForceWriteMask	uint32_t	Interrupt force register
irqMask	uint32_t	Interrupt mask register
irqMaskColdResetValue	uint32_t	Interrupt mask register
irqMaskForcedBits	uint32_t	Interrupt mask register
irqMaskForcedFlippedBits	uint32_t	Interrupt mask register
irqMaskReadMask	uint32_t	Interrupt mask register
irqMaskResetMask	uint32_t	Interrupt mask register
irqMaskResetValue	uint32_t	Interrupt mask register
irqMaskWriteMask	uint32_t	Interrupt mask register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
irqPending	uint32_t	Interrupt pending register
irqPendingColdResetValue	uint32_t	Interrupt pending register
irqPendingForcedBits	uint32_t	Interrupt pending register
irqPendingForcedFlippedBits	uint32_t	Interrupt pending register
irqPendingReadMask	uint32_t	Interrupt pending register
irqPendingResetMask	uint32_t	Interrupt pending register
irqPendingResetValue	uint32_t	Interrupt pending register
irqPendingWriteMask	uint32_t	Interrupt pending register
irqShape	uint32_t	Interrupt shape register
irqShapeColdResetValue	uint32_t	Interrupt shape register
irqShapeForcedBits	uint32_t	Interrupt shape register
irqShapeForcedFlippedBits	uint32_t	Interrupt shape register
irqShapeReadMask	uint32_t	Interrupt shape register
irqShapeResetMask	uint32_t	Interrupt shape register
irqShapeResetValue	uint32_t	Interrupt shape register
irqShapeWriteMask	uint32_t	Interrupt shape register
irqSignalStatus	uint16_t	Interrupt signal status (should be the same as pending in CPU)
mecCtrl	uint32_t	MEC control register
mecCtrlColdResetValue	uint32_t	MEC control register
mecCtrlForcedBits	uint32_t	MEC control register
mecCtrlForcedFlippedBits	uint32_t	MEC control register
mecCtrlReadMask	uint32_t	MEC control register
mecCtrlResetMask	uint32_t	MEC control register
mecCtrlResetValue	uint32_t	MEC control register
mecCtrlWriteMask	uint32_t	MEC control register
memoryConfig	uint32_t	Memory configuration register
memoryConfigColdResetValue	uint32_t	Memory configuration register
memoryConfigForcedBits	uint32_t	Memory configuration register
memoryConfigForcedFlippedBits	uint32_t	Memory configuration register
memoryConfigReadMask	uint32_t	Memory configuration register

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Name	Type	Description
memoryConfigResetMask	uint32_t	Memory configuration register
memoryConfigResetValue	uint32_t	Memory configuration register
memoryConfigWriteMask	uint32_t	Memory configuration register
outSignals	[temu_IfaceRef; 8]/ <unknown>	GPIO signals
powerDown	uint32_t	Power down register
powerDownColdResetValue	uint32_t	Power down register
powerDownForcedBits	uint32_t	Power down register
powerDownForcedFlippedBits	uint32_t	Power down register
powerDownReadMask	uint32_t	Power down register
powerDownResetMask	uint32_t	Power down register
powerDownResetValue	uint32_t	Power down register
powerDownWriteMask	uint32_t	Power down register
rtcCounter	uint32_t	Real-time clock counter register
rtcCounterColdResetValue	uint32_t	Real-time clock counter register
rtcCounterForcedBits	uint32_t	Real-time clock counter register
rtcCounterForcedFlippedBits	uint32_t	Real-time clock counter register
rtcCounterProgramReg	uint32_t	
rtcCounterReadMask	uint32_t	Real-time clock counter register
rtcCounterResetMask	uint32_t	Real-time clock counter register
rtcCounterResetValue	uint32_t	Real-time clock counter register
rtcCounterWriteMask	uint32_t	Real-time clock counter register
rtcScaler	uint32_t	Real-time clock scaler register
rtcScalerColdResetValue	uint32_t	Real-time clock scaler register
rtcScalerForcedBits	uint32_t	Real-time clock scaler register
rtcScalerForcedFlippedBits	uint32_t	Real-time clock scaler register
rtcScalerProgramReg	uint32_t	
rtcScalerReadMask	uint32_t	Real-time clock scaler register
rtcScalerResetMask	uint32_t	Real-time clock scaler register
rtcScalerResetValue	uint32_t	Real-time clock scaler register
rtcScalerWriteMask	uint32_t	Real-time clock scaler register
softwareReset	uint32_t	Software reset register
softwareResetColdResetValue	uint32_t	Software reset register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
softwareResetForcedBits	uint32_t	Software reset register
softwareResetForcedFlippedBits	uint32_t	Software reset register
softwareResetReadMask	uint32_t	Software reset register
softwareResetResetMask	uint32_t	Software reset register
softwareResetResetValue	uint32_t	Software reset register
softwareResetWriteMask	uint32_t	Software reset register
systemFaultStatus	uint32_t	System fault status register
systemFaultStatusColdResetValue	uint32_t	System fault status register
systemFaultStatusForcedBits	uint32_t	System fault status register
systemFaultStatusForcedFlippedBits	uint32_t	System fault status register
systemFaultStatusReadMask	uint32_t	System fault status register
systemFaultStatusResetMask	uint32_t	System fault status register
systemFaultStatusResetValue	uint32_t	System fault status register
systemFaultStatusWriteMask	uint32_t	System fault status register
testControl	uint32_t	Test control register
testControlColdResetValue	uint32_t	Test control register
testControlForcedBits	uint32_t	Test control register
testControlForcedFlippedBits	uint32_t	Test control register
testControlReadMask	uint32_t	Test control register
testControlResetMask	uint32_t	Test control register
testControlResetValue	uint32_t	Test control register
testControlWriteMask	uint32_t	Test control register
timerControl	uint32_t	Timer control register
timerControlColdResetValue	uint32_t	Timer control register
timerControlForcedBits	uint32_t	Timer control register
timerControlForcedFlippedBits	uint32_t	Timer control register
timerControlReadMask	uint32_t	Timer control register
timerControlResetMask	uint32_t	Timer control register
timerControlResetValue	uint32_t	Timer control register
timerControlWriteMask	uint32_t	Timer control register

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Name	Type	Description
uartChanARxTx	uint32_t	UART channel A receive/transmit register
uartChanARxTxColdResetValue	uint32_t	UART channel A receive/transmit register
uartChanARxTxForcedBits	uint32_t	UART channel A receive/transmit register
uartChanARxTxForcedFlippedBits	uint32_t	UART channel A receive/transmit register
uartChanARxTxReadMask	uint32_t	UART channel A receive/transmit register
uartChanARxTxResetMask	uint32_t	UART channel A receive/transmit register
uartChanARxTxResetValue	uint32_t	UART channel A receive/transmit register
uartChanARxTxWriteMask	uint32_t	UART channel A receive/transmit register
uartChanBRxTx	uint32_t	UART channel B receive/transmit register
uartChanBRxTxColdResetValue	uint32_t	UART channel B receive/transmit register
uartChanBRxTxForcedBits	uint32_t	UART channel B receive/transmit register
uartChanBRxTxForcedFlippedBits	uint32_t	UART channel B receive/transmit register
uartChanBRxTxReadMask	uint32_t	UART channel B receive/transmit register
uartChanBRxTxResetMask	uint32_t	UART channel B receive/transmit register
uartChanBRxTxResetValue	uint32_t	UART channel B receive/transmit register
uartChanBRxTxWriteMask	uint32_t	UART channel B receive/transmit register
uartStatus	uint32_t	UART status register
uartStatusColdResetValue	uint32_t	UART status register
uartStatusForcedBits	uint32_t	UART status register
uartStatusForcedFlippedBits	uint32_t	UART status register

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Name	Type	Description
uartStatusReadMask	uint32_t	UART status register
uartStatusResetMask	uint32_t	UART status register
uartStatusResetValue	uint32_t	UART status register
uartStatusWriteMask	uint32_t	UART status register
uarta	temu_IfaceRef/ <unknown>	Serial port A
uartb	temu_IfaceRef/ <unknown>	Serial port B
waitStateConfig	uint32_t	Wait-state configuration register
waitStateConfigColdResetValue	uint32_t	Wait-state configuration register
waitStateConfigForcedBits	uint32_t	Wait-state configuration register
waitStateConfigForcedFlippedBits	uint32_t	Wait-state configuration register
waitStateConfigReadMask	uint32_t	Wait-state configuration register
waitStateConfigResetMask	uint32_t	Wait-state configuration register
waitStateConfigResetValue	uint32_t	Wait-state configuration register
waitStateConfigWriteMask	uint32_t	Wait-state configuration register
wdogProgAndTimeoutAck	uint32_t	Watchdog program and timeout acknowledge register
wdogProgAndTimeoutAckColdResetValue	uint32_t	Watchdog program and timeout acknowledge register
wdogProgAndTimeoutAckForcedBits	uint32_t	Watchdog program and timeout acknowledge register
wdogProgAndTimeoutAckForcedFlippedBits	uint32_t	Watchdog program and timeout acknowledge register
wdogProgAndTimeoutAckReadMask	uint32_t	Watchdog program and timeout acknowledge register
wdogProgAndTimeoutAckResetMask	uint32_t	Watchdog program and timeout acknowledge register
wdogProgAndTimeoutAckResetValue	uint32_t	Watchdog program and timeout acknowledge register

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Name	Type	Description
wdogProgAndTimeoutAckWriteMask	uint32_t	Watchdog program and timeout acknowledge register
wdogTrapDoorSet	uint32_t	Watchdog trap door set register
wdogTrapDoorSetColdResetValue	uint32_t	Watchdog trap door set register
wdogTrapDoorSetForcedBits	uint32_t	Watchdog trap door set register
wdogTrapDoorSetForcedFlippedBits	uint32_t	Watchdog trap door set register
wdogTrapDoorSetReadMask	uint32_t	Watchdog trap door set register
wdogTrapDoorSetResetMask	uint32_t	Watchdog trap door set register
wdogTrapDoorSetResetValue	uint32_t	Watchdog trap door set register
wdogTrapDoorSetWriteMask	uint32_t	Watchdog trap door set register

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	
IrqClientIface	IrqClientIface	
IrqIface	IrqIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	
SignalIface	SignalIface	Incomming signals
UartAIface	SerialIface	
UartBIface	SerialIface	

Ports

Prop	Iface	Description
irqControl	IrqClientIface	uart a
uarta	UartAIface	uart a
uartb	UartBIface	uart b

Registers



Register support is currently experimental!

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Register Bank Regs

Register mecCtrl

Description

MEC control register

Reset value

0x01b50014

Warm reset mask

0xffff7fff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Scaler								UCS	USB	UP	UPE	UBR	DST	DPE	DMAE	reserved	RHMECHE	MECHEMSK	RHFPUCMP	FPUCMPMSK	RHIUCMP	IUCMPMSK	RHIUHE	IUHEMSK	RHIUEM	IUEMMSK	WDCS	BP	BTO	SWR	PRD
rw								rw	rw	rw	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
1								1	0	1	1	0	1	0	1	-	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Field	Mask	Reset	Description
Scaler	0xff000000	0x1	UART scaler
UCS	0x00800000	0x1	UART clock supply
USB	0x00400000	0x0	UART stop bits
UP	0x00200000	0x1	UART parity
UPE	0x00100000	0x1	UART parity enable
UBR	0x00080000	0x0	UART baud rate divider select
DST	0x00040000	0x1	DMA session timeout enable
DPE	0x00020000	0x0	DMA parity enable
DMAE	0x00010000	0x1	DMA enable
reserved	0x00008000	-	Reserved
RHMECHE	0x00004000	0x0	Reset or halt on MEC hardware error
MECHEMSK	0x00002000	0x0	MEC hardware error mask
RHFPUCMP	0x00001000	0x0	Reset or halt on FPU comparison error
FPUCMPMSK	0x00000800	0x0	FPU comparison error mask
RHIUCMP	0x00000400	0x0	Reset or halt on IU comparison error
IUCMPMSK	0x00000200	0x0	IU comparison error mask
RHIUHE	0x00000100	0x0	Reset or halt on IU hardware error
IUHEMSK	0x00000080	0x0	IU hardware error mask
RHIUEM	0x00000040	0x0	Reset or halt on IU error mode
IUEMMSK	0x00000020	0x0	IU error mode mask
WDCS	0x00000010	0x1	Watchdog clock supply

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Field	Mask	Reset	Description
BP	0x00000008	0x0	Block protection instead of normal access protection
BTO	0x00000004	0x1	Bus timeout enable
SWR	0x00000002	0x0	Software reset enable
PRD	0x00000001	0x0	Power-down mode enable

Register softwareReset

Description

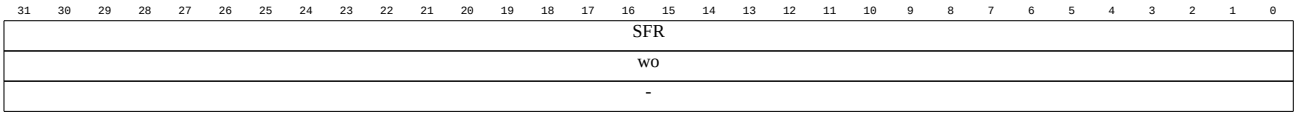
Software reset register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
SFR	0xffffffff	-	Software reset trigger

Register powerDown

Description

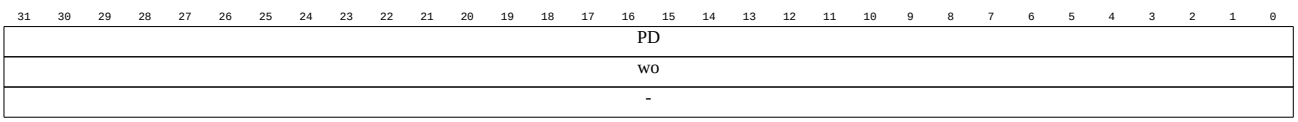
Power down register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
PD	0xffffffff	-	Power-down trigger

Register memoryConfig

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Description

Memory configuration register

Reset value

0x00010000

Warm reset mask

0x3f1f7fff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved		EEX	EEC	EPA	ESIZ			reserved			PSIZ			P8	PWR	reserved	REC	RPA	RSIZ			RBR1			RBS1	RBR0			RBS0	RBCS	
-		rw	rw	rw	rw			-			rw			rw	rw	-	rw	rw	rw			rw			rw	rw			rw	rw	
-		0	0	0	0			-			0			0	1	-	0	0	0			0			0	0			0	0	

Field	Mask	Reset	Description
reserved	0xc0000000	-	Reserved
EEX	0x20000000	0x0	Exchange memory enable
EEC	0x10000000	0x0	Exchange memory EDAC enable
EPA	0x08000000	0x0	Exchange memory parity enable
ESIZ	0x07000000	0x0	Exchange memory size
reserved	0x00e00000	-	Reserved
PSIZ	0x001c0000	0x0	PROM size
P8	0x00020000	0x0	PROM 8-bit mode
PWR	0x00010000	0x1	PROM write enable
reserved	0x00008000	-	Reserved
REC	0x00004000	0x0	RAM EDAC enable
RPA	0x00002000	0x0	RAM parity enable
RSIZ	0x00001c00	0x0	RAM size
RBR1	0x00000380	0x0	Redundant RAM block 1 replace
RBS1	0x00000040	0x0	Redundant RAM block 1 selected
RBR0	0x00000038	0x0	Redundant RAM block 0 replace
RBS0	0x00000004	0x0	Redundant RAM block 0 selected
RBCS	0x00000003	0x0	Number of RAM block chip selects

Register ioConfig

Description

I/O configuration register

Reset value

0x00000000

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Warm reset mask

0x3f3f3f3f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved		PA3	IO3	SIZ3				reserved		PA2	IO2	SIZ2				reserved		PA1	IO1	SIZ1				reserved		PA0	IO0	SIZ0			
-		rw	rw	rw				-		rw	rw	rw				-		rw	rw	rw				-		rw	rw	rw			
-		0	0	0				-		0	0	0				-		0	0	0				-		0	0	0			

Field	Mask	Reset	Description
reserved	0xc0000000	-	Reserved
PA3	0x20000000	0x0	I/O unit 3 parity enable
IO3	0x10000000	0x0	I/O unit 3 enable
SIZ3	0x0f000000	0x0	I/O unit 3 size
reserved	0x00c00000	-	Reserved
PA2	0x00200000	0x0	I/O unit 2 parity enable
IO2	0x00100000	0x0	I/O unit 2 enable
SIZ2	0x000f0000	0x0	I/O unit 2 size
reserved	0x0000c000	-	Reserved
PA1	0x00002000	0x0	I/O unit 1 parity enable
IO1	0x00001000	0x0	I/O unit 1 enable
SIZ1	0x00000f00	0x0	I/O unit 1 size
reserved	0x000000c0	-	Reserved
PA0	0x00000020	0x0	I/O unit 0 parity enable
IO0	0x00000010	0x0	I/O unit 0 enable
SIZ0	0x0000000f	0x0	I/O unit 0 size

Register waitStateConfig

Description

Wait-state configuration register

Reset value

0xffffffff

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IO3RW				IO2RW				IO1RW				IO0RW				EXRW				PRW				PRR				RAW		RAR	
rw				rw				rw				rw				rw				rw				rw				rw		rw	
15				15				15				15				15				15				15				3		3	

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Field	Mask	Reset	Description
IO3RW	0xf0000000	0xf	I/O unit 3 read/write waitstates
IO2RW	0x0f000000	0xf	I/O unit 2 read/write waitstates
IO1RW	0x00f00000	0xf	I/O unit 1 read/write waitstates
IO0RW	0x000f0000	0xf	I/O unit 0 read/write waitstates
EXRW	0x0000f000	0xf	Exchange memory read/write waitstates
PRW	0x00000f00	0xf	PROM write waitstates
PRR	0x000000f0	0xf	PROM read waitstates
RAW	0x0000000c	0x3	RAM write waitstates
RAR	0x00000003	0x3	RAM read waitstates

Register accessProtSegment1Base

Description

Access protection segment 1 base register

Reset value

0x00000000

Warm reset mask

0x01ffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved							SE	UE	SEGBASE																						
-							rw	rw	rw																						
-							0	0	0																						

Field	Mask	Reset	Description
reserved	0xfe000000	-	Reserved
SE	0x01000000	0x0	Supervisor mode enable
UE	0x00800000	0x0	User mode enable
SEGBASE	0x007fffff	0x0	Segment base address

Register accessProtSegment1End

Description

Access protection segment 1 end register

Reset value

0x00000000

Warm reset mask

0x007fffff

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved									SEGEND																						
-									rw																						
-									0																						

Field	Mask	Reset	Description
reserved	0xff800000	-	Reserved
SEGEND	0x007fffff	0x0	Segment end address

Register accessProtSegment2Base

Description

Access protection segment 2 base register

Reset value

0x00000000

Warm reset mask

0x01ffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved							SE	UE	SEGBASE																						
-							rw	rw	rw																						
-							0	0	0																						

Field	Mask	Reset	Description
reserved	0xfe000000	-	Reserved
SE	0x01000000	0x0	Supervisor mode enable
UE	0x00800000	0x0	User mode enable
SEGBASE	0x007fffff	0x0	Segment base address

Register accessProtSegment2End

Description

Access protection segment 2 end register

Reset value

0x00000000

Warm reset mask

0x007fffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved									SEGEND																						
-									rw																						
-									0																						

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Field	Mask	Reset	Description
reserved	0xff800000	-	Reserved
SEGEND	0x007fffff	0x0	Segment end address

Register irqShape

Description

Interrupt shape register

Reset value

0x00000000

Warm reset mask

0x00001fff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																			POL					ACK				EDGE			
-																			rw					rw				rw			
-																			0					0				0			

Field	Mask	Reset	Description
reserved	0xfffe000	-	Reserved
POL	0x00001f00	0x0	External interrupt polarity select
ACK	0x000000e0	0x0	External interrupt acknowledge select
EDGE	0x0000001f	0x0	External interrupt edge/level select

Register irqPending

Description

Interrupt pending register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																IP														reserve	
-																rw														-	
-																0														-	

Field	Mask	Reset	Description
reserved	0xffff0000	-	Reserved
IP	0x0000fffe	0x0	Interrupt pending bits
reserved	0x00000001	-	Reserved

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Register irqMask

Description

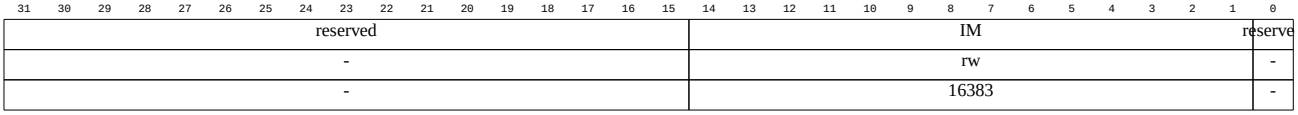
Interrupt mask register

Reset value

0x00007ffe

Warm reset mask

0x00007ffe



31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
reserved	IM	reserve
-	rw	-
-	16383	-

Field	Mask	Reset	Description
reserved	0xffff8000	-	Reserved
IM	0x00007ffe	0x3fff	Interrupt mask bits
reserved	0x00000001	-	Reserved

Register irqClear

Description

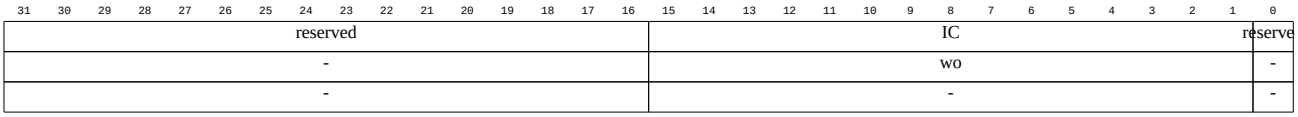
Interrupt clear register

Reset value

0x00000000

Warm reset mask

0x00000000



31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
reserved	IC	reserve
-	wo	-
-	-	-

Field	Mask	Reset	Description
reserved	0xffff0000	-	Reserved
IC	0x0000fffe	-	Interrupt clear bits
reserved	0x00000001	-	Reserved

Register irqForce

Description

Interrupt force register

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Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																IF															reserve
-																rw															-
-																0															-

Field	Mask	Reset	Description
reserved	0xffff0000	-	Reserved
IF	0x0000fffe	0x0	Interrupt force bits
reserved	0x00000001	-	Reserved

Register wdogProgAndTimeoutAck

Description

Watchdog program and timeout acknowledge register

Reset value

0xffffffff

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDR								WDS								WDC															
rw								rw								rw															
-								-								-															

Field	Mask	Reset	Description
WDR	0xff000000	-	Watchdog reset counter value
WDS	0x00ff0000	-	Watchdog preset scaler value
WDC	0x0000ffff	-	Watchdog preset counter value

Register wdogTrapDoorSet

Description

Watchdog trap door set register

Reset value

0xffffffff

Warm reset mask

0x00000000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TD																															
wo																															
-																															

Field	Mask	Reset	Description
TD	0xffffffff	-	Watchdog trap door set

Register rtcCounter

Description

Real-time clock counter register

Reset value

0xffffffff

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTCC																															
rw																															
4294967295																															

Field	Mask	Reset	Description
RTCC	0xffffffff	0xffffffff	Real-time clock counter

Register rtcScaler

Description

Real-time clock scaler register

Reset value

0x000000ff

Warm reset mask

0x000000ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								RTCS							
-																								rw							
-																								255							

Field	Mask	Reset	Description
reserved	0xffffff00	-	Reserved
RTCS	0x000000ff	0xff	Real-time clock scaler

Register gptCounter

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Description

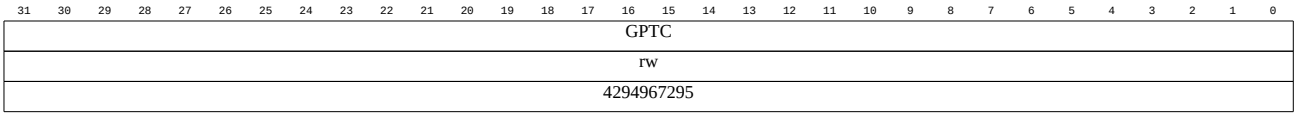
General purpose timer counter register

Reset value

0xffffffff

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
GPTC	0xffffffff	0xffffffff	General purpose timer counter

Register gptScaler

Description

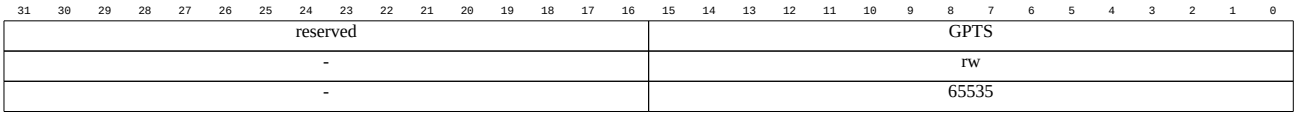
General purpose timer scaler register

Reset value

0x0000ffff

Warm reset mask

0x0000ffff



Field	Mask	Reset	Description
reserved	0xffff0000	-	Reserved
GPTS	0x0000ffff	0xffff	General purpose timer scaler

Register timerControl

Description

Timer control register

Reset value

0x00000100

Warm reset mask

0x00000f0f

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																				RTCSL	RTCSE	RTCCL	RTCCR	reserved				GSL	GSE	GCL	GCR	
-																				rw	rw	rw	rw	-				rw	rw	rw	rw	
-																				0	0	0	1	-				0	0	0	0	

Field	Mask	Reset	Description
reserved	0xfffff000	-	Reserved
RTCSL	0x00000800	0x0	Real-time clock scaler load
RTCSE	0x00000400	0x0	Real-time clock scaler enable
RTCCL	0x00000200	0x0	Real-time clock counter load
RTCCR	0x00000100	0x1	Real-time clock counter reload
reserved	0x000000f0	-	Reserved
GSL	0x00000008	0x0	General purpose timer scaler load
GSE	0x00000004	0x0	General purpose timer enable
GCL	0x00000002	0x0	General purpose timer counter load
GCR	0x00000001	0x0	General purpose timer counter reload

Register systemFaultStatus

Description

System fault status register

Reset value

0x00000078

Warm reset mask

0x0000f77c

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																AT				reserved		ASFT	ASFV	reserved				SRFT		SDFV	reserved	
-																rw				-		rw	rw	-				rw		rw	-	
-																0				-		0	0	-				15		0	-	

Field	Mask	Reset	Description
reserved	0xffff0000	-	Reserved
AT	0x0000f000	0x0	Access type
reserved	0x00000800	-	Reserved
ASFT	0x00000600	0x0	Asynchronous fault type
ASFV	0x00000100	0x0	Asynchronous fault valid
reserved	0x00000080	-	Reserved
SRFT	0x00000078	0xf	Data fault type or DMA error type
SDFV	0x00000004	0x0	IU data fault valid

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Field	Mask	Reset	Description
reserved	0x00000003	-	Reserved

Register failingAddr

Description

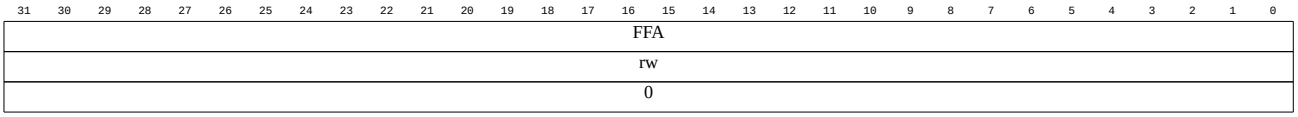
Failing address register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
FFA	0xffffffff	0x0	Failing address

Register gpiConfig

Description

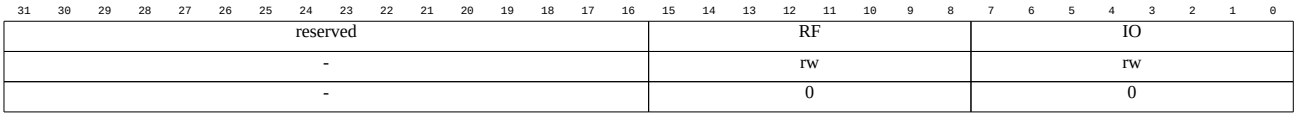
GPIO configuration register

Reset value

0x00000000

Warm reset mask

0x0000ffff



Field	Mask	Reset	Description
reserved	0xffff0000	-	Reserved
RF	0x0000ff00	0x0	GPIO read flag
IO	0x000000ff	0x0	GPIO input/output select

Register gpiData

Description

GPIO data register

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Reset value

0x00000000

Warm reset mask

0x000000ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								IOD							
-																								rw							
-																								0							

Field	Mask	Reset	Description
reserved	0xffffff00	-	Reserved
IOD	0x000000ff	0x0	GPIO data

Register errorAndResetStatus

Description

Error and reset status register

Reset value

0x00000000

Warm reset mask

0x0000f03f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																RSTC		HLT	SYSAV	reserved						MECHE	FPUCMP	FPUHE	IUCMP	IUHE	IUEM
-																rw		rw	rw	-						rw	rw	rw	rw	rw	rw
-																0		0	0	-						0	0	0	0	0	0

Field	Mask	Reset	Description
reserved	0xffff0000	-	Reserved
RSTC	0x0000c000	0x0	Reset cause
HLT	0x00002000	0x0	IU/FPU halted
SYSAV	0x00001000	0x0	ERC32 system availability
reserved	0x00000fc0	-	Reserved
MECHE	0x00000020	0x0	MEC hardware error
FPUCMP	0x00000010	0x0	FPU comparison error
FPUHE	0x00000008	0x0	FPU hardware error
IUCMP	0x00000004	0x0	IU comparison error
IUHE	0x00000002	0x0	IU hardware error
IUEM	0x00000001	0x0	IU error mode

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Register testControl

Description

Test control register

Reset value

0x00000000

Warm reset mask

0x001e007f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved											EWE	IT	PT	ET	reserved										CB						
-											rw	rw	rw	rw	-										rw						
-											0	0	0	0	-										0						

Field	Mask	Reset	Description
reserved	0xffe00000	-	Reserved
EWE	0x00100000	0x0	Error write enable
IT	0x00080000	0x0	Interrupt test enable
PT	0x00040000	0x0	Memory parity test enable
ET	0x00020000	0x0	EDAC test enable
reserved	0x0001ff80	-	Reserved
CB	0x0000007f	0x0	EDAC test checkbits

Register uartChanARxTx

Description

UART channel A receive/transmit register

Reset value

0x00000000

Warm reset mask

0x000000ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								Data							
-																								rw							
-																								0							

Field	Mask	Reset	Description
reserved	0xffffff00	-	Reserved
Data	0x000000ff	0x0	UART channel A receive/transmit data

Register uartChanBRxTx

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

UART channel B receive/transmit register

Reset value

0x00000000

Warm reset mask

0x000000ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved																								Data							
-																								rw							
-																								0							

Field	Mask	Reset	Description
reserved	0xffffff00	-	Reserved
Data	0x000000ff	0x0	UART channel B receive/transmit data

Register uartStatus

Description

UART status register

Reset value

0x00060006

Warm reset mask

0x00f700f7

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved								CLB	OEB	PEB	FEB	reserved	THEB	TSEB	DRB	reserved								CL	OE	PE	FE	reserved	THEA	TSEA	DR
-								rw	rw	rw	rw	-	rw	rw	rw	-								rw	rw	rw	rw	-	rw	rw	rw
-								0	0	0	0	-	1	1	0	-								0	0	0	0	-	1	1	0

Field	Mask	Reset	Description
reserved	0xff000000	-	Reserved
CLB	0x00800000	0x0	UART B clear
OEB	0x00400000	0x0	UART B overrun error
PEB	0x00200000	0x0	UART B parity error
FEB	0x00100000	0x0	UART B framing error
reserved	0x00080000	-	Reserved
THEB	0x00040000	0x1	UART B transmitter holding register empty
TSEB	0x00020000	0x1	UART B transmitter send register empty
DRB	0x00010000	0x0	UART B data ready
reserved	0x0000ff00	-	Reserved

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Field	Mask	Reset	Description
CL	0x00000080	0x0	UART A clear
OE	0x00000040	0x0	UART A overrun error
PE	0x00000020	0x0	UART A parity error
FE	0x00000010	0x0	UART A framing error
reserved	0x00000008	-	Reserved
THEA	0x00000004	0x1	UART A transmitter holding register empty
TSEA	0x00000002	0x1	UART A transmitter send register empty
DR	0x00000001	0x0	UART A data ready

Commands

Name	Description
delete	Dispose instance of Mec

8.3. Notes

The MEC sets the interrupt pending register bit when an interrupt is raised even when the interrupt is masked. The mask is only applied when evaluating whether to raise an IRQ with the CPU.

8.4. Limitations

The following deviations from real hardware are known to exist. If you need the correct behavior (contact us for more info).

- The UARTs do not support external (watchdog) clocks.
- The UARTs do not support parity, framing errors, break signals or stop bit configuration. Note that transmission times do take into account stop and parity bits.
- Write protection registers have no effect
- Timer values are lazily computed on reads, the content in the case a timer is disabled is estimated on disabling time. This is in principle correct. However, the prescaler counter write has no effect, only the reload value has an effect when written. This may cause an offset of 1024 cycles when re-enabling a timer.

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Chapter 9. GRLIB

9.1. APBUART

The ApbUart model is available in the ApbUart plugin. That plugin is part of the GRLIB device library feature. The ApbUart model supports both FIFO simualtion and infinite speed UARTs. In infinite speed mode bytes are sent directly when they are written to the data register.

9.1.1. Loading the Plugin

```
import ApbUart
```

@ApbUart Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @ApbUart
new	Create new instance of ApbUart

Command new Arguments

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Required	Description
name	string	yes	Name of object to create

ApbUart Reference

Properties

Name	Type	Description
CTRLColdResetValue	uint32_t	UART control register
CTRLForcedBits	uint32_t	UART control register
CTRLForcedFlippedBits	uint32_t	UART control register
CTRLReadMask	uint32_t	UART control register
CTRLResetMask	uint32_t	UART control register
CTRLResetValue	uint32_t	UART control register
CTRLWriteMask	uint32_t	UART control register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
DATAColdResetValue	uint32_t	UART data register
DATAForcedBits	uint32_t	UART data register
DATAForcedFlippedBits	uint32_t	UART data register
DATAReadMask	uint32_t	UART data register
DATAResetMask	uint32_t	UART data register
DATAResetValue	uint32_t	UART data register
DATAWriteMask	uint32_t	UART data register
DEBUG	uint32_t	UART FIFO debug register
DEBUGColdResetValue	uint32_t	UART FIFO debug register
DEBUGForcedBits	uint32_t	UART FIFO debug register
DEBUGForcedFlippedBits	uint32_t	UART FIFO debug register
DEBUGReadMask	uint32_t	UART FIFO debug register
DEBUGResetMask	uint32_t	UART FIFO debug register
DEBUGResetValue	uint32_t	UART FIFO debug register
DEBUGWriteMask	uint32_t	UART FIFO debug register
LocalName	*char	Local name (in component, if applicable)

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Name	Type	Description
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
SCALERColdResetValue	uint32_t	UART scaler reload register
SCALERForcedBits	uint32_t	UART scaler reload register
SCALERForcedFlippedBits	uint32_t	UART scaler reload register
SCALERReadMask	uint32_t	UART scaler reload register
SCALERResetMask	uint32_t	UART scaler reload register
SCALERResetValue	uint32_t	UART scaler reload register
SCALERWriteMask	uint32_t	UART scaler reload register
STATColdResetValue	uint32_t	UART status register
STATForcedBits	uint32_t	UART status register
STATForcedFlippedBits	uint32_t	UART status register
STATReadMask	uint32_t	UART status register
STATResetMask	uint32_t	UART status register
STATResetValue	uint32_t	UART status register
STATWriteMask	uint32_t	UART status register
TimeSource	*void	Time source object
config.clockDivider	uint32_t	Clock divider
config.fifoSize	uint8_t	UART FIFO size
config.infiniteUartSpeed	uint8_t	Set to 1 to enable immediate UARTs
config.interrupt	uint8_t	Interrupt number
config.littleEndian	uint8_t	Endianess of memory interface.
control	uint32_t	UART control register
data	uint32_t	UART data register
irqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller.
pnp.bar	uint32_t	AMBA plug and play base address register

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Name	Type	Description
pnp.config	uint32_t	AMBA plug and play config word
rxFifo.data	[uint8_t; 32]	RX FIFO data
rxFifo.size	uint8_t	RX size
rxFifo.start	uint8_t	RX start index
rxFifo.usage	uint8_t	RX usage
scaler	uint32_t	UART scaler reload register
status	uint32_t	UART status register
tx	temu_IfaceRef/ <unknown>	Transmit target.
txFifo.data	[uint8_t; 32]	TX FIFO data
txFifo.size	uint8_t	TX size
txFifo.start	uint8_t	TX start index
txFifo.usage	uint8_t	TX usage
txShift	uint8_t	UART shift register

Interfaces

Name	Type	Description
ApbIface	ApbIface	AMBA plug and play interface.
DeviceIface	DeviceIface	Device interface.
MemAccessIface	MemAccessIface	Memory access interface.
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	Reset interface.
UartIface	SerialIface	Serial input interface.

Ports

Prop	Iface	Description
tx	UartIface	serial port

Registers



Register support is currently experimental!

Register Bank Regs

Register DATA

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Description

UART data register

Reset value

0x00000000

Warm reset mask

0x000000ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								DATA							
-																								rw							
-																								0							

Field	Mask	Reset	Description
DATA	0x000000ff	0x0	Receiver/Transmitter holding register or FIFO

Register STAT

Description

UART status register

Reset value

0x00000006

Warm reset mask

0xfff007ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RCNT						TCNT						-									RF	TF	RH	TH	FE	PE	OV	BR	TE	TS	DR
ro						ro						-									ro	ro	ro	ro	rw	rw	rw	rw	ro	ro	ro
0						0						-									0	0	0	0	0	0	0	0	1	1	0

Field	Mask	Reset	Description
RCNT	0xfc000000	0x0	Receiver FIFO count
TCNT	0x03f00000	0x0	Transmitter FIFO count
RF	0x00000400	0x0	Receiver FIFO full
TF	0x00000200	0x0	Transmitter FIFO full
RH	0x00000100	0x0	Receiver FIFO half-full
TH	0x00000080	0x0	Transmitter FIFO half-full
FE	0x00000040	0x0	Framing error
PE	0x00000020	0x0	Parity error
OV	0x00000010	0x0	Overrun
BR	0x00000008	0x0	Break received
TE	0x00000004	0x1	Transmitter FIFO empty

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Field	Mask	Reset	Description
TS	0x00000002	0x1	Transmitter shift register empty
DR	0x00000001	0x0	Data Ready

Register CTRL

Description

UART control register

Reset value

0x00000000

Warm reset mask

0x8000ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FA	-															NS	SI	DI	BI	DB	RF	TF	EC	LB	FL	PE	PS	TI	RI	TE	RE
ro	-															rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	-															0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
FA	0x80000000	0x0	FIFOs available
NS	0x00008000	0x0	Number of stop bits
SI	0x00004000	0x0	Transmitter shift register empty interrupt enable
DI	0x00002000	0x0	Delayed interrupt enable
BI	0x00001000	0x0	Break interrupt enable
DB	0x00000800	0x0	FIFO debug mode enable
RF	0x00000400	0x0	Receiver FIFO interrupt enable
TF	0x00000200	0x0	Transmitter FIFO interrupt enable
EC	0x00000100	0x0	External clock
LB	0x00000080	0x0	Loop back
FL	0x00000040	0x0	Flow control
PE	0x00000020	0x0	Parity enable
PS	0x00000010	0x0	Parity select
TI	0x00000008	0x0	Transmitter interrupt enable
RI	0x00000004	0x0	Receiver interrupt enable
TE	0x00000002	0x0	Transmitter enable
RE	0x00000001	0x0	Receiver enable

Register SCALER

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Description

UART scaler reload register

Reset value

0x00000000

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCALER																															
rw																															
0																															

Field	Mask	Reset	Description
SCALER	0xffffffff	0x0	Scaler reload value

Register DEBUG

Description

UART FIFO debug register

Reset value

0x00000000

Warm reset mask

0x000000ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								DATA							
-																								rw							
-																								0							

Field	Mask	Reset	Description
DATA	0x000000ff	0x0	Receiver/Transmitter holding register or FIFO

Commands

Name	Description
delete	Dispose instance of ApbUart
enable-rx	Enable receiver
enable-tx	Enable transmitter

9.1.2. Limitations

- Loop back mode is not presently supported.
- Control flow (cts) is not supported.

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9.2. B1553BRM

The B1553BRM is part of the GRLIB device library from Gaisler. The device integrates the Actel Core1553BRM chip inside an AMBA bridge.

9.2.1. Loading the Plugin

```
import B1553BRM
```

9.2.2. Configuration

9.2.3. B1553BRM Reference

Properties

Name	Type	Description
AHBPAGEColdResetValue	uint32_t	AHB page address register
AHBPAGEForcedBits	uint32_t	AHB page address register
AHBPAGEForcedFlippedBits	uint32_t	AHB page address register
AHBPAGEReadMask	uint32_t	AHB page address register
AHBPAGEResetMask	uint32_t	AHB page address register
AHBPAGEResetValue	uint32_t	AHB page address register
AHBPAGEWriteMask	uint32_t	AHB page address register
AMBAIRQColdResetValue	uint32_t	B1553BRM interrupt settings register
AMBAIRQForcedBits	uint32_t	B1553BRM interrupt settings register
AMBAIRQForcedFlippedBits	uint32_t	B1553BRM interrupt settings register
AMBAIRQReadMask	uint32_t	B1553BRM interrupt settings register
AMBAIRQResetMask	uint32_t	B1553BRM interrupt settings register
AMBAIRQResetValue	uint32_t	B1553BRM interrupt settings register
AMBAIRQWriteMask	uint32_t	B1553BRM interrupt settings register
AMBASTATCTRLColdResetValue	uint32_t	B1553BRM status/control register

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Name	Type	Description
AMBASTATCTRLForcedBits	uint32_t	B1553BRM status/control register
AMBASTATCTRLForcedFlippedBits	uint32_t	B1553BRM status/control register
AMBASTATCTRLReadMask	uint32_t	B1553BRM status/control register
AMBASTATCTRLResetMask	uint32_t	B1553BRM status/control register
AMBASTATCTRLResetValue	uint32_t	B1553BRM status/control register
AMBASTATCTRLWriteMask	uint32_t	B1553BRM status/control register
BITREGColdResetValue	uint16_t	BRM built-in test register
BITREGForcedBits	uint16_t	BRM built-in test register
BITREGForcedFlippedBits	uint16_t	BRM built-in test register
BITREGReadMask	uint16_t	BRM built-in test register
BITREGResetMask	uint16_t	BRM built-in test register
BITREGResetValue	uint16_t	BRM built-in test register
BITREGWriteMask	uint16_t	BRM built-in test register
BrmBcCommandBlockPointer	uint16_t	BRM descriptor/command block pointer register
BrmBcMinorFrameTimerRegister	uint16_t	BRM time tag / minor frame timer register
BrmBuiltinTestRegister	uint16_t	BRM built-in test register
BrmControl	uint16_t	BRM control register
BrmCurrentCommand	uint16_t	BRM current command register
BrmEnhancedFeaturesRegister	uint16_t	BRM enhanced features register
BrmInterruptMask	uint16_t	BRM interrupt mask
BrmInterruptPointer	uint16_t	BRM interrupt pointer
BrmOperationAndStatus	uint16_t	BRM operation and status register
BrmPendingInterrupt	uint16_t	BRM pending interrupt
BrmRt1553abStatusWordRegister	uint16_t	BRM 1553A/B status word register
BrmRtLegalizationRegisters	[uint16_t; 16]	RT legalization register

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Name	Type	Description
CONTROLColdResetValue	uint16_t	BRM control register
CONTROLForcedBits	uint16_t	BRM control register
CONTROLForcedFlippedBits	uint16_t	BRM control register
CONTROLReadMask	uint16_t	BRM control register
CONTROLResetMask	uint16_t	BRM control register
CONTROLResetValue	uint16_t	BRM control register
CONTROLWriteMask	uint16_t	BRM control register
CURRENTCOMMANDColdResetValue	uint16_t	BRM current command register
CURRENTCOMMANDForcedBits	uint16_t	BRM current command register
CURRENTCOMMANDForcedFlippedBits	uint16_t	BRM current command register
CURRENTCOMMANDReadMask	uint16_t	BRM current command register
CURRENTCOMMANDResetMask	uint16_t	BRM current command register
CURRENTCOMMANDResetValue	uint16_t	BRM current command register
CURRENTCOMMANDWriteMask	uint16_t	BRM current command register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
DESCCMDPTRColdResetValue	uint16_t	BRM descriptor/command block pointer register
DESCCMDPTRForcedBits	uint16_t	BRM descriptor/command block pointer register
DESCCMDPTRForcedFlippedBits	uint16_t	BRM descriptor/command block pointer register
DESCCMDPTRReadMask	uint16_t	BRM descriptor/command block pointer register
DESCCMDPTRResetMask	uint16_t	BRM descriptor/command block pointer register
DESCCMDPTRResetValue	uint16_t	BRM descriptor/command block pointer register
DESCCMDPTRWriteMask	uint16_t	BRM descriptor/command block pointer register
ENHANCEDColdResetValue	uint16_t	BRM enhanced features register
ENHANCEDForcedBits	uint16_t	BRM enhanced features register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ENHANCEDForcedFlippedBits	uint16_t	BRM enhanced features register
ENHANCEDReadMask	uint16_t	BRM enhanced features register
ENHANCEDResetMask	uint16_t	BRM enhanced features register
ENHANCEDResetValue	uint16_t	BRM enhanced features register
ENHANCEDWriteMask	uint16_t	BRM enhanced features register
INITCOUNT	uint16_t	BRM initialization count register
INITCOUNTColdResetValue	uint16_t	BRM initialization count register
INITCOUNTForcedBits	uint16_t	BRM initialization count register
INITCOUNTForcedFlippedBits	uint16_t	BRM initialization count register
INITCOUNTReadMask	uint16_t	BRM initialization count register
INITCOUNTResetMask	uint16_t	BRM initialization count register
INITCOUNTResetValue	uint16_t	BRM initialization count register
INITCOUNTWriteMask	uint16_t	BRM initialization count register
INTMASKColdResetValue	uint16_t	BRM interrupt mask
INTMASKForcedBits	uint16_t	BRM interrupt mask
INTMASKForcedFlippedBits	uint16_t	BRM interrupt mask
INTMASKReadMask	uint16_t	BRM interrupt mask
INTMASKResetMask	uint16_t	BRM interrupt mask
INTMASKResetValue	uint16_t	BRM interrupt mask
INTMASKWriteMask	uint16_t	BRM interrupt mask
INTPTRColdResetValue	uint16_t	BRM interrupt pointer
INTPTRForcedBits	uint16_t	BRM interrupt pointer
INTPTRForcedFlippedBits	uint16_t	BRM interrupt pointer
INTPTRReadMask	uint16_t	BRM interrupt pointer
INTPTRResetMask	uint16_t	BRM interrupt pointer
INTPTRResetValue	uint16_t	BRM interrupt pointer

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
INTPTRWriteMask	uint16_t	BRM interrupt pointer
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
OPSTATColdResetValue	uint16_t	BRM operation and status register
OPSTATForcedBits	uint16_t	BRM operation and status register
OPSTATForcedFlippedBits	uint16_t	BRM operation and status register
OPSTATReadMask	uint16_t	BRM operation and status register
OPSTATResetMask	uint16_t	BRM operation and status register
OPSTATResetValue	uint16_t	BRM operation and status register
OPSTATWriteMask	uint16_t	BRM operation and status register
ObjectID	uint64_t	Unique ObjectID.
PENDINTColdResetValue	uint16_t	BRM pending interrupt
PENDINTForcedBits	uint16_t	BRM pending interrupt
PENDINTForcedFlippedBits	uint16_t	BRM pending interrupt
PENDINTReadMask	uint16_t	BRM pending interrupt
PENDINTResetMask	uint16_t	BRM pending interrupt
PENDINTResetValue	uint16_t	BRM pending interrupt
PENDINTWriteMask	uint16_t	BRM pending interrupt
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
STATUSWORDColdResetValue	uint16_t	BRM 1553A/B status word register
STATUSWORDForcedBits	uint16_t	BRM 1553A/B status word register

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Name	Type	Description
STATUSWORDForcedFlippedBits	uint16_t	BRM 1553A/B status word register
STATUSWORDReadMask	uint16_t	BRM 1553A/B status word register
STATUSWORDResetMask	uint16_t	BRM 1553A/B status word register
STATUSWORDResetValue	uint16_t	BRM 1553A/B status word register
STATUSWORDWriteMask	uint16_t	BRM 1553A/B status word register
TIMETAGMFTColdResetValue	uint16_t	BRM time tag / minor frame timer register
TIMETAGMFTForcedBits	uint16_t	BRM time tag / minor frame timer register
TIMETAGMFTForcedFlippedBits	uint16_t	BRM time tag / minor frame timer register
TIMETAGMFTReadMask	uint16_t	BRM time tag / minor frame timer register
TIMETAGMFTResetMask	uint16_t	BRM time tag / minor frame timer register
TIMETAGMFTResetValue	uint16_t	BRM time tag / minor frame timer register
TIMETAGMFTWriteMask	uint16_t	BRM time tag / minor frame timer register
TimeSource	*void	Time source object
ambaAhbPageAddress	uint32_t	AHB page address register
ambaInterruptSettings	uint32_t	B1553BRM interrupt settings register
ambaStatusControlReg	uint32_t	B1553BRM status/control register
config.bc.minorFrameTimerFreq	uint64_t	Frequency of the minor frame timer
config.bc.msgToMsgTimerFreq	uint64_t	Frequency of the Message to Message Timer
config.interruptHw	uint8_t	Hardware interrupt
config.interruptMsg	uint8_t	Message interrupt

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Name	Type	Description
config.littleEndian	uint8_t	Endianess of memory interface.
config.lock	uint8_t	Value of the Lock Signal. Locks Operation and Status Register
config.rt.timeTagFreq	uint64_t	Frequency of the Time Tag Counter
internals.bc.protocolPhase	uint32_t	Current Protocol Phase.
internals.bc.transferType	uint32_t	Current Transfer Type.
internals.milRetriesLeft	uint8_t	Counter for milbus transaction retry.
internals.milSelectedBus	uint8_t	Selected bus for the transaction.
internals.minorFrameReload	uint16_t	Value to reload the Minor Frame Timer with.
internals.rt.receivedOnBusA	uint8_t	If 0 the message has been received on bus B, otherwise on bus A.
internals.rt.timeTagCmd	uint16_t	Value of TimeTag register when the command was received.
internals.rt.timeTagStart	uint64_t	TimeTag Counter Start Time.
irqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller.
memAccess	temu_IfaceRef/ <unknown>	Memory access interface for accessing RAM (for DMA).

Interfaces

Name	Type	Description
AhbIface	AhbIface	AHB interface
DeviceIface	DeviceIface	Device interface.
MemAccessIface	MemAccessIface	
Mil1553DevIface	Mil1553DevIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Registers



Register support is currently experimental!

Register Bank Regs

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Register CONTROL

Description

BRM control register

Reset value

0x0000

Warm reset mask

0xffbf

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STEX	SBIT	SRST	BAEN	BBEN	ETCE	MSGTO	BUFM		-	BMC	BCEN	DYNBC	PPEN	INEN	XMTSW
rw	rw	rw	rw	rw	rw	rw	rw		-	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0		-	0	0	0	0	0	0

Field	Mask	Reset	Description
STEX	0x8000	0x0	Start execution
SBIT	0x4000	0x0	Start built-in test
SRST	0x2000	0x0	Software reset
BAEN	0x1000	0x0	Bus A enable
BBEN	0x0800	0x0	Bus B enable
ETCE	0x0400	0x0	External timer clock enable
MSGTO	0x0200	0x0	Message timeout
BUFM	0x0180	0x0	Buffer mode
BMC	0x0020	0x0	Bus monitor control
BCEN	0x0010	0x0	Broadcast enable
DYNBC	0x0008	0x0	Dynamic bus control acceptance
PPEN	0x0004	0x0	Ping pong enable
INEN	0x0002	0x0	Interrupt log list enable
XMTSW	0x0001	0x0	Transmit status word

Register OPSTAT

Description

BRM operation and status register

Reset value

0x0000

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Warm reset mask

0xffdf

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTA					RTPTY	MSEL		ABSTD	LOCK	-	SSYSF	EX	TAPF	READY	TERACT
rw					rw	rw		rw	ro	-	ro	ro	ro	ro	ro
0					0	0		0	0	-	0	0	0	0	0

Field	Mask	Reset	Description
RTA	0xf800	0x0	Remote terminal address
RTPTY	0x0400	0x0	RT address parity
MSEL	0x0300	0x0	Mode select
ABSTD	0x0080	0x0	1553A or 1553B support
LOCK	0x0040	0x0	LOCK status
SSYSF	0x0010	0x0	SSYSF status
EX	0x0008	0x0	Core executing
TAPF	0x0004	0x0	RT address parity fail
READY	0x0002	0x0	READY status
TERACT	0x0001	0x0	Terminal active

Register CURRENTCOMMAND

Description

BRM current command register

Reset value

0x0000

Warm reset mask

0xffff

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC															
ro															
0															

Field	Mask	Reset	Description
CC	0xffff	0x0	Current command

Register INTMASK

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Description

BRM interrupt mask

Reset value

0x0000

Warm reset mask

0xefbf

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAF	WRAPF	TAPF	-	MERR	SUBAD	BDRCV	IXEQ0	ILLCMDRT	-	EOL	ILLCMDBC	ILLOP	RTF	CBA	MBC
rw	rw	rw	-	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw
0	0	0	-	0	0	0	0	0	-	0	0	0	0	0	0

Field	Mask	Reset	Description
DMAF	0x8000	0x0	DMA fail interrupt
WRAPF	0x4000	0x0	Wrap fail interrupt
TAPF	0x2000	0x0	Terminal address parity fail interrupt
MERR	0x0800	0x0	Message error interrupt
SUBAD	0x0400	0x0	Subaddress accessed interrupt
BDRCV	0x0200	0x0	Broadcast command received interrupt
IXEQ0	0x0100	0x0	Index equal zero interrupt
ILLCMDRT	0x0080	0x0	RT illegal command interrupt
EOL	0x0020	0x0	BC end of list interrupt
ILLCMDBC	0x0010	0x0	BC illogical command interrupt
ILLOP	0x0008	0x0	BC illogical opcode interrupt
RTF	0x0004	0x0	BC retry fail interrupt
CBA	0x0002	0x0	BC command block accessed interrupt
MBC	0x0001	0x0	BM monitor block counter interrupt

Register PENDINT

Description

BRM pending interrupt

Reset value

0x0000

Warm reset mask

0xefbf

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAF	WRAPF	TAPF	-	MERR	SUBAD	BDRCV	IXEQ0	ILLCMDRT	-	EOL	ILLCMDBC	ILLOP	RTF	CBA	MBC
rw	rw	rw	-	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw
0	0	0	-	0	0	0	0	0	-	0	0	0	0	0	0

Field	Mask	Reset	Description
DMAF	0x8000	0x0	DMA fail interrupt
WRAPF	0x4000	0x0	Wrap fail interrupt
TAPF	0x2000	0x0	Terminal address parity fail interrupt
MERR	0x0800	0x0	Message error interrupt
SUBAD	0x0400	0x0	Subaddress accessed interrupt
BDRCV	0x0200	0x0	Broadcast command received interrupt
IXEQ0	0x0100	0x0	Index equal zero interrupt
ILLCMDRT	0x0080	0x0	RT illegal command interrupt
EOL	0x0020	0x0	BC end of list interrupt
ILLCMDBC	0x0010	0x0	BC illogical command interrupt
ILLOP	0x0008	0x0	BC illogical opcode interrupt
RTF	0x0004	0x0	BC retry fail interrupt
CBA	0x0002	0x0	BC command block accessed interrupt
MBC	0x0001	0x0	BM monitor block counter interrupt

Register INTPTR

Description

BRM interrupt pointer

Reset value

0x0000

Warm reset mask

0xffff

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTA															
rw															
0															

Field	Mask	Reset	Description
INTA	0xffff	0x0	Interrupt pointer

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Register BITREG

Description

BRM built-in test register

Reset value

0x0000

Warm reset mask

0xecff

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAF	WRAPF	TAPF	-	CHAF	CHBF	-	BITW								
rw	rw	rw	-	rw	rw	-	rw								
0	0	0	-	0	0	-	0								

Field	Mask	Reset	Description
DMAF	0x8000	0x0	DMA fail status
WRAPF	0x4000	0x0	Wrap fail status
TAPF	0x2000	0x0	Terminal address parity fail status
CHAF	0x0800	0x0	Channel A failure
CHBF	0x0400	0x0	Channel B failure
BITW	0x00ff	0x0	Built-in test word

Register TIMETAGMFT

Description

BRM time tag / minor frame timer register

Reset value

0x0000

Warm reset mask

0xffff

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
rw															
0															

Field	Mask	Reset	Description
VALUE	0xffff	0x0	Time tag or minor frame timer value

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Register DESCCMDPTR

Description

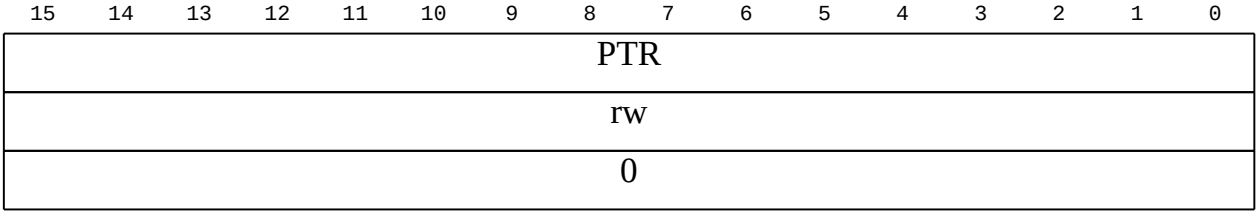
BRM descriptor/command block pointer register

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
PTR	0xffff	0x0	Descriptor or command block pointer

Register STATUSWORD

Description

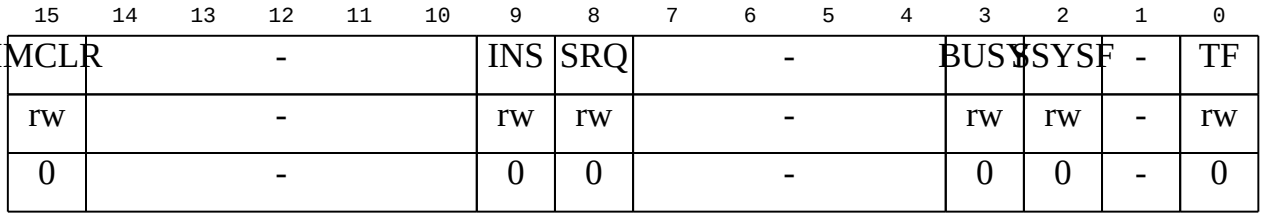
BRM 1553A/B status word register

Reset value

0x0000

Warm reset mask

0x830d



Field	Mask	Reset	Description
IMCLR	0x8000	0x0	Immediate clear enable
INS	0x0200	0x0	Instrumentation
SRQ	0x0100	0x0	Service request
BUSY	0x0008	0x0	Busy
SSYSF	0x0004	0x0	Subsystem flag
TF	0x0001	0x0	Terminal flag

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register INITCOUNT

Description

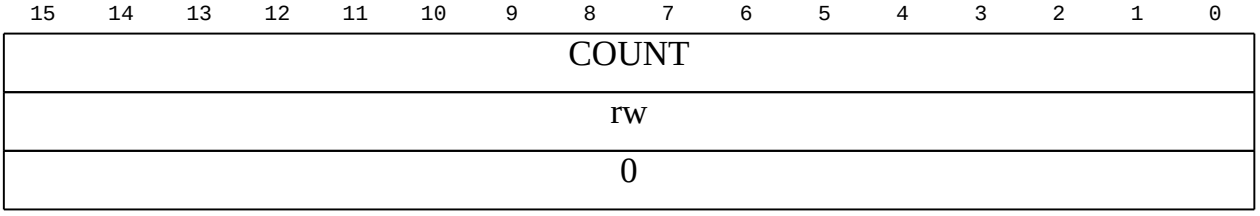
BRM initialization count register

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
COUNT	0xffff	0x0	Initialization count

Register ENHANCED

Description

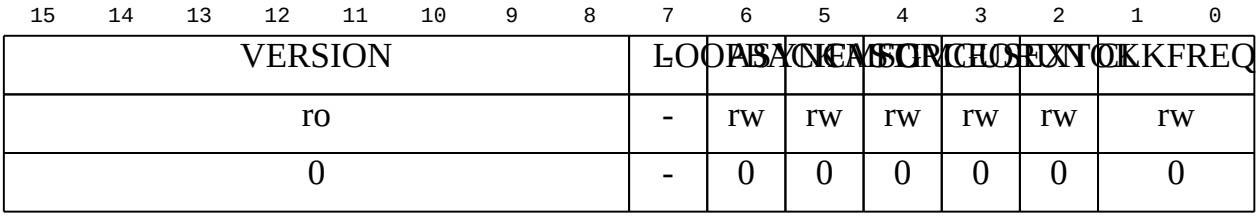
BRM enhanced features register

Reset value

0x0000

Warm reset mask

0xff7f



Field	Mask	Reset	Description
VERSION	0xff00	0x0	Core version
LOOPBACK	0x0040	0x0	Loopback enable
ASYNCMSG	0x0020	0x0	Asynchronous message enable
FASTIMG	0x0010	0x0	Fast inter-message gap
FORCEORUN	0x0008	0x0	Force overrun
USEXTOK	0x0004	0x0	Use external verification

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Field	Mask	Reset	Description
CLKFREQ	0x0003	0x0	Core operating frequency

Register AMBASTATCTRL

Description

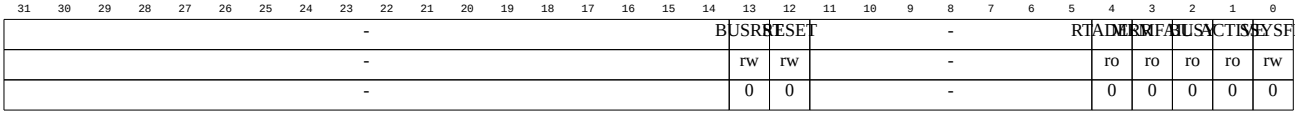
B1553BRM status/control register

Reset value

0x00000000

Warm reset mask

0x0000301f



Field	Mask	Reset	Description
BUSRST	0x00002000	0x0	Bus reset mode code received
RESET	0x00001000	0x0	Software reset
RTADERR	0x00000010	0x0	RT address error
MEMFAIL	0x00000008	0x0	Memory failure
BUSY	0x00000004	0x0	Busy
ACTIVE	0x00000002	0x0	Active
SSYSFN	0x00000001	0x0	Subsystem flag input

Register AMBAIRQ

Description

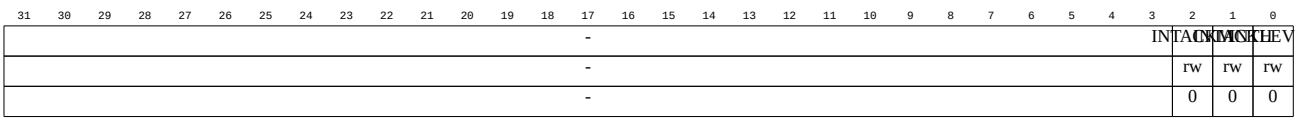
B1553BRM interrupt settings register

Reset value

0x00000000

Warm reset mask

0x00000007



Field	Mask	Reset	Description
INTACKM	0x00000004	0x0	Message interrupt acknowledge

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Field	Mask	Reset	Description
INTACKH	0x00000002	0x0	Hardware interrupt acknowledge
INTLEVEL	0x00000001	0x0	Interrupt level

Register AHBPAGE

Description

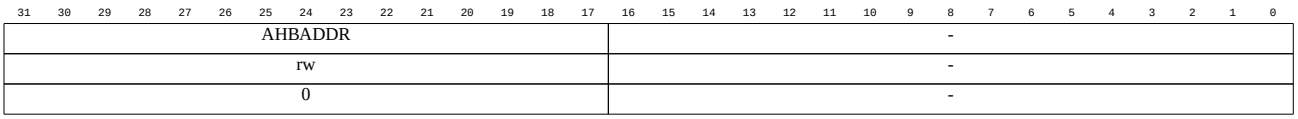
AHB page address register

Reset value

0x00000000

Warm reset mask

0xfffe0000



Field	Mask	Reset	Description
AHBADDR	0xfffe0000	0x0	AHB page address

Register RTLEGAL

Description

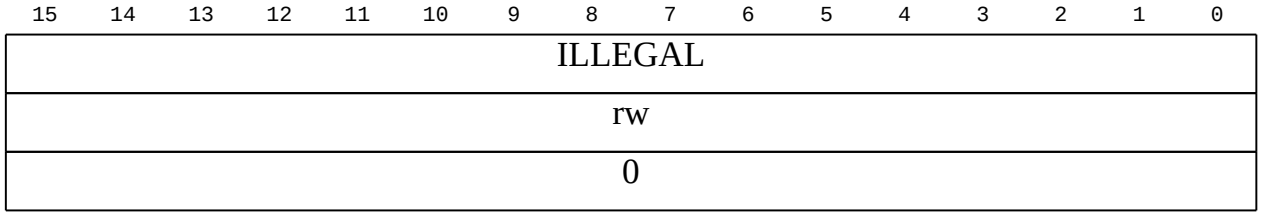
RT legalization register

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

RT legalization register

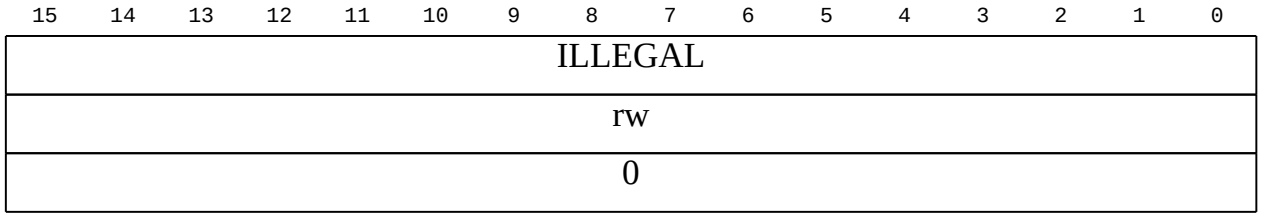
The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

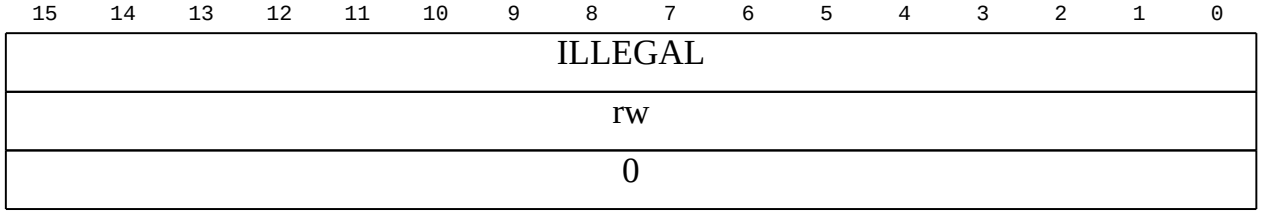
RT legalization register

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

RT legalization register

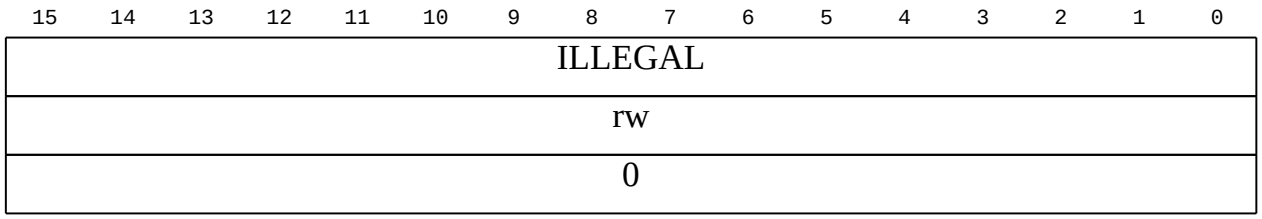
Reset value

0x0000

Warm reset mask

0xffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

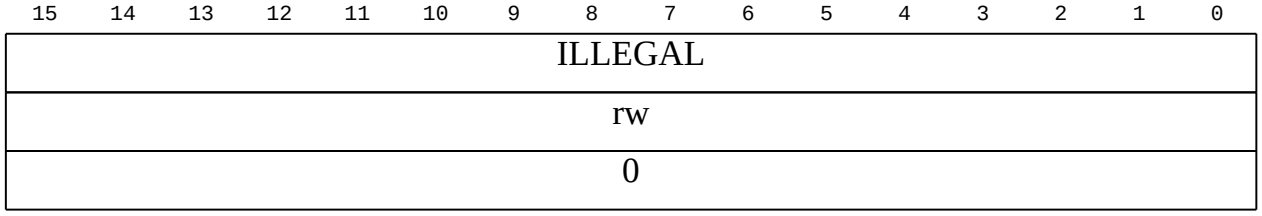
RT legalization register

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

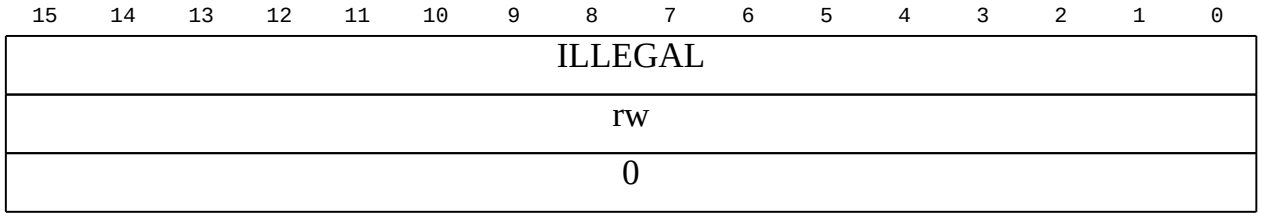
RT legalization register

Reset value

0x0000

Warm reset mask

0xffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

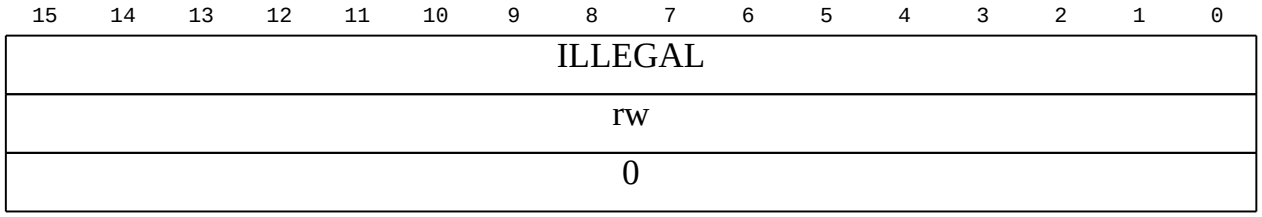
RT legalization register

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

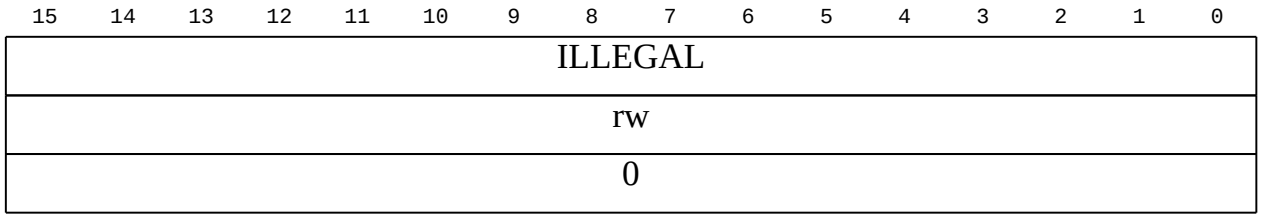
RT legalization register

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

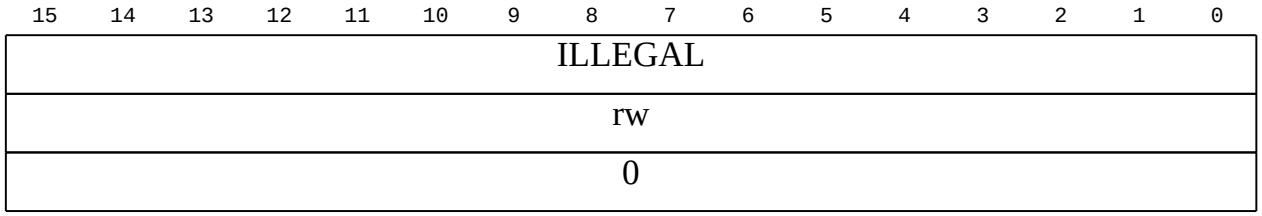
RT legalization register

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

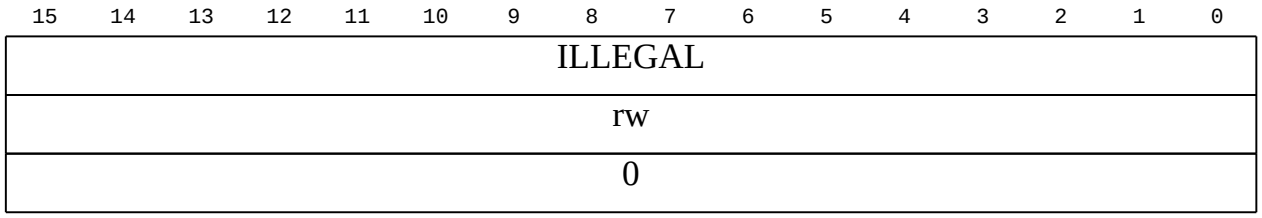
RT legalization register

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

RT legalization register

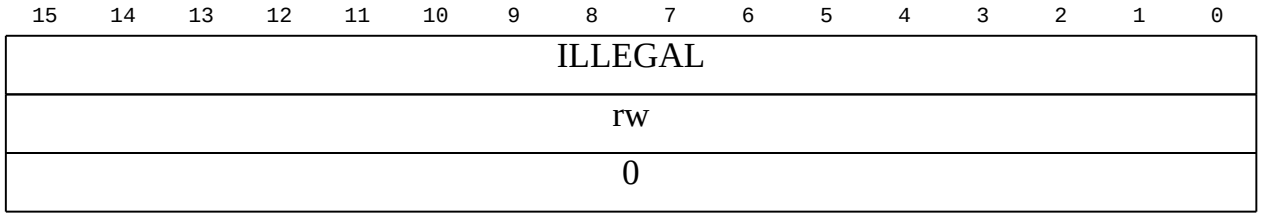
Reset value

0x0000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffff



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

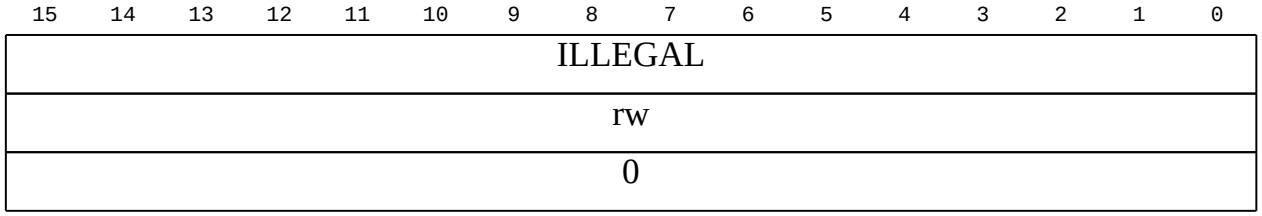
RT legalization register

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

RT legalization register

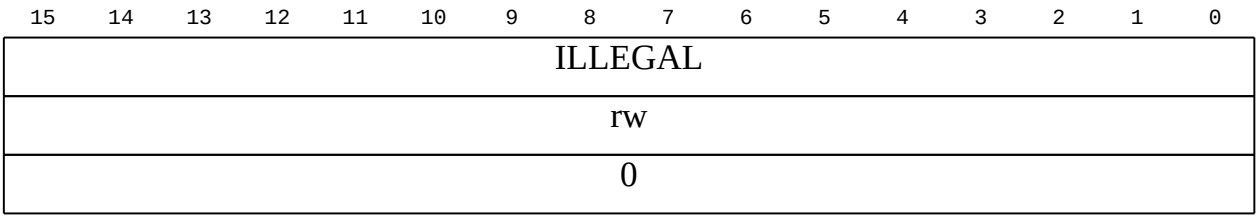
Reset value

0x0000

Warm reset mask

0xffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

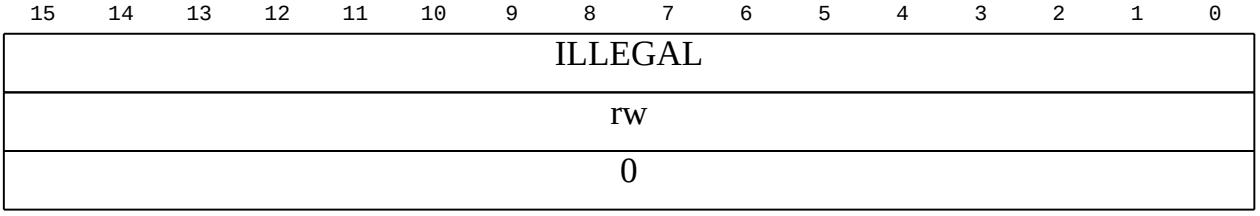
RT legalization register

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

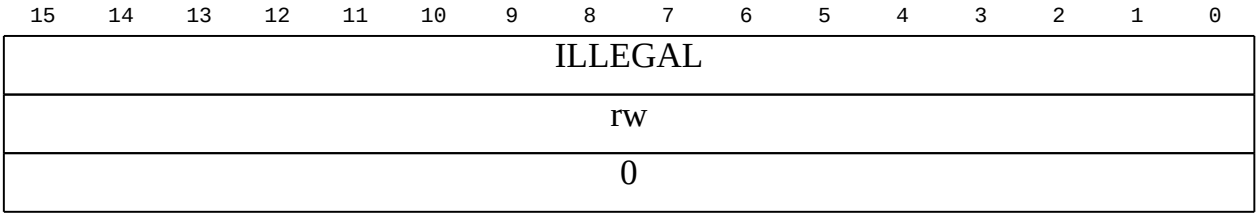
RT legalization register

Reset value

0x0000

Warm reset mask

0xffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Register RTLEGAL

Description

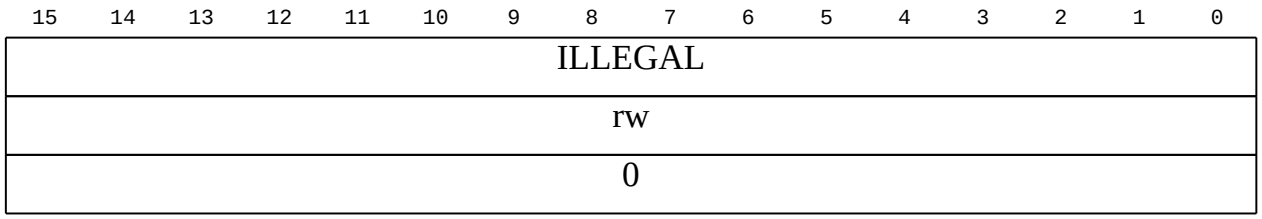
RT legalization register

Reset value

0x0000

Warm reset mask

0xffff



Field	Mask	Reset	Description
ILLEGAL	0xffff	0x0	Command illegalization bits

Commands

Name	Description
delete	Dispose instance of B1553BRM

9.2.4. Limitations

The following deviations from real hardware are known to exist with this model:

- Monitoring mode is not supported, use the TEMU API instead.

9.3. CANOC

The CAN_OC device is part of the OpenCores and the GRLIB IP libraries. It is available in `libTEMUOpenCores.so`.

9.3.1. Loading the Plugin

```
import OpenCores
```

9.3.2. Configuration

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

There are two configuration parameters in the CAN device. Firstly the `config.interrupt` property can be set to influence the interrupt that is raised with the IRQ controller. Setting that property also updates the AHB PnP info.

The second configuration property is `config.infiniteSpeed`. If that property is set, messages will be sent immediately instead of being scheduled.

The device should be connected to an interrupt controller and a CAN bus, to work properly.

9.3.3. @CAN_OC Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @CAN_OC
new	Create new instance of CAN_OC

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.3.4. CAN_OC Reference

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Properties

Name	Type	Description
BASIC_ACCEPT_CODEColdResetValue	uint8_t	Accept code register for BasicCAN mode
BASIC_ACCEPT_CODEForcedBits	uint8_t	Accept code register for BasicCAN mode
BASIC_ACCEPT_CODEForcedFlippedBits	uint8_t	Accept code register for BasicCAN mode
BASIC_ACCEPT_CODEReadMask	uint8_t	Accept code register for BasicCAN mode
BASIC_ACCEPT_CODEResetMask	uint8_t	Accept code register for BasicCAN mode
BASIC_ACCEPT_CODEResetValue	uint8_t	Accept code register for BasicCAN mode
BASIC_ACCEPT_CODEWriteMask	uint8_t	Accept code register for BasicCAN mode
BASIC_ACCEPT_MASKColdResetValue	uint8_t	Accept mask register for BasicCAN mode
BASIC_ACCEPT_MASKForcedBits	uint8_t	Accept mask register for BasicCAN mode
BASIC_ACCEPT_MASKForcedFlippedBits	uint8_t	Accept mask register for BasicCAN mode
BASIC_ACCEPT_MASKReadMask	uint8_t	Accept mask register for BasicCAN mode
BASIC_ACCEPT_MASKResetMask	uint8_t	Accept mask register for BasicCAN mode
BASIC_ACCEPT_MASKResetValue	uint8_t	Accept mask register for BasicCAN mode
BASIC_ACCEPT_MASKWriteMask	uint8_t	Accept mask register for BasicCAN mode
BASIC_CONTROLColdResetValue	uint8_t	Control register for BasicCAN mode
BASIC_CONTROLForcedBits	uint8_t	Control register for BasicCAN mode
BASIC_CONTROLForcedFlippedBits	uint8_t	Control register for BasicCAN mode
BASIC_CONTROLReadMask	uint8_t	Control register for BasicCAN mode

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BASIC_CONTROLResetMask	uint8_t	Control register for BasicCAN mode
BASIC_CONTROLResetValue	uint8_t	Control register for BasicCAN mode
BASIC_CONTROLWriteMask	uint8_t	Control register for BasicCAN mode
CLOCKDIVIDERColdResetValue	uint8_t	Clock divider register
CLOCKDIVIDERForcedBits	uint8_t	Clock divider register
CLOCKDIVIDERForcedFlippedBits	uint8_t	Clock divider register
CLOCKDIVIDERReadMask	uint8_t	Clock divider register
CLOCKDIVIDERResetMask	uint8_t	Clock divider register
CLOCKDIVIDERResetValue	uint8_t	Clock divider register
CLOCKDIVIDERWriteMask	uint8_t	Clock divider register
COMMANDColdResetValue	uint8_t	Command register
COMMANDForcedBits	uint8_t	Command register
COMMANDForcedFlippedBits	uint8_t	Command register
COMMANDReadMask	uint8_t	Command register
COMMANDResetMask	uint8_t	Command register
COMMANDResetValue	uint8_t	Command register
COMMANDWriteMask	uint8_t	Command register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
INTERRUPTColdResetValue	uint8_t	Interrupt register
INTERRUPTForcedBits	uint8_t	Interrupt register
INTERRUPTForcedFlippedBits	uint8_t	Interrupt register
INTERRUPTReadMask	uint8_t	Interrupt register
INTERRUPTResetMask	uint8_t	Interrupt register
INTERRUPTResetValue	uint8_t	Interrupt register
INTERRUPTWriteMask	uint8_t	Interrupt register
LocalName	*char	Local name (in component, if applicable)

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
PELICAN_ARB_LOST_CAPTUREColdResetValue	uint8_t	Arbitration lost capture register
PELICAN_ARB_LOST_CAPTUREForcedBits	uint8_t	Arbitration lost capture register
PELICAN_ARB_LOST_CAPTUREForcedFlippedBits	uint8_t	Arbitration lost capture register
PELICAN_ARB_LOST_CAPTUREReadMask	uint8_t	Arbitration lost capture register
PELICAN_ARB_LOST_CAPTUREResetMask	uint8_t	Arbitration lost capture register
PELICAN_ARB_LOST_CAPTUREResetValue	uint8_t	Arbitration lost capture register
PELICAN_ARB_LOST_CAPTUREWriteMask	uint8_t	Arbitration lost capture register
PELICAN_ERR_CODE_CAPTUREColdResetValue	uint8_t	Error code capture register
PELICAN_ERR_CODE_CAPTUREForcedBits	uint8_t	Error code capture register
PELICAN_ERR_CODE_CAPTUREForcedFlippedBits	uint8_t	Error code capture register
PELICAN_ERR_CODE_CAPTUREReadMask	uint8_t	Error code capture register
PELICAN_ERR_CODE_CAPTUREResetMask	uint8_t	Error code capture register
PELICAN_ERR_CODE_CAPTUREResetValue	uint8_t	Error code capture register
PELICAN_ERR_CODE_CAPTUREWriteMask	uint8_t	Error code capture register
PELICAN_ERR_WARN_LIMITColdResetValue	uint8_t	Error warning limit register
PELICAN_ERR_WARN_LIMITForcedBits	uint8_t	Error warning limit register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
PELICAN_ERR_WARN_LIMITForcedFlippedBits	uint8_t	Error warning limit register
PELICAN_ERR_WARN_LIMITReadMask	uint8_t	Error warning limit register
PELICAN_ERR_WARN_LIMITResetMask	uint8_t	Error warning limit register
PELICAN_ERR_WARN_LIMITResetValue	uint8_t	Error warning limit register
PELICAN_ERR_WARN_LIMITWriteMask	uint8_t	Error warning limit register
PELICAN_INTERRUPT_ENABLEColdResetValue	uint8_t	Interrupt enable register for PeliCAN mode
PELICAN_INTERRUPT_ENABLEForcedBits	uint8_t	Interrupt enable register for PeliCAN mode
PELICAN_INTERRUPT_ENABLEForcedFlippedBits	uint8_t	Interrupt enable register for PeliCAN mode
PELICAN_INTERRUPT_ENABLEReadMask	uint8_t	Interrupt enable register for PeliCAN mode
PELICAN_INTERRUPT_ENABLEResetMask	uint8_t	Interrupt enable register for PeliCAN mode
PELICAN_INTERRUPT_ENABLEResetValue	uint8_t	Interrupt enable register for PeliCAN mode
PELICAN_INTERRUPT_ENABLEWriteMask	uint8_t	Interrupt enable register for PeliCAN mode
PELICAN_MODEColdResetValue	uint8_t	Mode register for PeliCAN mode
PELICAN_MODEForcedBits	uint8_t	Mode register for PeliCAN mode
PELICAN_MODEForcedFlippedBits	uint8_t	Mode register for PeliCAN mode
PELICAN_MODEReadMask	uint8_t	Mode register for PeliCAN mode
PELICAN_MODEResetMask	uint8_t	Mode register for PeliCAN mode
PELICAN_MODEResetValue	uint8_t	Mode register for PeliCAN mode
PELICAN_MODEWriteMask	uint8_t	Mode register for PeliCAN mode
PELICAN_RX_ERR_COUNTERColdResetValue	uint8_t	RX error counter register
PELICAN_RX_ERR_COUNTERForcedBits	uint8_t	RX error counter register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
PELICAN_RX_ERR_COUNTERForcedFlippedBits	uint8_t	RX error counter register
PELICAN_RX_ERR_COUNTERReadMask	uint8_t	RX error counter register
PELICAN_RX_ERR_COUNTERResetMask	uint8_t	RX error counter register
PELICAN_RX_ERR_COUNTERResetValue	uint8_t	RX error counter register
PELICAN_RX_ERR_COUNTERWriteMask	uint8_t	RX error counter register
PELICAN_RX_MSG_COUNTERColdResetValue	uint8_t	RX message counter register
PELICAN_RX_MSG_COUNTERForcedBits	uint8_t	RX message counter register
PELICAN_RX_MSG_COUNTERForcedFlippedBits	uint8_t	RX message counter register
PELICAN_RX_MSG_COUNTERReadMask	uint8_t	RX message counter register
PELICAN_RX_MSG_COUNTERResetMask	uint8_t	RX message counter register
PELICAN_RX_MSG_COUNTERResetValue	uint8_t	RX message counter register
PELICAN_RX_MSG_COUNTERWriteMask	uint8_t	RX message counter register
PELICAN_TX_ERR_COUNTERColdResetValue	uint8_t	TX error counter register
PELICAN_TX_ERR_COUNTERForcedBits	uint8_t	TX error counter register
PELICAN_TX_ERR_COUNTERForcedFlippedBits	uint8_t	TX error counter register
PELICAN_TX_ERR_COUNTERReadMask	uint8_t	TX error counter register
PELICAN_TX_ERR_COUNTERResetMask	uint8_t	TX error counter register
PELICAN_TX_ERR_COUNTERResetValue	uint8_t	TX error counter register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
PELICAN_TX_ERR_COUNTERWriteMask	uint8_t	TX error counter register
PELICAN_TX_FIColdResetValue	uint8_t	TX frame info register for PeliCAN mode
PELICAN_TX_FIForcedBits	uint8_t	TX frame info register for PeliCAN mode
PELICAN_TX_FIForcedFlippedBits	uint8_t	TX frame info register for PeliCAN mode
PELICAN_TX_FIReadMask	uint8_t	TX frame info register for PeliCAN mode
PELICAN_TX_FIResetMask	uint8_t	TX frame info register for PeliCAN mode
PELICAN_TX_FIResetValue	uint8_t	TX frame info register for PeliCAN mode
PELICAN_TX_FIWriteMask	uint8_t	TX frame info register for PeliCAN mode
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
STATUSColdResetValue	uint8_t	Status register
STATUSForcedBits	uint8_t	Status register
STATUSForcedFlippedBits	uint8_t	Status register
STATUSReadMask	uint8_t	Status register
STATUSResetMask	uint8_t	Status register
STATUSResetValue	uint8_t	Status register
STATUSWriteMask	uint8_t	Status register
TimeSource	*void	Time source object
basiccan.acceptCode	uint8_t	Accept code register for BasicCAN mode
basiccan.acceptMask	uint8_t	Accept mask register for BasicCAN mode
basiccan.ctrl	uint8_t	Control register for BasicCAN mode
basiccan.txID	[uint8_t; 2]	TxID register for BasicCAN mode
bus	temu_IfaceRef/ <unknown>	CAN bus the device is connected to.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
busTiming	[uint8_t; 2]	Bus timing register
clockDivider	uint8_t	Clock divider register
command	uint8_t	Command register
config.infiniteSpeed	uint8_t	Enable infinite speed mode (no delays when sending messages).
config.interrupt	uint8_t	External interrupt raised with IRQ controller.
fifo.data	[uint8_t; 64]	RX FIFO data buffer.
fifo.start	uint32_t	RX FIFO buffer start location.
fifo.usage	uint32_t	RX FIFO buffer usage.
interrupt	uint8_t	Interrupt register
irqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller.
pelican.acceptCode	[uint8_t; 4]	Accept code register for PeliCAN mode
pelican.acceptMask	[uint8_t; 4]	Accept mask register for PeliCAN mode
pelican.arbLostCaputure	uint8_t	Arbitration lost capture register
pelican.errCodeCapture	uint8_t	Error code capture register
pelican.errWarnLimit	uint8_t	Error warning limit register
pelican.interruptEnable	uint8_t	Interrupt enable register for PeliCAN mode
pelican.mode	uint8_t	Mode register for PeliCAN mode
pelican.rxErrCounter	uint8_t	RX error counter register
pelican.rxMsgCounter	uint8_t	RX message counter register
pelican.txErrCounter	uint8_t	TX error counter register
pelican.txFI	uint8_t	TX frame info register for PeliCAN mode
pelican.txID	[uint8_t; 4]	TxID register for PeliCAN mode
status	uint8_t	Status register
txData	[uint8_t; 8]	TX data buffer

Interfaces

Name	Type	Description
AhbIface	AhbIface	AHB interface

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Name	Type	Description
CanDevIface	CanDevIface	CAN device interface.
DeviceIface	DeviceIface	Device interface.
MemAccessIface	MemAccessIface	Memory access interface for memory mapped registers.
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Registers



Register support is currently experimental!

Register Bank BasicCAN

Register BASIC_CONTROL

Description

Control register for BasicCAN mode

Reset value

0x00

Warm reset mask

0x1f

7	6	5	4	3	2	1	0
-			DOIE	EIE	TIE	RIE	RR
-			rw	rw	rw	rw	rw
-			0	0	0	0	0

Field	Mask	Reset	Description
DOIE	0x10	0x0	Data overrun interrupt enable
EIE	0x08	0x0	Error interrupt enable
TIE	0x04	0x0	Transmit interrupt enable
RIE	0x02	0x0	Receive interrupt enable
RR	0x01	0x0	Reset request

Register BASIC_ACCEPT_CODE

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Description

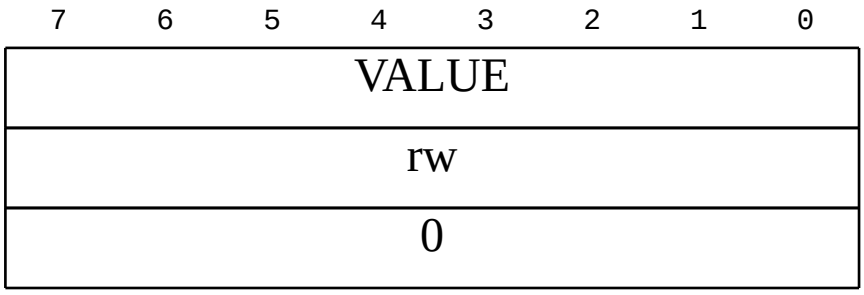
Accept code register for BasicCAN mode

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register BASIC_ACCEPT_MASK

Description

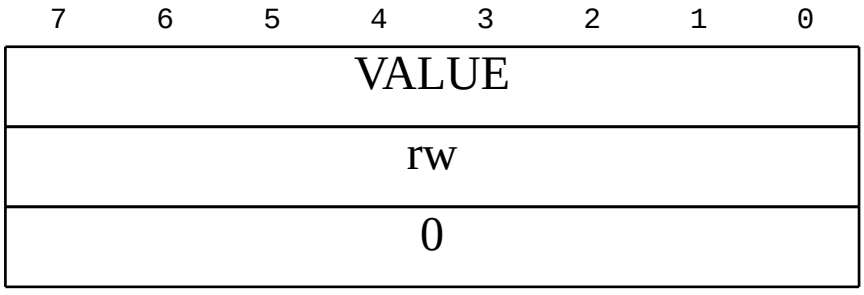
Accept mask register for BasicCAN mode

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register BASIC_TXID

Description

TxID register for BasicCAN mode

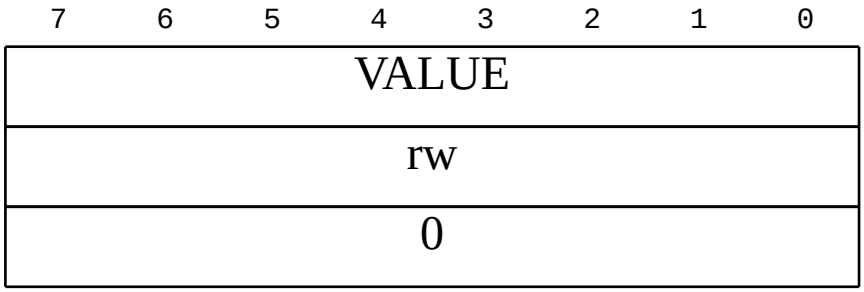
The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register BASIC_TXID

Description

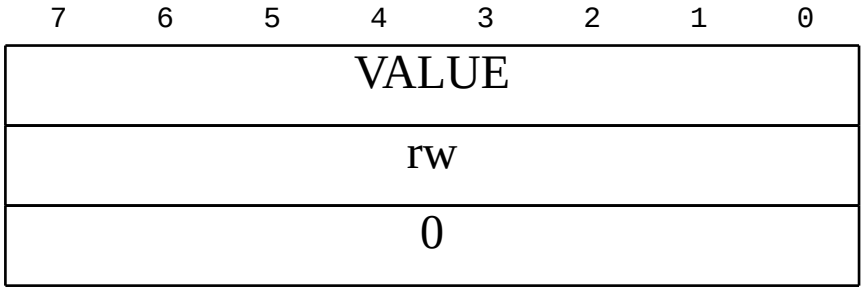
TxID register for BasicCAN mode

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register Bank DefaultRegs

Register COMMAND

Description

Command register

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Reset value

0x00

Warm reset mask

0x00

7	6	5	4	3	2	1	0
-			SRR	CDO	RRB	AT	TR
-			WO	WO	WO	WO	WO
-			-	-	-	-	-

Field	Mask	Reset	Description
SRR	0x10	-	Self reception request
CDO	0x08	-	Clear data overrun
RRB	0x04	-	Release receive buffer
AT	0x02	-	Abort transmission
TR	0x01	-	Transmission request

Register STATUS

Description

Status register

Reset value

0x00

Warm reset mask

0xff

7	6	5	4	3	2	1	0
BS	ES	TS	RS	TCS	TBS	DOS	RBS
ro	ro	ro	ro	ro	ro	ro	ro
0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
BS	0x80	0x0	Bus status
ES	0x40	0x0	Error status
TS	0x20	0x0	Transmit status

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Field	Mask	Reset	Description
RS	0x10	0x0	Receive status
TCS	0x08	0x0	Transmission complete status
TBS	0x04	0x0	Transmit buffer status
DOS	0x02	0x0	Data overrun status
RBS	0x01	0x0	Receive buffer status

Register INTERRUPT

Description

Interrupt register

Reset value

0x00

Warm reset mask

0xff

7	6	5	4	3	2	1	0
BEI	ALI	EPI	WUI	DOI	EI	TI	RI
ro	ro	ro	ro	ro	ro	ro	ro
0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
BEI	0x80	0x0	Bus error interrupt
ALI	0x40	0x0	Arbitration lost interrupt
EPI	0x20	0x0	Error passive interrupt
WUI	0x10	0x0	Wake-up interrupt
DOI	0x08	0x0	Data overrun interrupt
EI	0x04	0x0	Error interrupt
TI	0x02	0x0	Transmit interrupt
RI	0x01	0x0	Receive interrupt

Register CLOCKDIVIDER

Description

Clock divider register

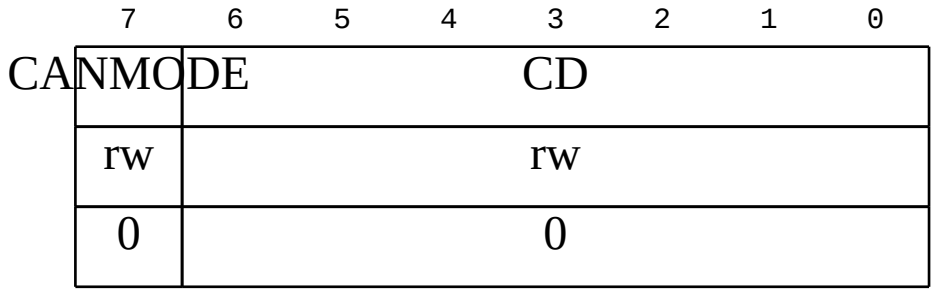
The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
CANMODE	0x80	0x0	CAN mode select
CD	0x7f	0x0	Clock divider

Register BUSTIMING

Description

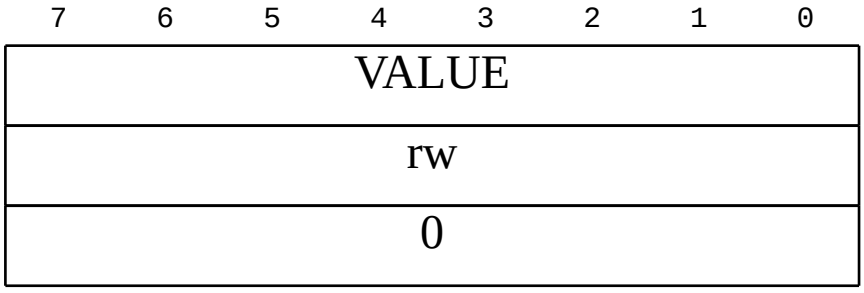
Bus timing register

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register BUSTIMING

Description

Bus timing register

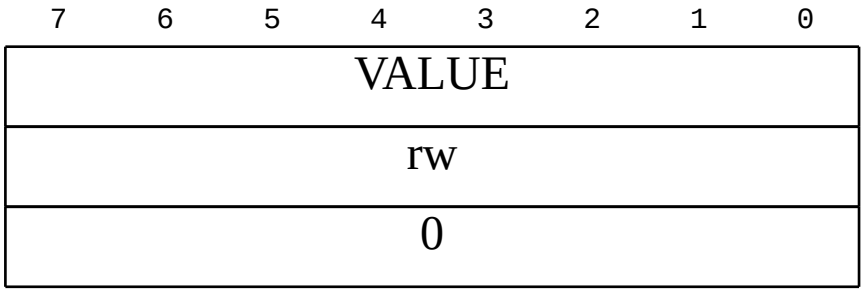
The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register TXDATA

Description

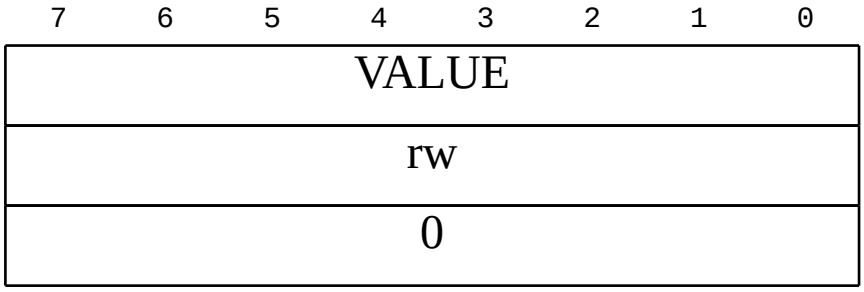
TX data buffer

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register TXDATA

Description

TX data buffer

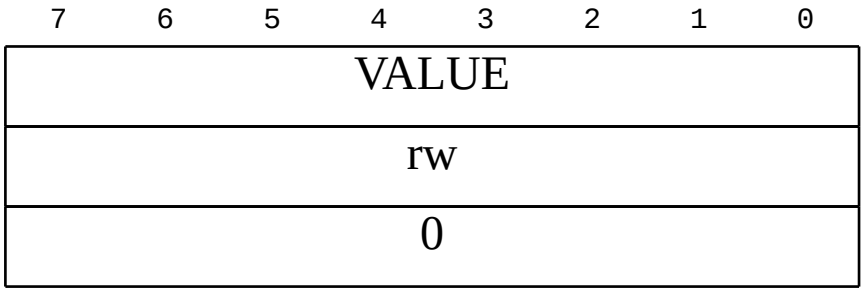
Reset value

0x00

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Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register TXDATA

Description

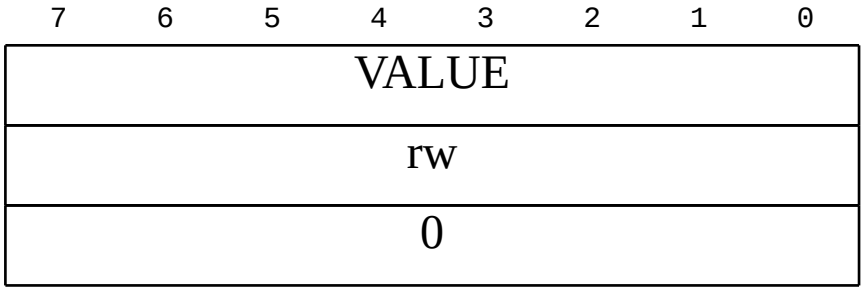
TX data buffer

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register TXDATA

Description

TX data buffer

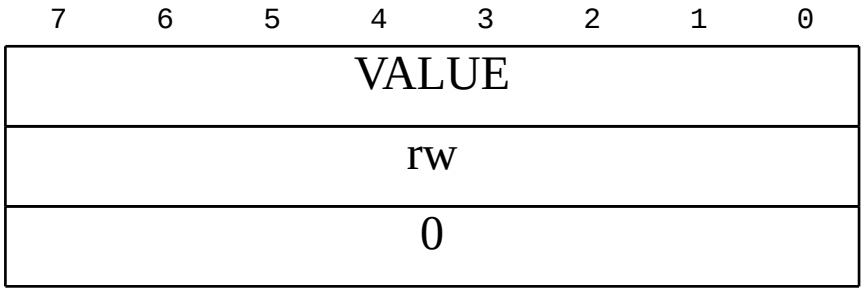
Reset value

0x00

Warm reset mask

0xff

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Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register TXDATA

Description

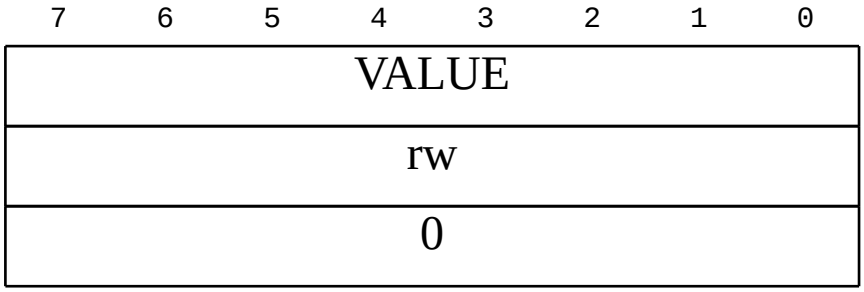
TX data buffer

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register TXDATA

Description

TX data buffer

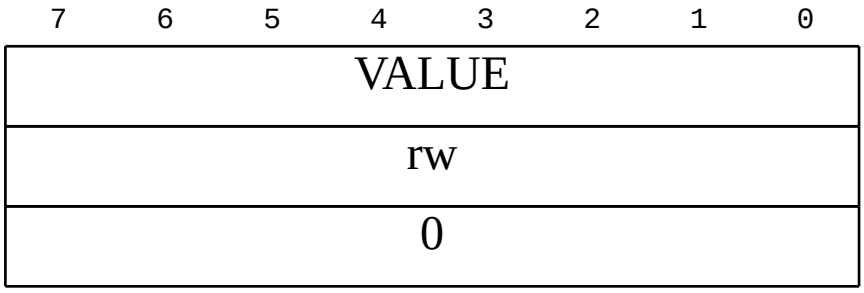
Reset value

0x00

Warm reset mask

0xff

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Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register TXDATA

Description

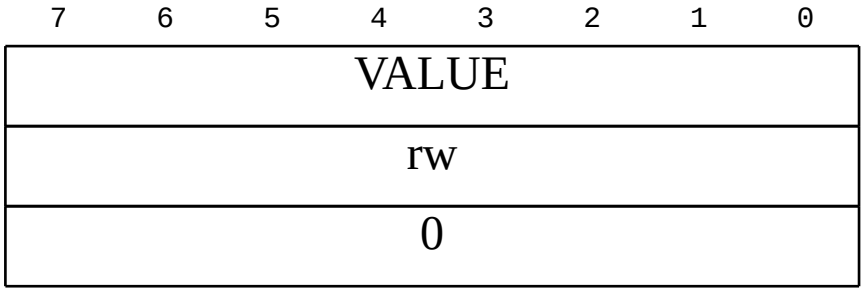
TX data buffer

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register TXDATA

Description

TX data buffer

Reset value

0x00

Warm reset mask

0xff

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7	6	5	4	3	2	1	0
VALUE							
rw							
0							

Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register Bank PeliCAN

Register PELICAN_MODE

Description

Mode register for PeliCAN mode

Reset value

0x00

Warm reset mask

0x1f

7	6	5	4	3	2	1	0
-			SM	AFM	STM	LOM	RM
-			rw	rw	rw	rw	rw
-			0	0	0	0	0

Field	Mask	Reset	Description
SM	0x10	0x0	Sleep mode
AFM	0x08	0x0	Acceptance filter mode
STM	0x04	0x0	Self test mode
LOM	0x02	0x0	Listen only mode
RM	0x01	0x0	Reset mode

Register PELICAN_INTERRUPT_ENABLE

Description

Interrupt enable register for PeliCAN mode

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Reset value

0x00

Warm reset mask

0xff

7	6	5	4	3	2	1	0
BEIE	ALIE	EPIE	WUIE	DOIE	EIE	TIE	RIE
rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
BEIE	0x80	0x0	Bus error interrupt enable
ALIE	0x40	0x0	Arbitration lost interrupt enable
EPIE	0x20	0x0	Error passive interrupt enable
WUIE	0x10	0x0	Wake-up interrupt enable
DOIE	0x08	0x0	Data overrun interrupt enable
EIE	0x04	0x0	Error interrupt enable
TIE	0x02	0x0	Transmit interrupt enable
RIE	0x01	0x0	Receive interrupt enable

Register PELICAN_ARB_LOST_CAPTURE

Description

Arbitration lost capture register

Reset value

0x00

Warm reset mask

0xff

7	6	5	4	3	2	1	0
VALUE							
rw							
0							

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Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_ERR_CODE_CAPTURE

Description

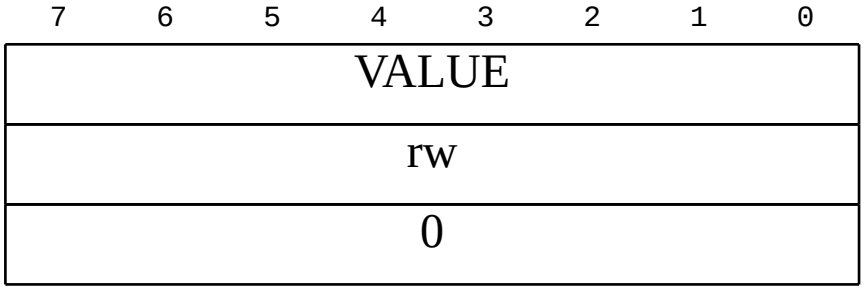
Error code capture register

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_ERR_WARN_LIMIT

Description

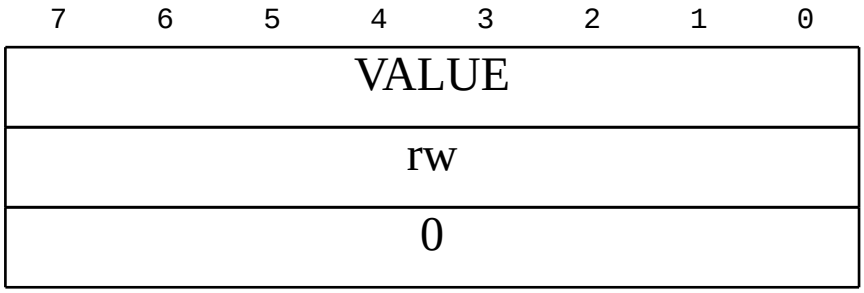
Error warning limit register

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

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Register PELICAN_RX_ERR_COUNTER

Description

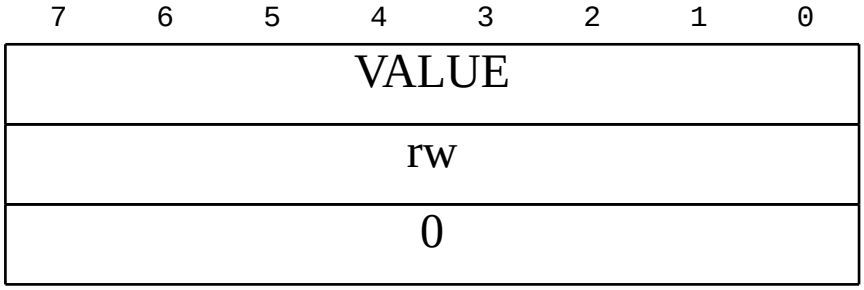
RX error counter register

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_TX_ERR_COUNTER

Description

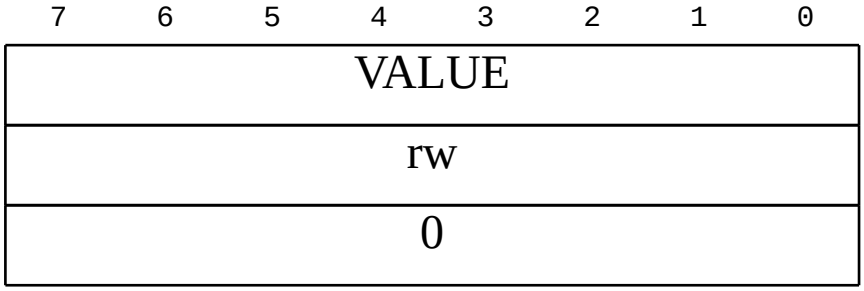
TX error counter register

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_TX_FI

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Description

TX frame info register for PeliCAN mode

Reset value

0x00

Warm reset mask

0xcf

7	6	5	4	3	2	1	0
FF	RTR	-		DLC			
rw	rw	-		rw			
0	0	-		0			

Field	Mask	Reset	Description
FF	0x80	0x0	Frame format
RTR	0x40	0x0	Remote transmission request
DLC	0x0f	0x0	Data length code

Register PELICAN_RX_MSG_COUNTER

Description

RX message counter register

Reset value

0x00

Warm reset mask

0xff

7	6	5	4	3	2	1	0
VALUE							
rw							
0							

Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_ACCEPT_CODE

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Description

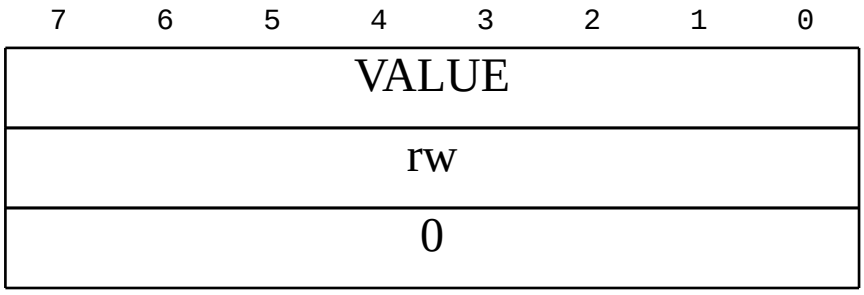
Accept code register for PeliCAN mode

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_ACCEPT_CODE

Description

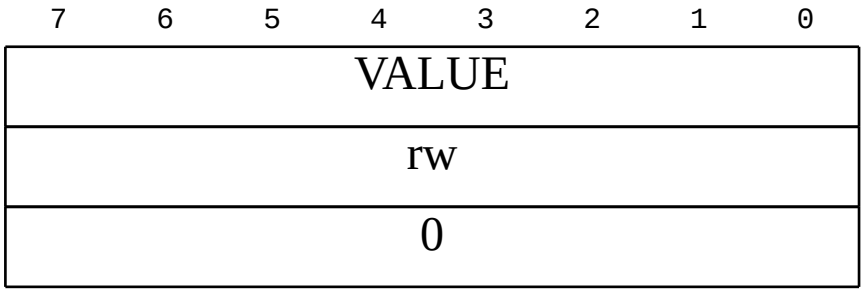
Accept code register for PeliCAN mode

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_ACCEPT_CODE

Description

Accept code register for PeliCAN mode

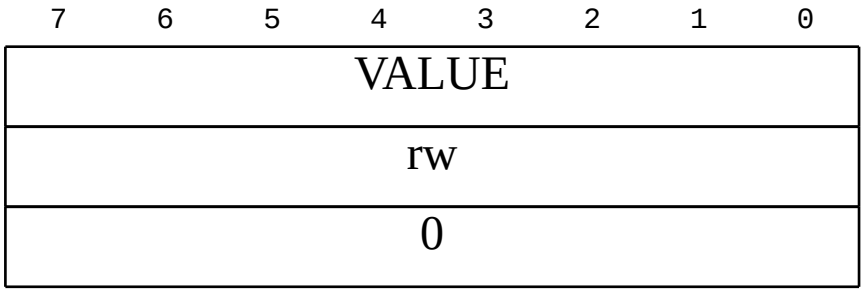
The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_ACCEPT_CODE

Description

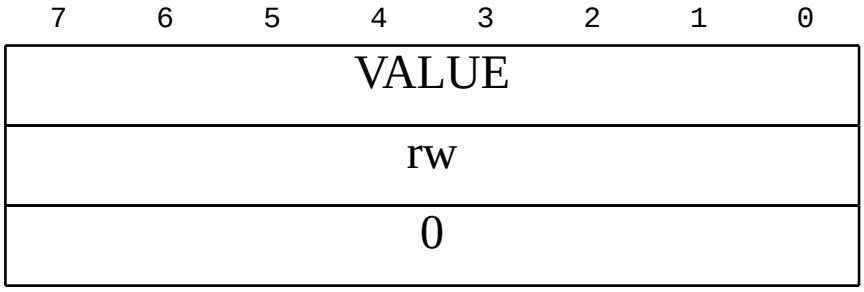
Accept code register for PeliCAN mode

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_TX_ID

Description

TxID register for PeliCAN mode

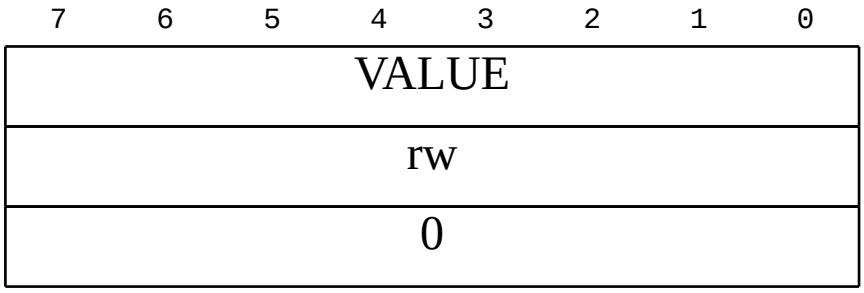
Reset value

0x00

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_TX_ID

Description

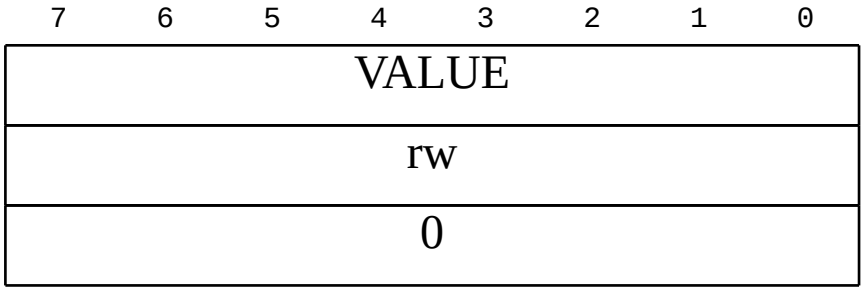
TxID register for PeliCAN mode

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_TX_ID

Description

TxID register for PeliCAN mode

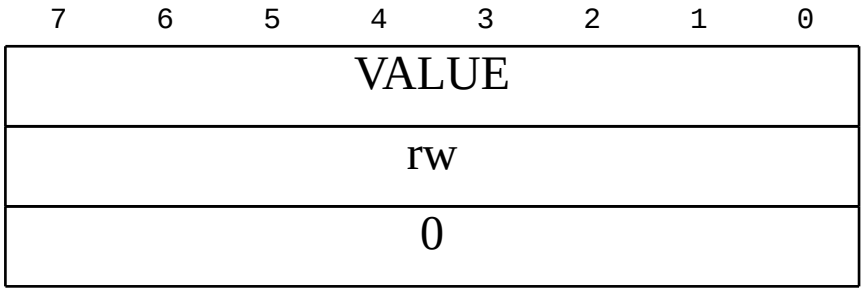
Reset value

0x00

Warm reset mask

0xff

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Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_TX_ID

Description

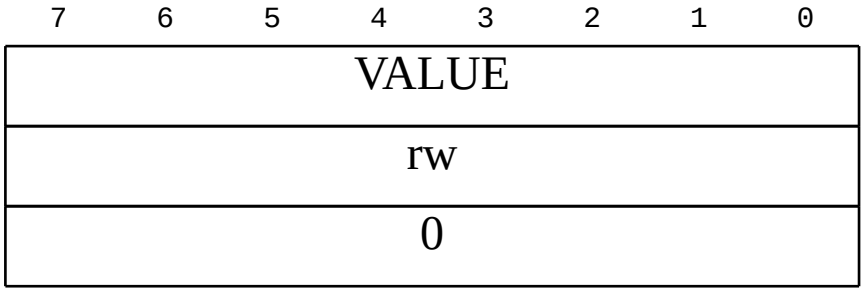
TxID register for PeliCAN mode

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_ACCEPT_MASK

Description

Accept mask register for PeliCAN mode

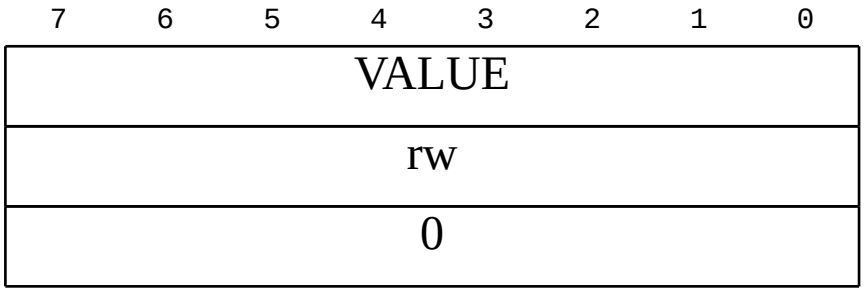
Reset value

0x00

Warm reset mask

0xff

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Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_ACCEPT_MASK

Description

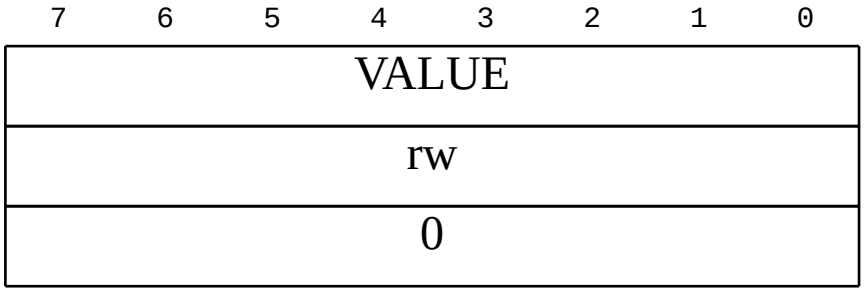
Accept mask register for PeliCAN mode

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_ACCEPT_MASK

Description

Accept mask register for PeliCAN mode

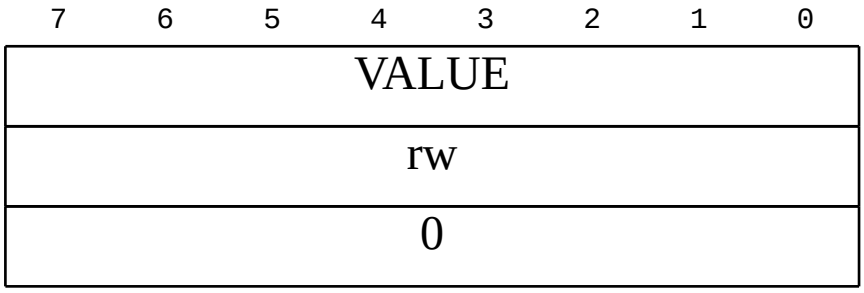
Reset value

0x00

Warm reset mask

0xff

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Field	Mask	Reset	Description
VALUE	0xff	0x0	

Register PELICAN_ACCEPT_MASK

Description

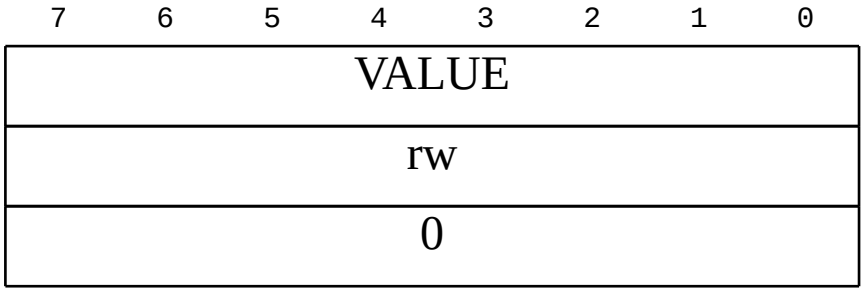
Accept mask register for PeliCAN mode

Reset value

0x00

Warm reset mask

0xff



Field	Mask	Reset	Description
VALUE	0xff	0x0	

Commands

Name	Description
delete	Dispose instance of CAN_OC

9.3.5. Limitations

The following deviations from real hardware are known to exist with this model:

- The controller clears the RX and TX buffers on reset. This is not the proper behavior and may have an impact on FDIR. Let us know if this is an issue.
- There is no arbitration of messages in the simulated world and busses are not synchronised.

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- The model does at present not register filters with the CAN bus model.
- The model currently ignores the error field in the CAN frame objects.
- The model currently assumes the CAN bus is running at 1 Mb/s (this assumption is in non-infinite speed mode). This is arguably incorrect and the timing should be picked from the bus timing register Contact Terma if this is this is critical for your needs.

9.4. GPTIMER

The GPTIMER is part of the GRLIB device library from Gaisler. The timer runs using synchronised events in order to ensure that would a timer tick be broadcasted by the interrupt controller, then the IRQ should be taken at roughly the same time.

9.4.1. Loading the Plugin

```
import GpTimer
```

9.4.2. Configuration

Separate Interrupts

Set the "config.separateInterrupts" property to non-zero.

Interrupt Index

The interrupt number can be set by configuring the "pnp.config" property. The lower 5 bits of the property is used for this.

Number of Timers

Set the "config.numTimers" property. By default this value is 4 to be compatible with the UT699.

Clear IRQ on Set

Set the "config.clearIrqOnSet" property changes the behaviour of bit 4 in the timer control registers. ClearOnSet can be non-zero (the default), in that case writing a 1 to the bit will clear bit 4 (i.e. it will read out as 0), if clearOnSet is zero, the bit is cleared if bit 4 is 0 in the written word.

The reason for this are ambiguities in the LEON3 and UT699 manuals.

9.4.3. @GpTimer Reference

Properties

Name	Type	Description
Class	*void	Class object

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GpTimer
new	Create new instance of GpTimer

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.4.4. GpTimer Reference

Properties

Name	Type	Description
CONFIGColdResetValue	uint32_t	Configuration register
CONFIGForcedBits	uint32_t	Configuration register
CONFIGForcedFlippedBits	uint32_t	Configuration register
CONFIGReadMask	uint32_t	Configuration register
CONFIGResetMask	uint32_t	Configuration register
CONFIGResetValue	uint32_t	Configuration register
CONFIGWriteMask	uint32_t	Configuration register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LATCHCFGColdResetValue	uint32_t	Timer latch configuration register
LATCHCFGForcedBits	uint32_t	Timer latch configuration register
LATCHCFGForcedFlippedBits	uint32_t	Timer latch configuration register
LATCHCFGReadMask	uint32_t	Timer latch configuration register
LATCHCFGResetMask	uint32_t	Timer latch configuration register
LATCHCFGResetValue	uint32_t	Timer latch configuration register
LATCHCFGWriteMask	uint32_t	Timer latch configuration register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
SCALERColdResetValue	uint32_t	Scaler value register
SCALERForcedBits	uint32_t	Scaler value register
SCALERForcedFlippedBits	uint32_t	Scaler value register
SCALERReadMask	uint32_t	Scaler value register
SCALERResetMask	uint32_t	Scaler value register
SCALERResetValue	uint32_t	Scaler value register
SCALERWriteMask	uint32_t	Scaler value register
SRELOADColdResetValue	uint32_t	Scaler reload value register
SRELOADForcedBits	uint32_t	Scaler reload value register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
SRELOADForcedFlippedBits	uint32_t	Scaler reload value register
SRELOADReadMask	uint32_t	Scaler reload value register
SRELOADResetMask	uint32_t	Scaler reload value register
SRELOADResetValue	uint32_t	Scaler reload value register
SRELOADWriteMask	uint32_t	Scaler reload value register
TimeSource	*void	Time source object
config.clearIrqOnSet	uint8_t	Use behaviour in GRIP manual. Set to zero for beahviour as documented in (UT699 manual from 2012 (p77).
config.clockDivider	uint32_t	Clock divider for scaling event posting
config.irqNumber	uint8_t	Set interrupt number for first interrupt
config.littleEndian	uint8_t	Endianess of memory interface.
config.numTimers	uint8_t	
config.separateInterrupts	uint8_t	Enable separate interrupts
config.traceInterrupts	uint8_t	
config.traceReads	uint8_t	
config.traceWrites	uint8_t	
config.underflowNotificationMask	uint32_t	
configReg	uint32_t	Configuration register
control	[uint32_t; 7]	Timer control register
counters	[uint32_t; 7]	Timer counter value register
irqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller.
latchConfigReg	uint32_t	Timer latch configuration register
latchReg	[uint32_t; 7]	Timer latch register
pnp.bar	uint32_t	
pnp.config	uint32_t	
reload	[uint32_t; 7]	Timer reload value register
scaler	uint32_t	Scaler value register
scalerReload	uint32_t	Scaler reload value register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
stats.interruptsRaised	[uint64_t; 32]	

Interfaces

Name	Type	Description
ApbIface	ApbIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
ObjectIface	ObjectIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Registers



Register support is currently experimental!

Register Bank Regs

Register SCALER

Description

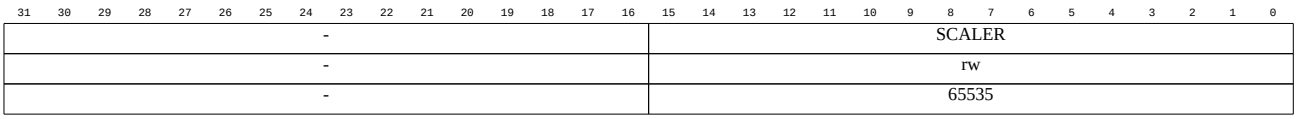
Scaler value register

Reset value

0x0000ffff

Warm reset mask

0x0000ffff



Field	Mask	Reset	Description
SCALER	0x0000ffff	0xffff	Scaler value

Register SRELOAD

Description

Scaler reload value register

Reset value

0x0000ffff

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Warm reset mask

0x0000ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																SRELOAD															
-																rw															
-																65535															

Field	Mask	Reset	Description
SRELOAD	0x0000ffff	0xffff	Scaler reload value

Register CONFIG

Description

Configuration register

Reset value

0x00000200

Warm reset mask

0x00003fff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																		EV	ES	EL	EE	DF	SI	IRQ					TIMERS		
-																		rw	rw	rw	rw	ro	ro	ro					ro		
-																		0	0	0	0	1	0	0					0		

Field	Mask	Reset	Description
EV	0x00002000	0x0	External events
ES	0x00001000	0x0	Enable set
EL	0x00000800	0x0	Enable latching
EE	0x00000400	0x0	Enable external clock source
DF	0x00000200	0x1	Disable timer freeze
SI	0x00000100	0x0	Separate interrupts
IRQ	0x000000f8	0x0	APB interrupt
TIMERS	0x00000007	0x0	Number of implemented timers

Register LATCHCFG

Description

Timer latch configuration register

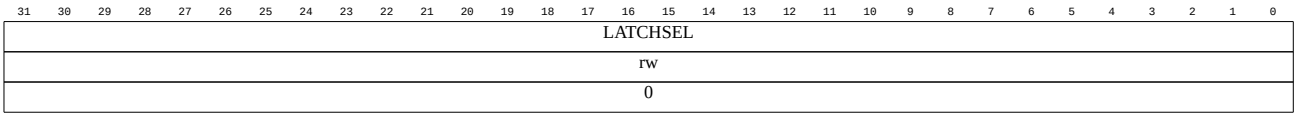
Reset value

0x00000000

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Warm reset mask

0xffffffff



Field	Mask	Reset	Description
LATCHSEL	0xffffffff	0x0	Latch select

Register TCNTVAL

Description

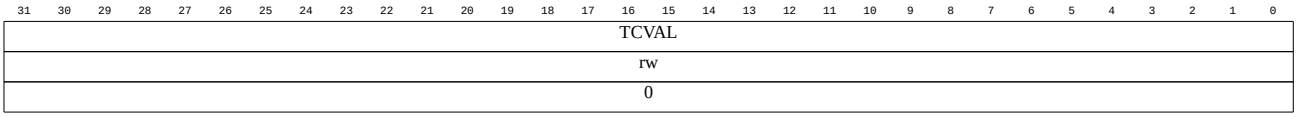
Timer counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCVAL	0xffffffff	0x0	Timer counter value

Register TCNTVAL

Description

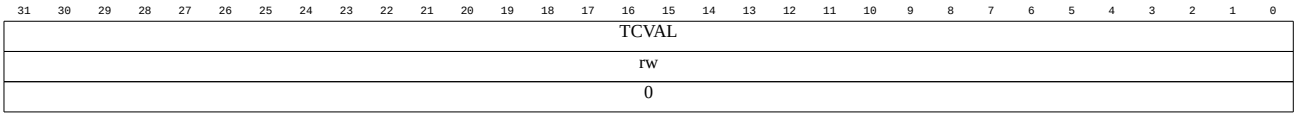
Timer counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCVAL	0xffffffff	0x0	Timer counter value

Register TCNTVAL

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

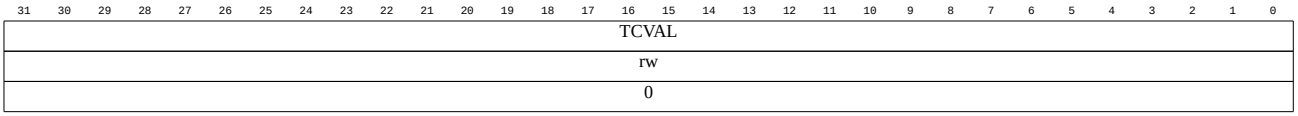
Timer counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCVAL	0xffffffff	0x0	Timer counter value

Register TCNTVAL

Description

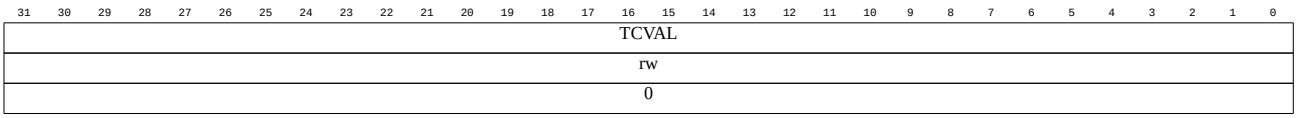
Timer counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCVAL	0xffffffff	0x0	Timer counter value

Register TCNTVAL

Description

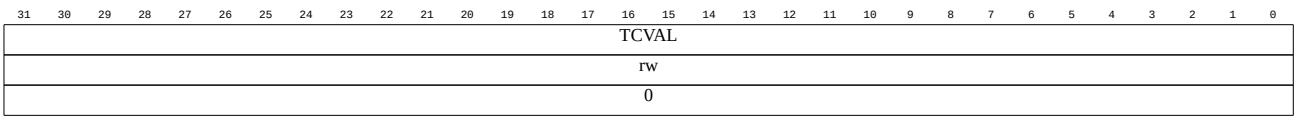
Timer counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
TCVAL	0xffffffff	0x0	Timer counter value

Register TCNTVAL

Description

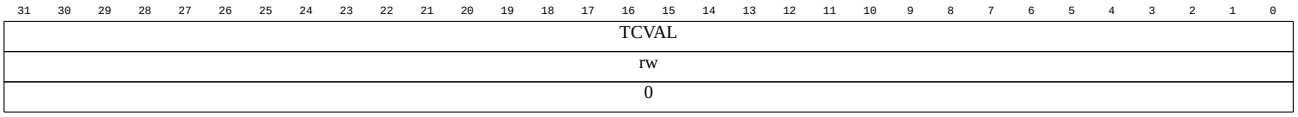
Timer counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCVAL	0xffffffff	0x0	Timer counter value

Register TCNTVAL

Description

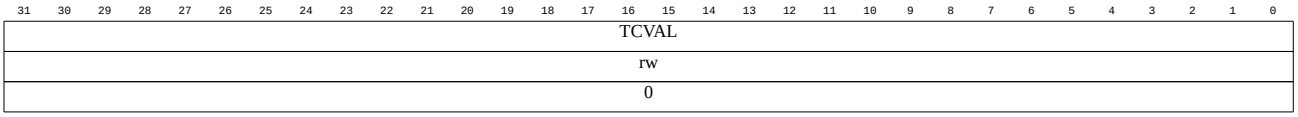
Timer counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCVAL	0xffffffff	0x0	Timer counter value

Register TRLDVAL

Description

Timer reload value register

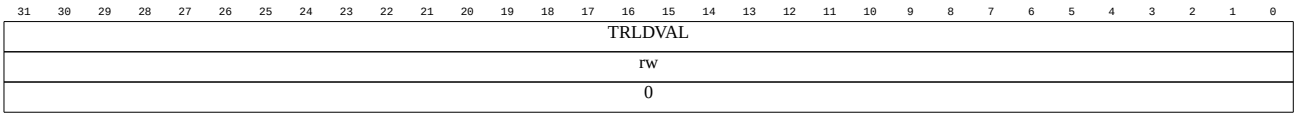
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TRLDVAL	0xffffffff	0x0	Timer reload value

Register TRLDVAL

Description

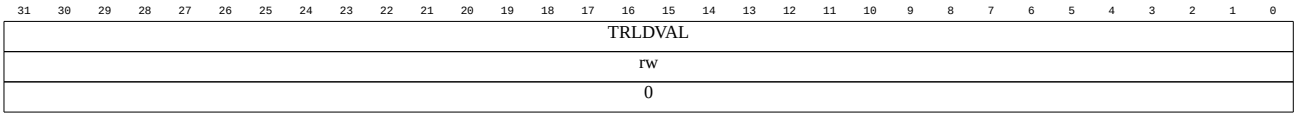
Timer reload value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TRLDVAL	0xffffffff	0x0	Timer reload value

Register TRLDVAL

Description

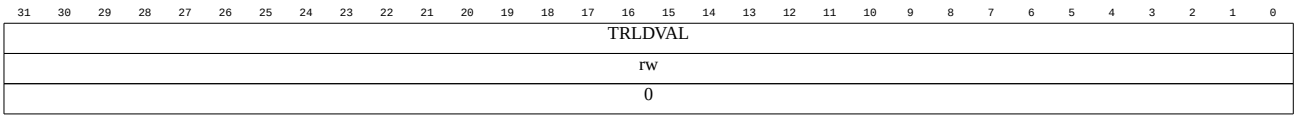
Timer reload value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TRLDVAL	0xffffffff	0x0	Timer reload value

Register TRLDVAL

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

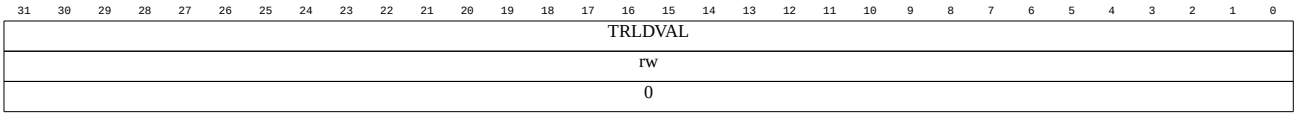
Timer reload value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TRLDVAL	0xffffffff	0x0	Timer reload value

Register TRLDVAL

Description

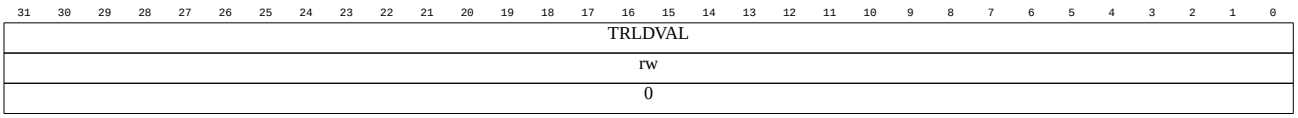
Timer reload value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TRLDVAL	0xffffffff	0x0	Timer reload value

Register TRLDVAL

Description

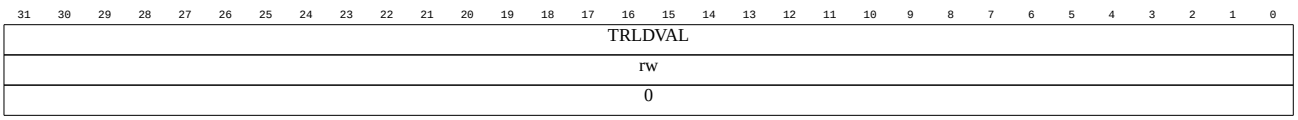
Timer reload value register

Reset value

0x00000000

Warm reset mask

0xffffffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
TRLDVAL	0xffffffff	0x0	Timer reload value

Register TRLDVAL

Description

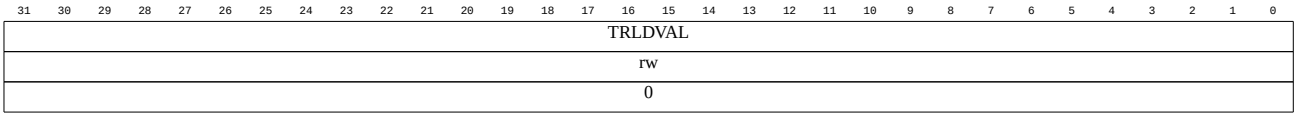
Timer reload value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TRLDVAL	0xffffffff	0x0	Timer reload value

Register TCTRL

Description

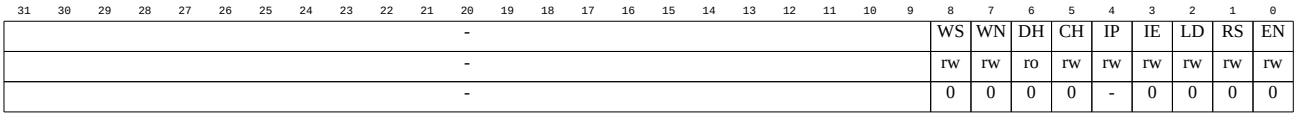
Timer control register

Reset value

0x00000000

Warm reset mask

0x000001ef



Field	Mask	Reset	Description
WS	0x00000100	0x0	Disable watchdog output
WN	0x00000080	0x0	Enable watchdog NMI
DH	0x00000040	0x0	Debug halt
CH	0x00000020	0x0	Chain with preceding timer
IP	0x00000010	-	Interrupt pending
IE	0x00000008	0x0	Interrupt enable
LD	0x00000004	0x0	Load

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
RS	0x00000002	0x0	Restart
EN	0x00000001	0x0	Enable

Register TCTRL

Description

Timer control register

Reset value

0x00000000

Warm reset mask

0x000001ef

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																							WS	WN	DH	CH	IP	IE	LD	RS	EN
-																							rw	rw	ro	rw	rw	rw	rw	rw	rw
-																							0	0	0	0	-	0	0	0	0

Field	Mask	Reset	Description
WS	0x00000100	0x0	Disable watchdog output
WN	0x00000080	0x0	Enable watchdog NMI
DH	0x00000040	0x0	Debug halt
CH	0x00000020	0x0	Chain with preceding timer
IP	0x00000010	-	Interrupt pending
IE	0x00000008	0x0	Interrupt enable
LD	0x00000004	0x0	Load
RS	0x00000002	0x0	Restart
EN	0x00000001	0x0	Enable

Register TCTRL

Description

Timer control register

Reset value

0x00000000

Warm reset mask

0x000001ef

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																							WS	WN	DH	CH	IP	IE	LD	RS	EN
-																							rw	rw	ro	rw	rw	rw	rw	rw	rw
-																							0	0	0	0	-	0	0	0	0

Field	Mask	Reset	Description
WS	0x00000100	0x0	Disable watchdog output
WN	0x00000080	0x0	Enable watchdog NMI
DH	0x00000040	0x0	Debug halt
CH	0x00000020	0x0	Chain with preceding timer
IP	0x00000010	-	Interrupt pending
IE	0x00000008	0x0	Interrupt enable
LD	0x00000004	0x0	Load
RS	0x00000002	0x0	Restart
EN	0x00000001	0x0	Enable

Register TCTRL

Description

Timer control register

Reset value

0x00000000

Warm reset mask

0x000001ef

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																							WS	WN	DH	CH	IP	IE	LD	RS	EN
-																							rw	rw	ro	rw	rw	rw	rw	rw	rw
-																							0	0	0	0	-	0	0	0	0

Field	Mask	Reset	Description
WS	0x00000100	0x0	Disable watchdog output
WN	0x00000080	0x0	Enable watchdog NMI
DH	0x00000040	0x0	Debug halt
CH	0x00000020	0x0	Chain with preceding timer
IP	0x00000010	-	Interrupt pending
IE	0x00000008	0x0	Interrupt enable
LD	0x00000004	0x0	Load
RS	0x00000002	0x0	Restart
EN	0x00000001	0x0	Enable

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register TCTRL

Description

Timer control register

Reset value

0x00000000

Warm reset mask

0x000001ef

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																							WS	WN	DH	CH	IP	IE	LD	RS	EN
-																							rw	rw	ro	rw	rw	rw	rw	rw	rw
-																							0	0	0	0	-	0	0	0	0

Field	Mask	Reset	Description
WS	0x00000100	0x0	Disable watchdog output
WN	0x00000080	0x0	Enable watchdog NMI
DH	0x00000040	0x0	Debug halt
CH	0x00000020	0x0	Chain with preceding timer
IP	0x00000010	-	Interrupt pending
IE	0x00000008	0x0	Interrupt enable
LD	0x00000004	0x0	Load
RS	0x00000002	0x0	Restart
EN	0x00000001	0x0	Enable

Register TCTRL

Description

Timer control register

Reset value

0x00000000

Warm reset mask

0x000001ef

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																							WS	WN	DH	CH	IP	IE	LD	RS	EN
-																							rw	rw	ro	rw	rw	rw	rw	rw	rw
-																							0	0	0	0	-	0	0	0	0

Field	Mask	Reset	Description
WS	0x00000100	0x0	Disable watchdog output
WN	0x00000080	0x0	Enable watchdog NMI

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
DH	0x00000040	0x0	Debug halt
CH	0x00000020	0x0	Chain with preceding timer
IP	0x00000010	-	Interrupt pending
IE	0x00000008	0x0	Interrupt enable
LD	0x00000004	0x0	Load
RS	0x00000002	0x0	Restart
EN	0x00000001	0x0	Enable

Register TCTRL

Description

Timer control register

Reset value

0x00000000

Warm reset mask

0x000001ef

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																							WS	WN	DH	CH	IP	IE	LD	RS	EN
-																							rw	rw	ro	rw	rw	rw	rw	rw	rw
-																							0	0	0	0	-	0	0	0	0

Field	Mask	Reset	Description
WS	0x00000100	0x0	Disable watchdog output
WN	0x00000080	0x0	Enable watchdog NMI
DH	0x00000040	0x0	Debug halt
CH	0x00000020	0x0	Chain with preceding timer
IP	0x00000010	-	Interrupt pending
IE	0x00000008	0x0	Interrupt enable
LD	0x00000004	0x0	Load
RS	0x00000002	0x0	Restart
EN	0x00000001	0x0	Enable

Register TLATCH

Description

Timer latch register

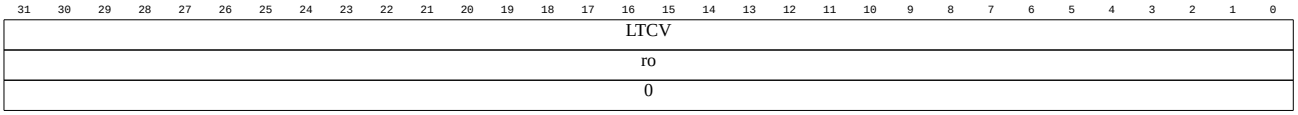
The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
LTCV	0xffffffff	0x0	Latched timer counter value

Register TLATCH

Description

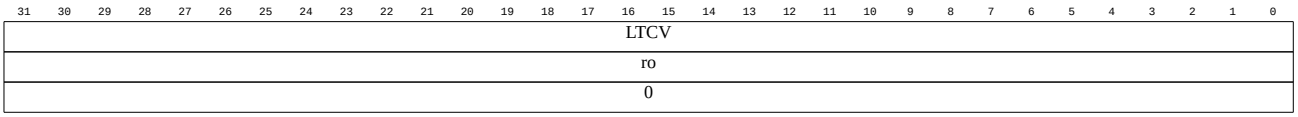
Timer latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
LTCV	0xffffffff	0x0	Latched timer counter value

Register TLATCH

Description

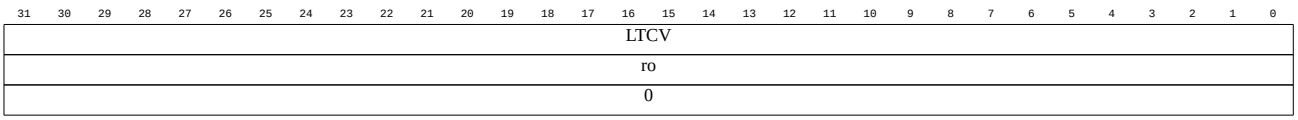
Timer latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
LTCV	0xffffffff	0x0	Latched timer counter value

Register TLATCH

Description

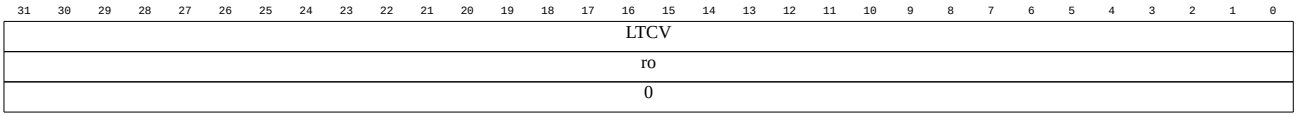
Timer latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
LTCV	0xffffffff	0x0	Latched timer counter value

Register TLATCH

Description

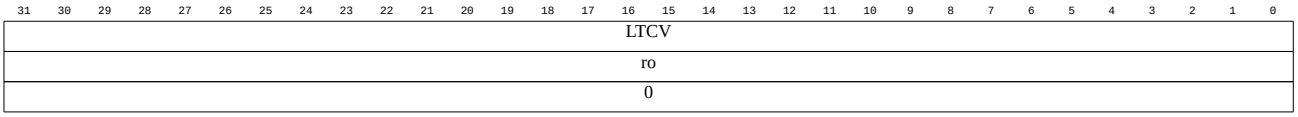
Timer latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
LTCV	0xffffffff	0x0	Latched timer counter value

Register TLATCH

Description

Timer latch register

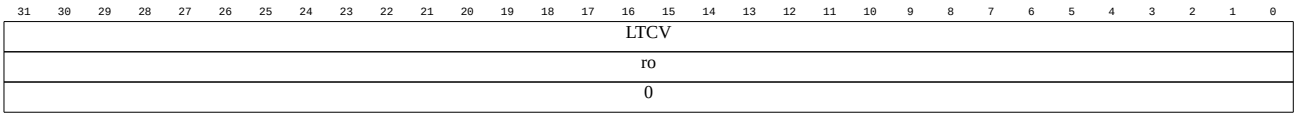
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
LTCV	0xffffffff	0x0	Latched timer counter value

Register TLATCH

Description

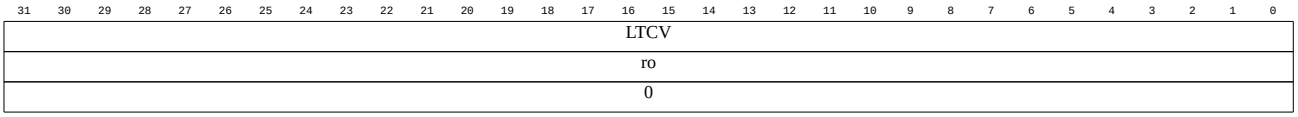
Timer latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
LTCV	0xffffffff	0x0	Latched timer counter value

Commands

Name	Description
delete	Dispose instance of GpTimer

9.4.5. Limitations

The following deviations from real hardware are known to exist with this model:

- The Disable Timer Freeze bit is always 1 and cannot be configured.
- The Debug Halt bit for each timer is always 0 and cannot be altered.
- The last timer does not work as a watchdog.
- The timer utilize synchronized events. The minimum time for a timer expiration on a multi-core CPU, will thus be equal to the time-quanta of the machine.

9.5. GRCAN

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

The GRCAN model is available in the GrCan plugin.

9.5.1. Loading the Plugin

```
import GrCan
```

9.5.2. Configuration

9.5.3. @GRCAN Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GRCAN
new	Create new instance of GRCAN

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.5.4. GRCAN Reference

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Properties

Name	Type	Description
CONFColdResetValue	uint32_t	Configuration register
CONFForcedBits	uint32_t	Configuration register
CONFForcedFlippedBits	uint32_t	Configuration register
CONFReadMask	uint32_t	Configuration register
CONFResetMask	uint32_t	Configuration register
CONFResetValue	uint32_t	Configuration register
CONFWriteMask	uint32_t	Configuration register
CTRLColdResetValue	uint32_t	Control register
CTRLForcedBits	uint32_t	Control register
CTRLForcedFlippedBits	uint32_t	Control register
CTRLReadMask	uint32_t	Control register
CTRLResetMask	uint32_t	Control register
CTRLResetValue	uint32_t	Control register
CTRLWriteMask	uint32_t	Control register
CanIMRColdResetValue	uint32_t	Interrupt mask register
CanIMRForcedBits	uint32_t	Interrupt mask register
CanIMRForcedFlippedBits	uint32_t	Interrupt mask register
CanIMRReadMask	uint32_t	Interrupt mask register
CanIMRResetMask	uint32_t	Interrupt mask register
CanIMRResetValue	uint32_t	Interrupt mask register
CanIMRWriteMask	uint32_t	Interrupt mask register
CanPIRColdResetValue	uint32_t	Pending interrupt register
CanPIRForcedBits	uint32_t	Pending interrupt register
CanPIRForcedFlippedBits	uint32_t	Pending interrupt register
CanPIRReadMask	uint32_t	Pending interrupt register
CanPIRResetMask	uint32_t	Pending interrupt register
CanPIRResetValue	uint32_t	Pending interrupt register
CanPIRWriteMask	uint32_t	Pending interrupt register
Class	*void	Class object
Component	*void	Pointer to component object if part of component

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
RXADDRColdResetValue	uint32_t	Receive channel address register
RXADDRForcedBits	uint32_t	Receive channel address register
RXADDRForcedFlippedBits	uint32_t	Receive channel address register
RXADDRReadMask	uint32_t	Receive channel address register
RXADDRResetMask	uint32_t	Receive channel address register
RXADDRResetValue	uint32_t	Receive channel address register
RXADDRWriteMask	uint32_t	Receive channel address register
RXCODEColdResetValue	uint32_t	Receive channel code register
RXCODEForcedBits	uint32_t	Receive channel code register
RXCODEForcedFlippedBits	uint32_t	Receive channel code register
RXCODEReadMask	uint32_t	Receive channel code register
RXCODEResetMask	uint32_t	Receive channel code register
RXCODEResetValue	uint32_t	Receive channel code register
RXCODEWriteMask	uint32_t	Receive channel code register
RXCTRLColdResetValue	uint32_t	Receive channel control register
RXCTRLForcedBits	uint32_t	Receive channel control register
RXCTRLForcedFlippedBits	uint32_t	Receive channel control register
RXCTRLReadMask	uint32_t	Receive channel control register
RXCTRLResetMask	uint32_t	Receive channel control register
RXCTRLResetValue	uint32_t	Receive channel control register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
RXCTRLWriteMask	uint32_t	Receive channel control register
RXIRQColdResetValue	uint32_t	Receive channel interrupt register
RXIRQForcedBits	uint32_t	Receive channel interrupt register
RXIRQForcedFlippedBits	uint32_t	Receive channel interrupt register
RXIRQReadMask	uint32_t	Receive channel interrupt register
RXIRQResetMask	uint32_t	Receive channel interrupt register
RXIRQResetValue	uint32_t	Receive channel interrupt register
RXIRQWriteMask	uint32_t	Receive channel interrupt register
RXMASKColdResetValue	uint32_t	Receive channel mask register
RXMASKForcedBits	uint32_t	Receive channel mask register
RXMASKForcedFlippedBits	uint32_t	Receive channel mask register
RXMASKReadMask	uint32_t	Receive channel mask register
RXMASKResetMask	uint32_t	Receive channel mask register
RXMASKResetValue	uint32_t	Receive channel mask register
RXMASKWriteMask	uint32_t	Receive channel mask register
RXRDColdResetValue	uint32_t	Receive channel read register
RXRDForcedBits	uint32_t	Receive channel read register
RXRDForcedFlippedBits	uint32_t	Receive channel read register
RXRDReadMask	uint32_t	Receive channel read register
RXRDResetMask	uint32_t	Receive channel read register
RXRDResetValue	uint32_t	Receive channel read register
RXRDWriteMask	uint32_t	Receive channel read register
RXSIZEColdResetValue	uint32_t	Receive channel size register
RXSIZEForcedBits	uint32_t	Receive channel size register
RXSIZEForcedFlippedBits	uint32_t	Receive channel size register
RXSIZEReadMask	uint32_t	Receive channel size register
RXSIZEResetMask	uint32_t	Receive channel size register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
RXSIZEResetValue	uint32_t	Receive channel size register
RXSIZEWriteMask	uint32_t	Receive channel size register
RXWRColdResetValue	uint32_t	Receive channel write register
RXWRForcedBits	uint32_t	Receive channel write register
RXWRForcedFlippedBits	uint32_t	Receive channel write register
RXWRReadMask	uint32_t	Receive channel write register
RXWRResetMask	uint32_t	Receive channel write register
RXWRResetValue	uint32_t	Receive channel write register
RXWRWriteMask	uint32_t	Receive channel write register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
STATColdResetValue	uint32_t	Status register
STATForcedBits	uint32_t	Status register
STATForcedFlippedBits	uint32_t	Status register
STATReadMask	uint32_t	Status register
STATResetMask	uint32_t	Status register
STATResetValue	uint32_t	Status register
STATWriteMask	uint32_t	Status register
SYNCCODEColdResetValue	uint32_t	Sync code filter register
SYNCCODEForcedBits	uint32_t	Sync code filter register
SYNCCODEForcedFlippedBits	uint32_t	Sync code filter register
SYNCCODEReadMask	uint32_t	Sync code filter register
SYNCCODEResetMask	uint32_t	Sync code filter register
SYNCCODEResetValue	uint32_t	Sync code filter register
SYNCCODEWriteMask	uint32_t	Sync code filter register
SYNCMASKColdResetValue	uint32_t	Sync mask filter register
SYNCMASKForcedBits	uint32_t	Sync mask filter register
SYNCMASKForcedFlippedBits	uint32_t	Sync mask filter register
SYNCMASKReadMask	uint32_t	Sync mask filter register
SYNCMASKResetMask	uint32_t	Sync mask filter register
SYNCMASKResetValue	uint32_t	Sync mask filter register
SYNCMASKWriteMask	uint32_t	Sync mask filter register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
TXADDRColdResetValue	uint32_t	Transmit channel address register
TXADDRForcedBits	uint32_t	Transmit channel address register
TXADDRForcedFlippedBits	uint32_t	Transmit channel address register
TXADDRReadMask	uint32_t	Transmit channel address register
TXADDRResetMask	uint32_t	Transmit channel address register
TXADDRResetValue	uint32_t	Transmit channel address register
TXADDRWriteMask	uint32_t	Transmit channel address register
TXCTRLColdResetValue	uint32_t	Transmit channel control register
TXCTRLForcedBits	uint32_t	Transmit channel control register
TXCTRLForcedFlippedBits	uint32_t	Transmit channel control register
TXCTRLReadMask	uint32_t	Transmit channel control register
TXCTRLResetMask	uint32_t	Transmit channel control register
TXCTRLResetValue	uint32_t	Transmit channel control register
TXCTRLWriteMask	uint32_t	Transmit channel control register
TXIRQColdResetValue	uint32_t	Transmit channel interrupt register
TXIRQForcedBits	uint32_t	Transmit channel interrupt register
TXIRQForcedFlippedBits	uint32_t	Transmit channel interrupt register
TXIRQReadMask	uint32_t	Transmit channel interrupt register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
TXIRQResetMask	uint32_t	Transmit channel interrupt register
TXIRQResetValue	uint32_t	Transmit channel interrupt register
TXIRQWriteMask	uint32_t	Transmit channel interrupt register
TXRDColdResetValue	uint32_t	Transmit channel read register
TXRDForcedBits	uint32_t	Transmit channel read register
TXRDForcedFlippedBits	uint32_t	Transmit channel read register
TXRDReadMask	uint32_t	Transmit channel read register
TXRDResetMask	uint32_t	Transmit channel read register
TXRDResetValue	uint32_t	Transmit channel read register
TXRDWriteMask	uint32_t	Transmit channel read register
TXSIZEColdResetValue	uint32_t	Transmit channel size register
TXSIZEForcedBits	uint32_t	Transmit channel size register
TXSIZEForcedFlippedBits	uint32_t	Transmit channel size register
TXSIZEReadMask	uint32_t	Transmit channel size register
TXSIZEResetMask	uint32_t	Transmit channel size register
TXSIZEResetValue	uint32_t	Transmit channel size register
TXSIZEWriteMask	uint32_t	Transmit channel size register
TXWRColdResetValue	uint32_t	Transmit channel write register
TXWRForcedBits	uint32_t	Transmit channel write register
TXWRForcedFlippedBits	uint32_t	Transmit channel write register
TXWRReadMask	uint32_t	Transmit channel write register
TXWRResetMask	uint32_t	Transmit channel write register
TXWRResetValue	uint32_t	Transmit channel write register
TXWRWriteMask	uint32_t	Transmit channel write register
TimeSource	*void	Time source object
bus	temu_IfaceRef/ <unknown>	CAN bus.
cfg	uint32_t	Configuration register
config.irq	uint8_t	Interrupt number
config.littleEndian	uint8_t	Endianess of memory interface.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
config.logMessages	uint8_t	Enable logging of transmitted and received messages.
config.singleIrq	uint8_t	Single interrupt
ctrl	uint32_t	Control register
irqCtrl	temu_IfaceRef/ <unknown>	IRQ controller.
irqMask	uint32_t	Interrupt mask register
memAccess	temu_IfaceRef/ <unknown>	Memory access for DMA
pendIrq	uint32_t	Pending interrupt register
pnp.bar	uint32_t	AMBA plug and play base address register
pnp.config	uint32_t	AMBA plug and play config word
rxChanAddr	uint32_t	Receive channel address register
rxChanCode	uint32_t	Receive channel code register
rxChanCtrl	uint32_t	Receive channel control register
rxChanIrq	uint32_t	Receive channel interrupt register
rxChanMask	uint32_t	Receive channel mask register
rxChanRd	uint32_t	Receive channel read register
rxChanSize	uint32_t	Receive channel size register
rxChanWr	uint32_t	Receive channel write register
stat	uint32_t	Status register
syncCodeFilt	uint32_t	Sync code filter register
syncMaskFilt	uint32_t	Sync mask filter register
txChanAddr	uint32_t	Transmit channel address register
txChanCtrl	uint32_t	Transmit channel control register
txChanIrq	uint32_t	Transmit channel interrupt register
txChanRd	uint32_t	Transmit channel read register
txChanSize	uint32_t	Transmit channel size register
txChanWr	uint32_t	Transmit channel write register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Interfaces

Name	Type	Description
ApbIface	ApbIface	APB P&P interface
CanDevIface	CanDevIface	CAN device interface
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	Memory access interface (registers)
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Registers



Register support is currently experimental!

Register Bank Regs

Register CONF

Description

Configuration register

Reset value

0x00000000

Warm reset mask

0xffff733f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCALER								PS1				PS2				-	RSJ			-		BPR		-		SAM	SILENT	SELECT	ENABLE	ENABLE0	BOR
rw								rw				rw				-	rw			-		rw		-		rw	rw	rw	rw	rw	rw
0								0				0				-	0			-		0		-		0	0	0	0	0	0

Field	Mask	Reset	Description
SCALER	0xff000000	0x0	Prescaler setting
PS1	0x00f00000	0x0	Phase segment 1
PS2	0x000f0000	0x0	Phase segment 2
RSJ	0x00007000	0x0	Resynchronization jumps
BPR	0x00000300	0x0	Baud rate prescaler
SAM	0x00000020	0x0	Sample mode
SILENT	0x00000010	0x0	Listen-only mode
SELECT	0x00000008	0x0	Receiver and transmitter selection

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Field	Mask	Reset	Description
ENABLE1	0x00000004	0x0	Output 1 enable
ENABLE0	0x00000002	0x0	Output 0 enable
ABORT	0x00000001	0x0	Abort transfer on AHB error

Register STAT

Description

Status register

Reset value

0x00000000

Warm reset mask

0xffffff0f

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3	2	1	0
TxChannels	RxChannels	TxErrCntr	RxErrCntr	-	AHBErr	OR	OFF	PASS
ro	ro	ro	ro	-	ro	ro	ro	ro
0	0	0	0	-	0	0	0	0

Field	Mask	Reset	Description
TxChannels	0xf0000000	0x0	Number of Tx channels minus one
RxChannels	0x0f000000	0x0	Number of Rx channels minus one
TxErrCntr	0x00ff0000	0x0	Transmission error counter
RxErrCntr	0x0000ff00	0x0	Reception error counter
AHBErr	0x00000008	0x0	AMBA AHB master interface blocked by previous AHB error
OR	0x00000004	0x0	Overrun during reception
OFF	0x00000002	0x0	Bus-off condition
PASS	0x00000001	0x0	Error-passive condition

Register CTRL

Description

Control register

Reset value

0x00000000

Warm reset mask

0x00000001

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																														RESET	ENABL
-																														wo	rw
-																														-	0

Field	Mask	Reset	Description
RESET	0x00000002	-	Reset complete core
ENABLE	0x00000001	0x0	Enable CAN controller

Register SYNCMASK

Description

Sync mask filter register

Reset value

0x1fffffff

Warm reset mask

0x1fffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	MASK																														
-	rw																														
-	536870911																														

Field	Mask	Reset	Description
MASK	0x1fffffff	0x1fffffff	SYNC message identifier mask

Register SYNCCODE

Description

Sync code filter register

Reset value

0x00000000

Warm reset mask

0x1fffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	SYNC																														
-	rw																														
-	0																														

Field	Mask	Reset	Description
SYNC	0x1fffffff	0x0	SYNC message identifier

Register CanPIMSR

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Pending interrupt masked status register

Reset value

0x00000000

Warm reset mask

0x0001ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-															TxLoss	RxMiss	TxErrCntr	RxErrCntr	TxSync	RxSync	Tx	Rx	TxEmpty	RxFull	TxIRQ	RxIRQ	TxAHBErr	RxAHBErr	OR	OFF	PASS
-															rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-															0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
TxLoss	0x00010000	0x0	Message arbitration lost during transmission
RxMiss	0x00008000	0x0	Message filtered away during reception
TxErrCntr	0x00004000	0x0	Transmission error counter incremented
RxErrCntr	0x00002000	0x0	Reception error counter incremented
TxSync	0x00001000	0x0	Synchronization message transmitted
RxSync	0x00000800	0x0	Synchronization message received
Tx	0x00000400	0x0	Successful transmission of message
Rx	0x00000200	0x0	Successful reception of message
TxEmpty	0x00000100	0x0	Successful transmission of all messages in buffer
RxFull	0x00000080	0x0	Successful reception of all messages possible to store in buffer
TxIRQ	0x00000040	0x0	Successful transmission of a predefined number of messages
RxIRQ	0x00000020	0x0	Successful reception of a predefined number of messages
TxAHBErr	0x00000010	0x0	AHB error during transmission
RxAHBErr	0x00000008	0x0	AHB error during reception
OR	0x00000004	0x0	Overrun during reception
OFF	0x00000002	0x0	Bus-off condition
PASS	0x00000001	0x0	Error-passive condition

Register CanPIMR

Description

Pending interrupt masked register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0x0001ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-															TxLoss	RxMiss	TxErrCntr	RxErrCntr	TxSync	RxSync	Tx	Rx	TxEmpty	RxFull	TxIRQ	RxIRQ	TxAHBErr	RxAHBErr	OR	OFF	PASS
-															rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-															0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
TxLoss	0x00010000	0x0	Message arbitration lost during transmission
RxMiss	0x00008000	0x0	Message filtered away during reception
TxErrCntr	0x00004000	0x0	Transmission error counter incremented
RxErrCntr	0x00002000	0x0	Reception error counter incremented
TxSync	0x00001000	0x0	Synchronization message transmitted
RxSync	0x00000800	0x0	Synchronization message received
Tx	0x00000400	0x0	Successful transmission of message
Rx	0x00000200	0x0	Successful reception of message
TxEmpty	0x00000100	0x0	Successful transmission of all messages in buffer
RxFull	0x00000080	0x0	Successful reception of all messages possible to store in buffer
TxIRQ	0x00000040	0x0	Successful transmission of a predefined number of messages
RxIRQ	0x00000020	0x0	Successful reception of a predefined number of messages
TxAHBErr	0x00000010	0x0	AHB error during transmission
RxAHBErr	0x00000008	0x0	AHB error during reception
OR	0x00000004	0x0	Overrun during reception
OFF	0x00000002	0x0	Bus-off condition
PASS	0x00000001	0x0	Error-passive condition

Register CanPISR

Description

Pending interrupt status register

Reset value

0x00000000

Warm reset mask

0x0001ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-															TxLoss	RxMiss	TxErrCntr	RxErrCntr	TxSync	RxSync	Tx	Rx	TxEmpty	RxFull	TxIRQ	RxIRQ	TxAHBErr	RxAHBErr	OR	OFF	PASS
-															rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-															0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
TxLoss	0x00010000	0x0	Message arbitration lost during transmission
RxMiss	0x00008000	0x0	Message filtered away during reception
TxErrCntr	0x00004000	0x0	Transmission error counter incremented
RxErrCntr	0x00002000	0x0	Reception error counter incremented
TxSync	0x00001000	0x0	Synchronization message transmitted
RxSync	0x00000800	0x0	Synchronization message received
Tx	0x00000400	0x0	Successful transmission of message
Rx	0x00000200	0x0	Successful reception of message
TxEmpty	0x00000100	0x0	Successful transmission of all messages in buffer
RxFull	0x00000080	0x0	Successful reception of all messages possible to store in buffer
TxIRQ	0x00000040	0x0	Successful transmission of a predefined number of messages
RxIRQ	0x00000020	0x0	Successful reception of a predefined number of messages
TxAHBErr	0x00000010	0x0	AHB error during transmission
RxAHBErr	0x00000008	0x0	AHB error during reception
OR	0x00000004	0x0	Overrun during reception
OFF	0x00000002	0x0	Bus-off condition
PASS	0x00000001	0x0	Error-passive condition

Register CanPIR

Description

Pending interrupt register

Reset value

0x00000000

Warm reset mask

0x0001ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-															TxLoss	RxMiss	TxErrCntr	RxErrCntr	TxSync	RxSync	Tx	Rx	TxEmpty	RxFull	TxIRQ	RxIRQ	TxAHBErr	RxAHBErr	OR	OFF	PASS
-															rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-															0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
TxLoss	0x00010000	0x0	Message arbitration lost during transmission
RxMiss	0x00008000	0x0	Message filtered away during reception
TxErrCntr	0x00004000	0x0	Transmission error counter incremented

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
RxErrCntr	0x00002000	0x0	Reception error counter incremented
TxSync	0x00001000	0x0	Synchronization message transmitted
RxSync	0x00000800	0x0	Synchronization message received
Tx	0x00000400	0x0	Successful transmission of message
Rx	0x00000200	0x0	Successful reception of message
TxEmpty	0x00000100	0x0	Successful transmission of all messages in buffer
RxFull	0x00000080	0x0	Successful reception of all messages possible to store in buffer
TxIRQ	0x00000040	0x0	Successful transmission of a predefined number of messages
RxIRQ	0x00000020	0x0	Successful reception of a predefined number of messages
TxAHBErr	0x00000010	0x0	AHB error during transmission
RxAHBErr	0x00000008	0x0	AHB error during reception
OR	0x00000004	0x0	Overrun during reception
OFF	0x00000002	0x0	Bus-off condition
PASS	0x00000001	0x0	Error-passive condition

Register CanIMR

Description

Interrupt mask register

Reset value

0x00000000

Warm reset mask

0x0001ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-															TxLoss	RxMiss	TxErrCntr	RxErrCntr	TxSync	RxSync	Tx	Rx	TxEmpty	RxFull	TxIRQ	RxIRQ	TxAHBErr	RxAHBErr	OR	OFF	PASS
-															rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-															0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
TxLoss	0x00010000	0x0	Message arbitration lost interrupt mask
RxMiss	0x00008000	0x0	Receive miss interrupt mask
TxErrCntr	0x00004000	0x0	Tx error counter interrupt mask
RxErrCntr	0x00002000	0x0	Rx error counter interrupt mask
TxSync	0x00001000	0x0	Tx synchronization interrupt mask
RxSync	0x00000800	0x0	Rx synchronization interrupt mask

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
Tx	0x00000400	0x0	Transmit interrupt mask
Rx	0x00000200	0x0	Receive interrupt mask
TxEmpty	0x00000100	0x0	Transmit empty interrupt mask
RxFull	0x00000080	0x0	Receive full interrupt mask
TxIRQ	0x00000040	0x0	Transmit channel interrupt mask
RxIRQ	0x00000020	0x0	Receive channel interrupt mask
TxAHBErr	0x00000010	0x0	Transmit AHB error interrupt mask
RxAHBErr	0x00000008	0x0	Receive AHB error interrupt mask
OR	0x00000004	0x0	Overrun interrupt mask
OFF	0x00000002	0x0	Bus-off interrupt mask
PASS	0x00000001	0x0	Error-passive interrupt mask

Register CanPICR

Description

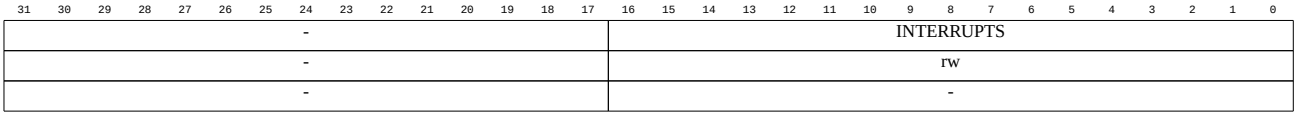
Pending interrupt clear register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
INTERRUPTS	0x0001ffff	-	Pending interrupt clear

Register TXCTRL

Description

Transmit channel control register

Reset value

0x00000000

Warm reset mask

0x00000007

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																													SINGLE	ONGOING	ENABLE
-																													rw	rw	rw
-																													0	0	0

Field	Mask	Reset	Description
SINGLE	0x00000004	0x0	Single shot mode
ONGOING	0x00000002	0x0	Transmission ongoing
ENABLE	0x00000001	0x0	Enable channel

Register TXADDR

Description

Transmit channel address register

Reset value

0x00000000

Warm reset mask

0xfffffc00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																						-									
rw																						-									
0																						-									

Field	Mask	Reset	Description
ADDR	0xfffffc00	0x0	Base address for circular buffer

Register TXSIZE

Description

Transmit channel size register

Reset value

0x00000000

Warm reset mask

0x001fffc0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																			SIZE										-			
-																			rw										-			
-																			0										-			

Field	Mask	Reset	Description
SIZE	0x001fffc0	0x0	Circular buffer size

Register TXWR

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Transmit channel write register

Reset value

0x00000000

Warm reset mask

0x000ffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-												WRITE																-			
-												rw																-			
-												0																-			

Field	Mask	Reset	Description
WRITE	0x000ffff0	0x0	Pointer to last written message plus one

Register TXRD

Description

Transmit channel read register

Reset value

0x00000000

Warm reset mask

0x000ffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-												READ																-			
-												rw																-			
-												0																-			

Field	Mask	Reset	Description
READ	0x000ffff0	0x0	Pointer to last read message plus one

Register TXIRQ

Description

Transmit channel interrupt register

Reset value

0x00000000

Warm reset mask

0x000ffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-												IRQ																-			
-												rw																-			
-												0																-			

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IRQ	0x000ffff0	0x0	Transmit interrupt pointer

Register RXCTRL

Description

Receive channel control register

Reset value

0x00000000

Warm reset mask

0x00000003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																														ONGOING	ENABLE
-																														ro	rw
-																														0	0

Field	Mask	Reset	Description
ONGOING	0x00000002	0x0	Reception ongoing
ENABLE	0x00000001	0x0	Enable channel

Register RXADDR

Description

Receive channel address register

Reset value

0x00000000

Warm reset mask

0xfffffc00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																						-									
rw																						-									
0																						-									

Field	Mask	Reset	Description
ADDR	0xfffffc00	0x0	Base address for circular buffer

Register RXSIZE

Description

Receive channel size register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0x001fffc0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-											SIZE																	-			
-											rw																	-			
-											0																	-			

Field	Mask	Reset	Description
SIZE	0x001fffc0	0x0	Circular buffer size

Register RXWR

Description

Receive channel write register

Reset value

0x00000000

Warm reset mask

0x000ffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-												WRITE																-			
-												rw																-			
-												0																-			

Field	Mask	Reset	Description
WRITE	0x000ffff0	0x0	Pointer to last written message plus one

Register RXRD

Description

Receive channel read register

Reset value

0x00000000

Warm reset mask

0x000ffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-												READ																-			
-												rw																-			
-												0																-			

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
READ	0x000ffff0	0x0	Pointer to last read message plus one

Register RXIRQ

Description

Receive channel interrupt register

Reset value

0x00000000

Warm reset mask

0x000ffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-												IRQ																-			
-												rw																-			
-												0																-			

Field	Mask	Reset	Description
IRQ	0x000ffff0	0x0	Receive interrupt pointer

Register RXMASK

Description

Receive channel mask register

Reset value

0x1fffffff

Warm reset mask

0x1fffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	AM																														
-	rw																														
-	536870911																														

Field	Mask	Reset	Description
AM	0x1fffffff	0x1fffffff	Acceptance mask

Register RXCODE

Description

Receive channel code register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0x1fffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	AC																														
-	rw																														
-	0																														

Field	Mask	Reset	Description
AC	`0x1fffffff`	`0x0`	Acceptance code

Commands

Name	Description
delete	Dispose instance of GRCAN

9.5.5. Limitations

- There is no arbitration of messages in the message passing simulated world and buses are not synchronized.
- The model does at present not register filters with the CAN bus model.

9.6. GRETH and GRETH_GBIT

The GRETH model is available in the GrEth plugin. The model needs to be combined with a MDIOBus, PHY and Ethernet model.

The GRETH model implements the behaviour of both `GRETH` and `GRETH_GBIT`.

9.6.1. Loading the Plugin

```
import BusModels
import GrEth
GRETH.new name=greth0
GenericPHY.new name=phy0
EthernetLink.new name=eth0
connect a=greth0.phy b=phy0:PHYIface
connect a=greth0.mdioBus b=phy0:MDIOIface
connect a=apbctrl0.slaves b=greth0:ApbIface
greth0.setMAC mac="00:00:00:00:00:01"
connect a=phy0.mac b=greth0:MACIface
eth0.connect device=phy0:PHYIface
```

9.6.2. Configuration

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

The `config.gbitVariant` property can be set to enable `GRETH_GBIT` extensions. The extensions includes:

- Gigabit speed.
- IP header checksum offloading.
- TCP checksum offloading.
- UDP checksum offloading.
- Scatter / gather send lists.

9.6.3. @GRETH Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GRETH
new	Create new instance of GRETH

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

9.6.4. GRETH Reference

Properties

Name	Type	Description
CTRLColdResetValue	uint32_t	Control register
CTRLForcedBits	uint32_t	Control register
CTRLForcedFlippedBits	uint32_t	Control register
CTRLReadMask	uint32_t	Control register
CTRLResetMask	uint32_t	Control register
CTRLResetValue	uint32_t	Control register
CTRLWriteMask	uint32_t	Control register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
EDCLIP	uint32_t	EDCL IP register
EDCLIPColdResetValue	uint32_t	EDCL IP register
EDCLIPForcedBits	uint32_t	EDCL IP register
EDCLIPForcedFlippedBits	uint32_t	EDCL IP register
EDCLIPReadMask	uint32_t	EDCL IP register
EDCLIPResetMask	uint32_t	EDCL IP register
EDCLIPResetValue	uint32_t	EDCL IP register
EDCLIPWriteMask	uint32_t	EDCL IP register
EMACLSB	uint32_t	EDCL MAC address LSB register
EMACLSBColdResetValue	uint32_t	EDCL MAC address LSB register
EMACLSBForcedBits	uint32_t	EDCL MAC address LSB register
EMACLSBForcedFlippedBits	uint32_t	EDCL MAC address LSB register
EMACLSBReadMask	uint32_t	EDCL MAC address LSB register
EMACLSBResetMask	uint32_t	EDCL MAC address LSB register
EMACLSBResetValue	uint32_t	EDCL MAC address LSB register
EMACLSBWriteMask	uint32_t	EDCL MAC address LSB register
EMACMSB	uint32_t	EDCL MAC address MSB register
EMACMSBColdResetValue	uint32_t	EDCL MAC address MSB register
EMACMSBForcedBits	uint32_t	EDCL MAC address MSB register
EMACMSBForcedFlippedBits	uint32_t	EDCL MAC address MSB register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
EMACMSBReadMask	uint32_t	EDCL MAC address MSB register
EMACMSBResetMask	uint32_t	EDCL MAC address MSB register
EMACMSBResetValue	uint32_t	EDCL MAC address MSB register
EMACMSBWriteMask	uint32_t	EDCL MAC address MSB register
ETHCTR	uint32_t	Control register
ETHMDC	uint32_t	MDIO control and status register
ETHRDP	uint32_t	Receiver descriptor base address register
ETHSIS	uint32_t	Status register
ETHTDP	uint32_t	Transmitter descriptor base address register
HLSB	uint32_t	Hash table LSB register
HLSBColdResetValue	uint32_t	Hash table LSB register
HLSBForcedBits	uint32_t	Hash table LSB register
HLSBForcedFlippedBits	uint32_t	Hash table LSB register
HLSBReadMask	uint32_t	Hash table LSB register
HLSBResetMask	uint32_t	Hash table LSB register
HLSBResetValue	uint32_t	Hash table LSB register
HLSBWriteMask	uint32_t	Hash table LSB register
HMSB	uint32_t	Hash table MSB register
HMSBColdResetValue	uint32_t	Hash table MSB register
HMSBForcedBits	uint32_t	Hash table MSB register
HMSBForcedFlippedBits	uint32_t	Hash table MSB register
HMSBReadMask	uint32_t	Hash table MSB register
HMSBResetMask	uint32_t	Hash table MSB register
HMSBResetValue	uint32_t	Hash table MSB register
HMSBWriteMask	uint32_t	Hash table MSB register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
MACLSB	uint32_t	MAC address LSB register
MACLSBColdResetValue	uint32_t	MAC address LSB register
MACLSBForcedBits	uint32_t	MAC address LSB register
MACLSBForcedFlippedBits	uint32_t	MAC address LSB register
MACLSBReadMask	uint32_t	MAC address LSB register
MACLSBResetMask	uint32_t	MAC address LSB register
MACLSBResetValue	uint32_t	MAC address LSB register
MACLSBWriteMask	uint32_t	MAC address LSB register
MACMSB	uint32_t	MAC address MSB register
MACMSBColdResetValue	uint32_t	MAC address MSB register
MACMSBForcedBits	uint32_t	MAC address MSB register
MACMSBForcedFlippedBits	uint32_t	MAC address MSB register
MACMSBReadMask	uint32_t	MAC address MSB register
MACMSBResetMask	uint32_t	MAC address MSB register
MACMSBResetValue	uint32_t	MAC address MSB register
MACMSBWriteMask	uint32_t	MAC address MSB register
MDIOColdResetValue	uint32_t	MDIO control and status register
MDIOForcedBits	uint32_t	MDIO control and status register
MDIOForcedFlippedBits	uint32_t	MDIO control and status register
MDIOReadMask	uint32_t	MDIO control and status register
MDIOResetMask	uint32_t	MDIO control and status register
MDIOResetValue	uint32_t	MDIO control and status register
MDIOWriteMask	uint32_t	MDIO control and status register
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
RXBASEColdResetValue	uint32_t	Receiver descriptor base address register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
RXBASEForcedBits	uint32_t	Receiver descriptor base address register
RXBASEForcedFlippedBits	uint32_t	Receiver descriptor base address register
RXBASEReadMask	uint32_t	Receiver descriptor base address register
RXBASEResetMask	uint32_t	Receiver descriptor base address register
RXBASEResetValue	uint32_t	Receiver descriptor base address register
RXBASEWriteMask	uint32_t	Receiver descriptor base address register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
STATColdResetValue	uint32_t	Status register
STATForcedBits	uint32_t	Status register
STATForcedFlippedBits	uint32_t	Status register
STATReadMask	uint32_t	Status register
STATResetMask	uint32_t	Status register
STATResetValue	uint32_t	Status register
STATWriteMask	uint32_t	Status register
TXBASEColdResetValue	uint32_t	Transmitter descriptor base address register
TXBASEForcedBits	uint32_t	Transmitter descriptor base address register
TXBASEForcedFlippedBits	uint32_t	Transmitter descriptor base address register
TXBASEReadMask	uint32_t	Transmitter descriptor base address register
TXBASEResetMask	uint32_t	Transmitter descriptor base address register
TXBASEResetValue	uint32_t	Transmitter descriptor base address register
TXBASEWriteMask	uint32_t	Transmitter descriptor base address register
TimeSource	*void	Time source object

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
config.checkCrc	uint8_t	Enable ethernet frame CRC checking.
config.checkIpCrc	uint8_t	Enable IP header CRC checking.
config.checkTcpCrc	uint8_t	Enable TCP header CRC checking.
config.checkUdpCrc	uint8_t	Enable UDP header CRC checking.
config.gbitVariant	uint8_t	Enable GRETH_GBIT behaviour.
config.generateCrc	uint8_t	Enable ethernet frame CRC generation.
config.irq	uint8_t	IRQ
config.littleEndian	uint8_t	Endianess of memory interface.
config.logTraffic	uint8_t	Enable traffic logging
irqCtrl	temu_IfaceRef/ <unknown>	IRQ controller.
mac	*char	Set MAC by string
mdioBus	temu_IfaceRef/ <unknown>	MDIO bus.
memAccess	temu_IfaceRef/ <unknown>	Memory access (for DMA).
phy	temu_IfaceRef/ <unknown>	PHY device.

Interfaces

Name	Type	Description
ApbIface	ApbIface	APB P&P interface
DeviceIface	DeviceIface	
MACIface	temu::MACIface	MAC interface
MemAccessIface	MemAccessIface	Mem access interface
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Registers



Register support is currently experimental!

Register Bank Regs

Register CTRL

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Description

Control register

Reset value

0x00000000

Warm reset mask

0xfe007fff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EA	BS			GA	MA	MC	-										ED	RD	DD	ME	PI	BM	GB	SP	RS	PM	FD	RI	TI	RE	TE
ro	ro			ro	ro	ro	-										rw	ro	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0			0	0	0	-										0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
EA	0x80000000	0x0	EDCL available
BS	0x70000000	0x0	EDCL buffer size
GA	0x08000000	0x0	Gigabit MAC available
MA	0x04000000	0x0	MDIO interrupts supported
MC	0x02000000	0x0	Multicast available
ED	0x00004000	0x0	EDCL disable
RD	0x00002000	0x0	RAM debug enable
DD	0x00001000	0x0	Disable duplex detection
ME	0x00000800	0x0	Multicast enable
PI	0x00000400	0x0	PHY status change interrupt enable
BM	0x00000200	0x0	Burst mode
GB	0x00000100	0x0	Gigabit speed mode
SP	0x00000080	0x0	Speed
RS	0x00000040	0x0	Reset
PM	0x00000020	0x0	Promiscuous mode
FD	0x00000010	0x0	Full duplex
RI	0x00000008	0x0	Receiver interrupt enable
TI	0x00000004	0x0	Transmitter interrupt enable
RE	0x00000002	0x0	Receive enable
TE	0x00000001	0x0	Transmit enable

Register STAT

Description

Status register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																							PS	IA	TS	TA	RA	TI	RI	TE	RE
-																							rw	rw	rw	rw	rw	rw	rw	rw	rw
-																							-	-	-	-	-	-	-	-	-

Field	Mask	Reset	Description
PS	0x00000100	-	PHY status changes
IA	0x00000080	-	Invalid address
TS	0x00000040	-	Too small
TA	0x00000020	-	Transmitter AHB error
RA	0x00000010	-	Receiver AHB error
TI	0x00000008	-	Transmit successful
RI	0x00000004	-	Receive successful
TE	0x00000002	-	Transmitter error
RE	0x00000001	-	Receiver error

Register MACMSB

Description

MAC address MSB register

Reset value

0x00000000

Warm reset mask

0x0000ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																MSB															
-																rw															
-																0															

Field	Mask	Reset	Description
MSB	0x0000ffff	0x0	Two most significant bytes of the MAC address

Register MACLSB

Description

MAC address LSB register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSB																															
rw																															
0																															

Field	Mask	Reset	Description
LSB	0xffffffff	0x0	Four least significant bytes of the MAC address

Register MDIO

Description

MDIO control and status register

Reset value

0x00000000

Warm reset mask

0xffffffcf

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																PHYADDR					REGADDR					-		BU		LF	RD	WR
rw																rw					rw					-		ro		ro	rw	rw
0																0					0					-		0		0	0	0

Field	Mask	Reset	Description
DATA	0xffff0000	0x0	Data
PHYADDR	0x0000f800	0x0	PHY address
REGADDR	0x000007c0	0x0	Register address
BU	0x00000008	0x0	Busy
LF	0x00000004	0x0	Link fail
RD	0x00000002	0x0	Read
WR	0x00000001	0x0	Write

Register TXBASE

Description

Transmitter descriptor base address register

Reset value

0x00000000

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Warm reset mask

0xfffffff8

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3	2 1 0
BASEADDR	DESCPNT	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
BASEADDR	0xfffffc00	0x0	Transmitter descriptor table base address
DESCPNT	0x000003f8	0x0	Descriptor pointer

Register RXBASE

Description

Receiver descriptor base address register

Reset value

0x00000000

Warm reset mask

0xfffffff8

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3	2 1 0
BASEADDR	DESCPNT	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
BASEADDR	0xfffffc00	0x0	Receiver descriptor table base address
DESCPNT	0x000003f8	0x0	Descriptor pointer

Register EDCLIP

Description

EDCL IP register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
IP
rw
0

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IP	0xffffffff	0x0	EDCL IP address

Register HMSB

Description

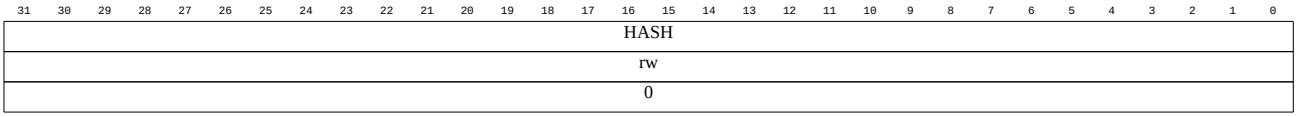
Hash table MSB register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
HASH	0xffffffff	0x0	Hash table MSB

Register HLSB

Description

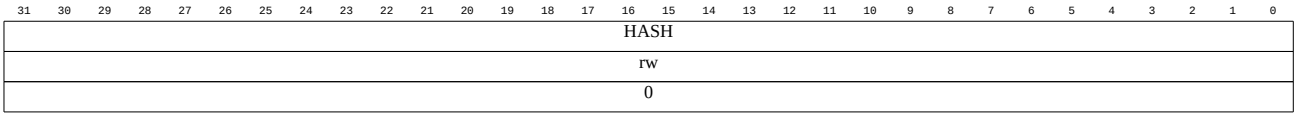
Hash table LSB register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
HASH	0xffffffff	0x0	Hash table LSB

Register EMACMSB

Description

EDCL MAC address MSB register

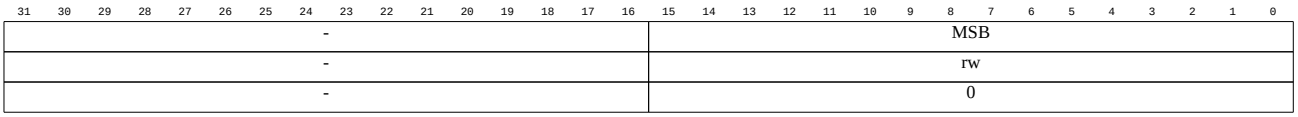
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0x0000ffff



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																MSB															
-																rw															
-																0															

Field	Mask	Reset	Description
MSB	0x0000ffff	0x0	Two most significant bytes of the EDCL MAC address

Register EMACLSB

Description

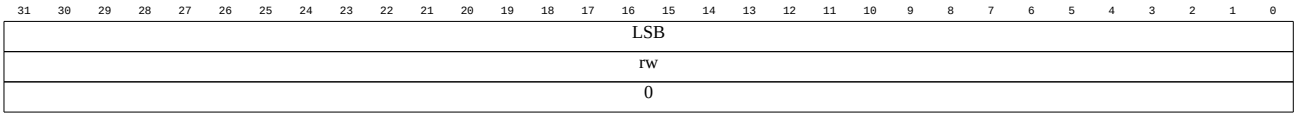
EDCL MAC address LSB register

Reset value

0x00000000

Warm reset mask

0xffffffff



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSB																															
rw																															
0																															

Field	Mask	Reset	Description
LSB	0xffffffff	0x0	Four least significant bytes of the EDCL MAC address

Commands

Name	Description
delete	Dispose instance of GRETH
sendFrame	Send frame
setMAC	Set MAC address

Command sendFrame Arguments

Name	Type	Required	Description
mac	string	yes	MAC address of target

Command setMAC Arguments

Name	Type	Required	Description
mac	string	yes	MAC address to set

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9.6.5. Limitations

- Multicast groups are not yet supported.
- ECDL mode is not supported.

9.7. GRGPIO

The GRGPIO device is part of the GRLIB device library from Gaisler. The GrGPIO model simulates a 16 pin GPIO device by providing input and output via the SignalIface.

9.7.1. Loading the Plugin

```
import GrGPIO
```

9.7.2. Usage

The device can be connected to and from via the signal interface it implements. It implements 16 usable signals (signal 0 through 15). Signal 0 cannot raise interrupts.

You can connect the signal interface as follows:

Listing 21. Connecting via Command Line

```
# Connect GPIO device signal 0 to device model
connect a=gpio.outSignals[0] b=mydevice:SignalIface

# Connect a device signal interface ref to GPIO device
connect a=mydevice.signal b=gpio:SignalIface[1]
```

Listing 22. Connecting via API

```
// Connect GPIO device signal 0 to device model
temu_connect(gpio, "outSignals[0]", mydevice, "SignalIface");

// Connect a device signal interface ref to GPIO device
temu_connect(mydevice, "signal", gpio, "SignalIface[1]");
```

9.7.3. @GrGPIO Reference

Properties

Name	Type	Description
Class	*void	Class object

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GrGPIO
new	Create new instance of GrGPIO

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.7.4. GrGPIO Reference

Properties

Name	Type	Description
BYPASSColdResetValue	uint32_t	Bypass register
BYPASSForcedBits	uint32_t	Bypass register
BYPASSForcedFlippedBits	uint32_t	Bypass register
BYPASSReadMask	uint32_t	Bypass register
BYPASSResetMask	uint32_t	Bypass register
BYPASSResetValue	uint32_t	Bypass register
BYPASSWriteMask	uint32_t	Bypass register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
CAPColdResetValue	uint32_t	Capability register
CAPForcedBits	uint32_t	Capability register
CAPForcedFlippedBits	uint32_t	Capability register
CAPReadMask	uint32_t	Capability register
CAPResetMask	uint32_t	Capability register
CAPResetValue	uint32_t	Capability register
CAPWriteMask	uint32_t	Capability register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
DATAColdResetValue	uint32_t	I/O port data register
DATAForcedBits	uint32_t	I/O port data register
DATAForcedFlippedBits	uint32_t	I/O port data register
DATAReadMask	uint32_t	I/O port data register
DATAResetMask	uint32_t	I/O port data register
DATAResetValue	uint32_t	I/O port data register
DATAWriteMask	uint32_t	I/O port data register
DIRECTIONColdResetValue	uint32_t	I/O port direction register
DIRECTIONForcedBits	uint32_t	I/O port direction register
DIRECTIONForcedFlippedBits	uint32_t	I/O port direction register
DIRECTIONReadMask	uint32_t	I/O port direction register
DIRECTIONResetMask	uint32_t	I/O port direction register
DIRECTIONResetValue	uint32_t	I/O port direction register
DIRECTIONWriteMask	uint32_t	I/O port direction register
IAVAILColdResetValue	uint32_t	Interrupt available register
IAVAILForcedBits	uint32_t	Interrupt available register
IAVAILForcedFlippedBits	uint32_t	Interrupt available register
IAVAILReadMask	uint32_t	Interrupt available register
IAVAILResetMask	uint32_t	Interrupt available register
IAVAILResetValue	uint32_t	Interrupt available register
IAVAILWriteMask	uint32_t	Interrupt available register
IEDGEColdResetValue	uint32_t	Interrupt edge register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
IEDGEForcedBits	uint32_t	Interrupt edge register
IEDGEForcedFlippedBits	uint32_t	Interrupt edge register
IEDGEReadMask	uint32_t	Interrupt edge register
IEDGEResetMask	uint32_t	Interrupt edge register
IEDGEResetValue	uint32_t	Interrupt edge register
IEDGEWriteMask	uint32_t	Interrupt edge register
IFLAGColdResetValue	uint32_t	Interrupt flag register
IFLAGForcedBits	uint32_t	Interrupt flag register
IFLAGForcedFlippedBits	uint32_t	Interrupt flag register
IFLAGReadMask	uint32_t	Interrupt flag register
IFLAGResetMask	uint32_t	Interrupt flag register
IFLAGResetValue	uint32_t	Interrupt flag register
IFLAGWriteMask	uint32_t	Interrupt flag register
IMASKColdResetValue	uint32_t	Interrupt mask register
IMASKForcedBits	uint32_t	Interrupt mask register
IMASKForcedFlippedBits	uint32_t	Interrupt mask register
IMASKReadMask	uint32_t	Interrupt mask register
IMASKResetMask	uint32_t	Interrupt mask register
IMASKResetValue	uint32_t	Interrupt mask register
IMASKWriteMask	uint32_t	Interrupt mask register
IPENColdResetValue	uint32_t	Input enable register
IPENForcedBits	uint32_t	Input enable register
IPENForcedFlippedBits	uint32_t	Input enable register
IPENReadMask	uint32_t	Input enable register
IPENResetMask	uint32_t	Input enable register
IPENResetValue	uint32_t	Input enable register
IPENWriteMask	uint32_t	Input enable register
IPOLColdResetValue	uint32_t	Interrupt polarity register
IPOLForcedBits	uint32_t	Interrupt polarity register
IPOLForcedFlippedBits	uint32_t	Interrupt polarity register
IPOLReadMask	uint32_t	Interrupt polarity register
IPOLResetMask	uint32_t	Interrupt polarity register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
IPOLResetValue	uint32_t	Interrupt polarity register
IPOLWriteMask	uint32_t	Interrupt polarity register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
OUTPUTColdResetValue	uint32_t	I/O port output register
OUTPUTForcedBits	uint32_t	I/O port output register
OUTPUTForcedFlippedBits	uint32_t	I/O port output register
OUTPUTReadMask	uint32_t	I/O port output register
OUTPUTResetMask	uint32_t	I/O port output register
OUTPUTResetValue	uint32_t	I/O port output register
OUTPUTWriteMask	uint32_t	I/O port output register
ObjectID	uint64_t	Unique ObjectID.
PULSEColdResetValue	uint32_t	Pulse register
PULSEForcedBits	uint32_t	Pulse register
PULSEForcedFlippedBits	uint32_t	Pulse register
PULSEReadMask	uint32_t	Pulse register
PULSEResetMask	uint32_t	Pulse register
PULSEResetValue	uint32_t	Pulse register
PULSEWriteMask	uint32_t	Pulse register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
bypass	uint32_t	Bypass register
capability	uint32_t	Capability register
config.inputEnable	uint8_t	
config.irqFlag	uint8_t	
config.irqGen	uint8_t	
config.irqMask	uint32_t	
config.littleEndian	uint8_t	Endianess of memory interface.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
config.pinMask	uint32_t	
config.pirq	uint8_t	
config.pulse	uint8_t	
data	uint32_t	I/O port data register
direction	uint32_t	I/O port direction register
edge	uint32_t	Interrupt edge register
inputEnable	uint32_t	Input enable register
irqAvailable	uint32_t	Interrupt available register
irqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller
irqFlag	uint32_t	Interrupt flag register
irqMap	[uint32_t; 8]	Interrupt map register
mask	uint32_t	Interrupt mask register
outSignals	[temu_IfaceRef; 32]/ <unknown>	GPIO signals
output	uint32_t	I/O port output register
pnp.bar	uint32_t	
pnp.config	uint32_t	
polarity	uint32_t	Interrupt polarity register
pulse	uint32_t	Pulse register

Interfaces

Name	Type	Description
ApbIface	ApbIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
PulseIface	SignalIface	Pulse signals
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	
SignalIface	SignalIface	Incoming signals

Registers



Register support is currently experimental!

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Register Bank Regs

Register DATA

Description

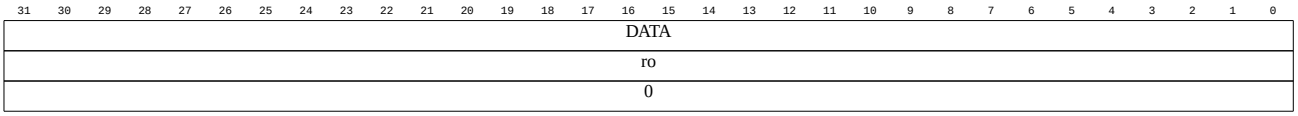
I/O port data register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
DATA	0xffffffff	0x0	I/O port input value

Register OUTPUT

Description

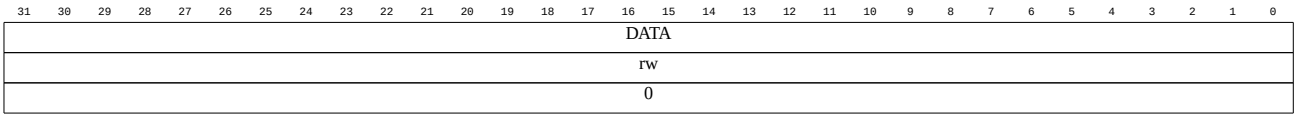
I/O port output register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
DATA	0xffffffff	0x0	I/O port output value

Register DIRECTION

Description

I/O port direction register

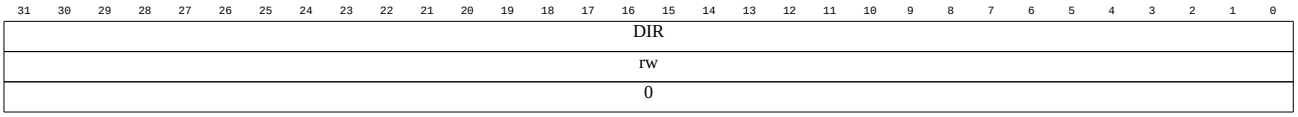
Reset value

0x00000000

Warm reset mask

0xffffffff

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Field	Mask	Reset	Description
DIR	0xffffffff	0x0	I/O port direction value

Register IMASK

Description

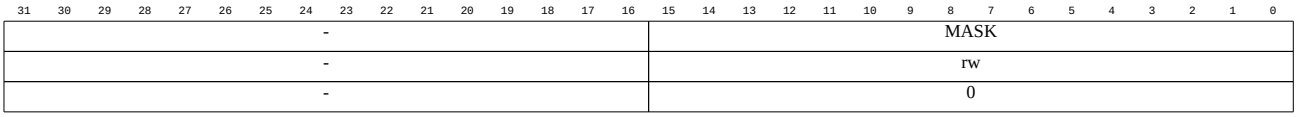
Interrupt mask register

Reset value

0x00000000

Warm reset mask

0x0000ffff



Field	Mask	Reset	Description
MASK	0x0000ffff	0x0	Interrupt mask

Register IPOL

Description

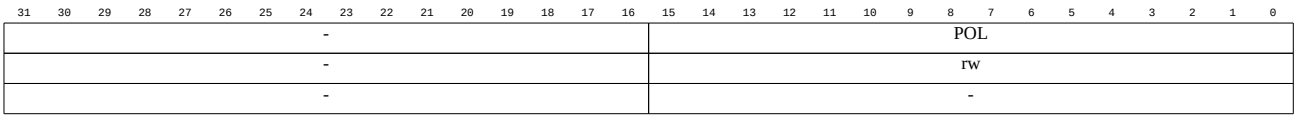
Interrupt polarity register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
POL	0x0000ffff	-	Interrupt polarity

Register IEDGE

Description

Interrupt edge register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																EDGE															
-																rw															
-																-															

Field	Mask	Reset	Description
EDGE	0x0000ffff	-	Interrupt edge

Register BYPASS

Description

Bypass register

Reset value

0x00000000

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
rw																															
0																															

Field	Mask	Reset	Description
DATA	0xffffffff	0x0	Bypass alternate function selection

Register CAP

Description

Capability register

Reset value

0x00010400

Warm reset mask

0x00071f1f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-													PU	IER	IFL	-			IRQGEN					-			NLINES			
-													ro	ro	ro	-			ro					-			ro			
-													0	0	1	-			4					-			0			

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
PU	0x00040000	0x0	Pulse register implemented
IER	0x00020000	0x0	Input enable register implemented
IFL	0x00010000	0x1	Interrupt flag register implemented
IRQGEN	0x00001f00	0x4	Interrupt generation setting
NLINES	0x0000001f	0x0	Number of pins in GPIO port minus one

Register IAVAIL

Description

Interrupt available register

Reset value

0x0000ffff

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMASK																															
ro																															
65535																															

Field	Mask	Reset	Description
IMASK	0xffffffff	0xffff	Interrupt available bit field

Register IFLAG

Description

Interrupt flag register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																IFLAG															
-																rw															
-																-															

Field	Mask	Reset	Description
IFLAG	0x0000ffff	-	Interrupt flag

Register IPEN

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Input enable register

Reset value

0x00000000

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
rw																															
0																															

Field	Mask	Reset	Description
DATA	0xffffffff	0x0	Input enable value

Register PULSE

Description

Pulse register

Reset value

0x00000000

Warm reset mask

0x0000ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																PULSE															
-																rw															
-																0															

Field	Mask	Reset	Description
PULSE	0x0000ffff	0x0	Pulse enable

Register IPEN_OR

Description

Input enable register, logical-OR

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
wo																															
-																															

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
DATA	0xffffffff	-	Input enable logical-OR

Register OUTPUT_OR

Description

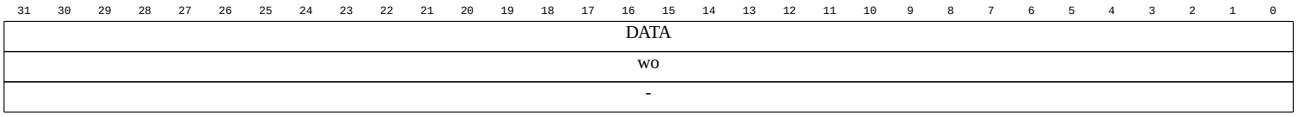
I/O port output register, logical-OR

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
DATA	0xffffffff	-	I/O port output logical-OR

Register DIRECTION_OR

Description

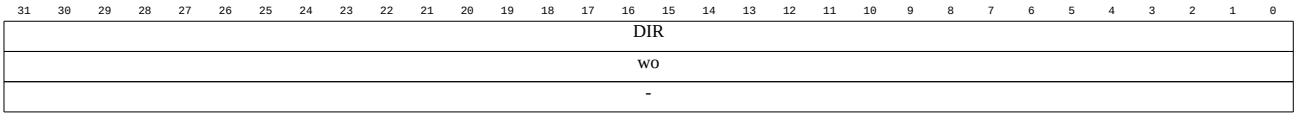
I/O port direction register, logical-OR

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
DIR	0xffffffff	-	I/O port direction logical-OR

Register IMASK_OR

Description

Interrupt mask register, logical-OR

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																MASK															
-																wo															
-																-															

Field	Mask	Reset	Description
MASK	0x0000ffff	-	Interrupt mask logical-OR

Register IPEN_AND

Description

Input enable register, logical-AND

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
wo																															
-																															

Field	Mask	Reset	Description
DATA	0xffffffff	-	Input enable logical-AND

Register OUTPUT_AND

Description

I/O port output register, logical-AND

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
wo																															
-																															

Field	Mask	Reset	Description
DATA	0xffffffff	-	I/O port output logical-AND

Register DIRECTION_AND

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

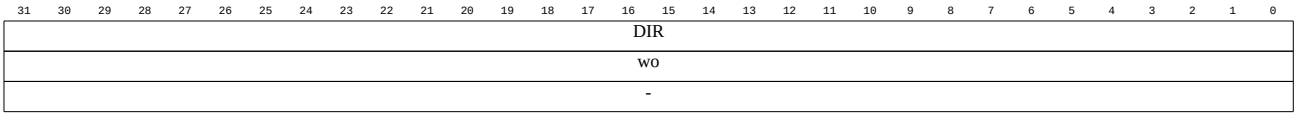
I/O port direction register, logical-AND

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
DIR	0xffffffff	-	I/O port direction logical-AND

Register IMASK_AND

Description

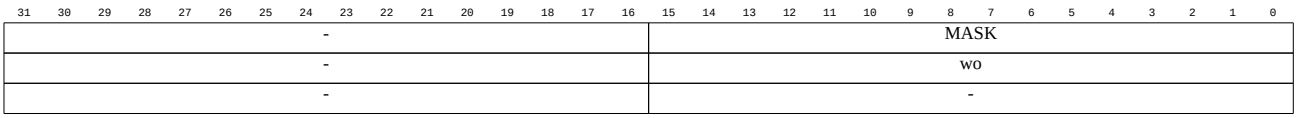
Interrupt mask register, logical-AND

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
MASK	0x0000ffff	-	Interrupt mask logical-AND

Register IPEN_XOR

Description

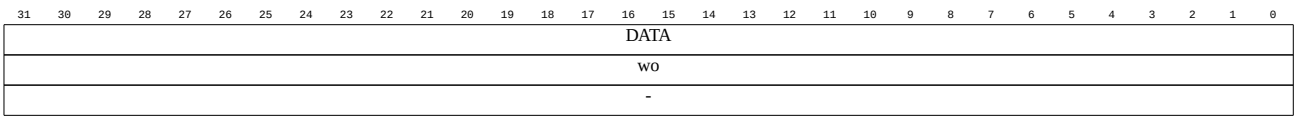
Input enable register, logical-XOR

Reset value

0x00000000

Warm reset mask

0x00000000



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
DATA	0xffffffff	-	Input enable logical-XOR

Register OUTPUT_XOR

Description

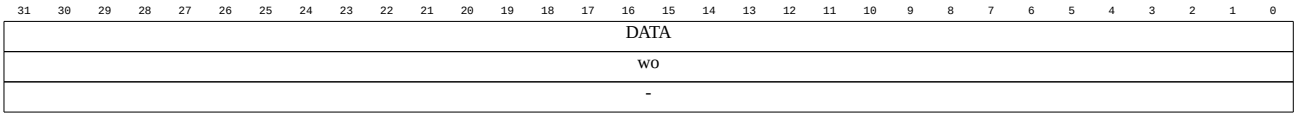
I/O port output register, logical-XOR

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
DATA	0xffffffff	-	I/O port output logical-XOR

Register DIRECTION_XOR

Description

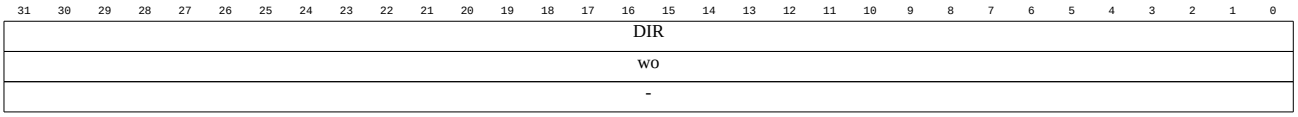
I/O port direction register, logical-XOR

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
DIR	0xffffffff	-	I/O port direction logical-XOR

Register IMASK_XOR

Description

Interrupt mask register, logical-XOR

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0x00000000

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
-	MASK
-	wo
-	-

Field	Mask	Reset	Description
MASK	0x0000ffff	-	Interrupt mask logical-XOR

Register IRQMAPR

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0x1f1f1f1f

31 30 29	28 27 26 25 24	23 22 21	20 19 18 17 16	15 14 13	12 11 10 9 8	7 6 5	4 3 2 1 0
-	IRQMAP3	-	IRQMAP2	-	IRQMAP1	-	IRQMAP0
-	rw	-	rw	-	rw	-	rw
-	0	-	0	-	0	-	0

Field	Mask	Reset	Description
IRQMAP3	0x1f000000	0x0	Interrupt map field for GPIO line n+3
IRQMAP2	0x001f0000	0x0	Interrupt map field for GPIO line n+2
IRQMAP1	0x00001f00	0x0	Interrupt map field for GPIO line n+1
IRQMAP0	0x0000001f	0x0	Interrupt map field for GPIO line n

Register IRQMAPR

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0x1f1f1f1f

31 30 29	28 27 26 25 24	23 22 21	20 19 18 17 16	15 14 13	12 11 10 9 8	7 6 5	4 3 2 1 0
-	IRQMAP3	-	IRQMAP2	-	IRQMAP1	-	IRQMAP0
-	rw	-	rw	-	rw	-	rw
-	0	-	0	-	0	-	0

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IRQMAP3	0x1f000000	0x0	Interrupt map field for GPIO line n+3
IRQMAP2	0x001f0000	0x0	Interrupt map field for GPIO line n+2
IRQMAP1	0x00001f00	0x0	Interrupt map field for GPIO line n+1
IRQMAP0	0x0000001f	0x0	Interrupt map field for GPIO line n

Register IRQMAPR

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0x1f1f1f1f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-			IRQMAP3					-			IRQMAP2					-			IRQMAP1					-			IRQMAP0				
-			rw					-			rw					-			rw					-			rw				
-			0					-			0					-			0					-			0				

Field	Mask	Reset	Description
IRQMAP3	0x1f000000	0x0	Interrupt map field for GPIO line n+3
IRQMAP2	0x001f0000	0x0	Interrupt map field for GPIO line n+2
IRQMAP1	0x00001f00	0x0	Interrupt map field for GPIO line n+1
IRQMAP0	0x0000001f	0x0	Interrupt map field for GPIO line n

Register IRQMAPR

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0x1f1f1f1f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-			IRQMAP3					-			IRQMAP2					-			IRQMAP1					-			IRQMAP0				
-			rw					-			rw					-			rw					-			rw				
-			0					-			0					-			0					-			0				

Field	Mask	Reset	Description
IRQMAP3	0x1f000000	0x0	Interrupt map field for GPIO line n+3

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IRQMAP2	0x001f0000	0x0	Interrupt map field for GPIO line n+2
IRQMAP1	0x00001f00	0x0	Interrupt map field for GPIO line n+1
IRQMAP0	0x0000001f	0x0	Interrupt map field for GPIO line n

Register IRQMAPR

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0x1f1f1f1f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-			IRQMAP3					-			IRQMAP2					-			IRQMAP1					-			IRQMAP0				
-			rw					-			rw					-			rw					-			rw				
-			0					-			0					-			0					-			0				

Field	Mask	Reset	Description
IRQMAP3	0x1f000000	0x0	Interrupt map field for GPIO line n+3
IRQMAP2	0x001f0000	0x0	Interrupt map field for GPIO line n+2
IRQMAP1	0x00001f00	0x0	Interrupt map field for GPIO line n+1
IRQMAP0	0x0000001f	0x0	Interrupt map field for GPIO line n

Register IRQMAPR

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0x1f1f1f1f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-			IRQMAP3					-			IRQMAP2					-			IRQMAP1					-			IRQMAP0				
-			rw					-			rw					-			rw					-			rw				
-			0					-			0					-			0					-			0				

Field	Mask	Reset	Description
IRQMAP3	0x1f000000	0x0	Interrupt map field for GPIO line n+3
IRQMAP2	0x001f0000	0x0	Interrupt map field for GPIO line n+2

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IRQMAP1	0x00001f00	0x0	Interrupt map field for GPIO line n+1
IRQMAP0	0x0000001f	0x0	Interrupt map field for GPIO line n

Register IRQMAPR

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0x1f1f1f1f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-			IRQMAP3					-			IRQMAP2					-			IRQMAP1					-			IRQMAP0				
-			rw					-			rw					-			rw					-			rw				
-			0					-			0					-			0					-			0				

Field	Mask	Reset	Description
IRQMAP3	0x1f000000	0x0	Interrupt map field for GPIO line n+3
IRQMAP2	0x001f0000	0x0	Interrupt map field for GPIO line n+2
IRQMAP1	0x00001f00	0x0	Interrupt map field for GPIO line n+1
IRQMAP0	0x0000001f	0x0	Interrupt map field for GPIO line n

Register IRQMAPR

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0x1f1f1f1f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-			IRQMAP3					-			IRQMAP2					-			IRQMAP1					-			IRQMAP0				
-			rw					-			rw					-			rw					-			rw				
-			0					-			0					-			0					-			0				

Field	Mask	Reset	Description
IRQMAP3	0x1f000000	0x0	Interrupt map field for GPIO line n+3
IRQMAP2	0x001f0000	0x0	Interrupt map field for GPIO line n+2
IRQMAP1	0x00001f00	0x0	Interrupt map field for GPIO line n+1

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IRQMAP0	0x0000001f	0x0	Interrupt map field for GPIO line n

Commands

Name	Description
delete	Dispose instance of GrGPIO

9.7.5. Limitations

- Only the UT700 based configuration is supported at the moment. That means that the bypass and capabilities registers are missing. Further the IRQ map registers are not available.

9.8. GRIOMMU

The GRIOMMU model is available in the GrIoMmu plugin.

9.8.1. Loading the Plugin

```
import GrIoMmu
```

9.8.2. Configuration

The model should be attached in two directions:

Firstly, IO-devices need to have their memory access interface references routed through the IOMMU. To do this, connect the memory access iface ref in the device to `IOMMUAccessIface` in the IOMMU.

Secondly, the IOMMU needs to get access to the device's AMBA PNP info. The info is used to populate the `MasterConfig` registers. To set the PNP info, attach it to the `devicePnp` array.

The `IOMMUAccessIface` and `devicePnp` array assumes that the same device indexes are used. Not connecting devices the correct way is undefined behaviour.

Listing 23. Connecting the GRIOMMU

```
// Connect command
connect a=iommu.devicePnp[0] b=device:ApbIface ①
connect a=device.mem b=iommu:IOMMUAccessIface[0] ②

// Or with assigmment syntax
iommu.devicePnp[0] = device:ApbIface ①
device.mem = iommu:IOMMUAccessIface[0] ②
```

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

① Index should match index on next line.

② Index should match index on previous line.

9.8.3. @GRIOMMU Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GRIOMMU
new	Create new instance of GRIOMMU

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.8.4. GRIOMMU Reference

Properties

Name	Type	Description
AHBFASColdResetValue	uint32_t	AHB failing access register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
AHBFASForcedBits	uint32_t	AHB failing access register
AHBFASForcedFlippedBits	uint32_t	AHB failing access register
AHBFASReadMask	uint32_t	AHB failing access register
AHBFASResetMask	uint32_t	AHB failing access register
AHBFASResetValue	uint32_t	AHB failing access register
AHBFASWriteMask	uint32_t	AHB failing access register
CTRLColdResetValue	uint32_t	Control register
CTRLForcedBits	uint32_t	Control register
CTRLForcedFlippedBits	uint32_t	Control register
CTRLReadMask	uint32_t	Control register
CTRLResetMask	uint32_t	Control register
CTRLResetValue	uint32_t	Control register
CTRLWriteMask	uint32_t	Control register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
DERRIColdResetValue	uint32_t	Data RAM error injection register
DERRIForcedBits	uint32_t	Data RAM error injection register
DERRIForcedFlippedBits	uint32_t	Data RAM error injection register
DERRIReadMask	uint32_t	Data RAM error injection register
DERRIResetMask	uint32_t	Data RAM error injection register
DERRIResetValue	uint32_t	Data RAM error injection register
DERRIWriteMask	uint32_t	Data RAM error injection register
DIAGCTRLColdResetValue	uint32_t	Diagnostic cache access register
DIAGCTRLForcedBits	uint32_t	Diagnostic cache access register
DIAGCTRLForcedFlippedBits	uint32_t	Diagnostic cache access register
DIAGCTRLReadMask	uint32_t	Diagnostic cache access register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DIAGCTRLResetMask	uint32_t	Diagnostic cache access register
DIAGCTRLResetValue	uint32_t	Diagnostic cache access register
DIAGCTRLWriteMask	uint32_t	Diagnostic cache access register
DIAGTColdResetValue	uint32_t	Diagnostic cache access tag register
DIAGTForcedBits	uint32_t	Diagnostic cache access tag register
DIAGTForcedFlippedBits	uint32_t	Diagnostic cache access tag register
DIAGTReadMask	uint32_t	Diagnostic cache access tag register
DIAGTResetMask	uint32_t	Diagnostic cache access tag register
DIAGTResetValue	uint32_t	Diagnostic cache access tag register
DIAGTWriteMask	uint32_t	Diagnostic cache access tag register
FLUSHColdResetValue	uint32_t	TLB/cache flush register
FLUSHForcedBits	uint32_t	TLB/cache flush register
FLUSHForcedFlippedBits	uint32_t	TLB/cache flush register
FLUSHReadMask	uint32_t	TLB/cache flush register
FLUSHResetMask	uint32_t	TLB/cache flush register
FLUSHResetValue	uint32_t	TLB/cache flush register
FLUSHWriteMask	uint32_t	TLB/cache flush register
IMASKColdResetValue	uint32_t	Interrupt mask register
IMASKForcedBits	uint32_t	Interrupt mask register
IMASKForcedFlippedBits	uint32_t	Interrupt mask register
IMASKReadMask	uint32_t	Interrupt mask register
IMASKResetMask	uint32_t	Interrupt mask register
IMASKResetValue	uint32_t	Interrupt mask register
IMASKWriteMask	uint32_t	Interrupt mask register
LocalName	*char	Local name (in component, if applicable)

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
STATUSColdResetValue	uint32_t	Status register
STATUSForcedBits	uint32_t	Status register
STATUSForcedFlippedBits	uint32_t	Status register
STATUSReadMask	uint32_t	Status register
STATUSResetMask	uint32_t	Status register
STATUSResetValue	uint32_t	Status register
STATUSWriteMask	uint32_t	Status register
TERRIColdResetValue	uint32_t	Tag RAM error injection register
TERRIForcedBits	uint32_t	Tag RAM error injection register
TERRIForcedFlippedBits	uint32_t	Tag RAM error injection register
TERRIReadMask	uint32_t	Tag RAM error injection register
TERRIResetMask	uint32_t	Tag RAM error injection register
TERRIResetValue	uint32_t	Tag RAM error injection register
TERRIWriteMask	uint32_t	Tag RAM error injection register
TimeSource	*void	Time source object
abhFailingAccess	uint32_t	AHB failing access register
asmpAccessControl	[uint32_t; 4]	ASMP access control register
capbility	[uint32_t; 3]	Capability register
config.interrupt	uint8_t	Interrupt number
config.littleEndian	uint8_t	Endianess of memory interface.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
control	uint32_t	Control register
dataRamErrorInjection	uint32_t	Data RAM error injection register
devicePnp	[temu_IfaceRef; 16]/ <unknown>	Devices under IOMMU control
diagnosticCacheAccess	uint32_t	Diagnostic cache access register
diagnosticCacheAccessData	[uint32_t; 8]	Diagnostic cache access data register
diagnosticCacheAccessTag	uint32_t	Diagnostic cache access tag register
groupConfig	[uint32_t; 16]	Group control register
irq	temu_IfaceRef/ <unknown>	ASMP access control register
irqMask	uint32_t	Interrupt mask register
masterConfig	[uint32_t; 16]	Master configuration register
masterPnp.bar	[uint32_t; 4]	AMBA plug and play base address register
masterPnp.ident	uint32_t	AMBA plug and play config word
masterPnp.user	[uint32_t; 3]	AMBA plug and play user words
mem	temu_IfaceRef/ <unknown>	Main memory bus
secondaryMasterPnp.bar	[uint32_t; 4]	AMBA plug and play base address register
secondaryMasterPnp.ident	uint32_t	AMBA plug and play config word
secondaryMasterPnp.user	[uint32_t; 3]	AMBA plug and play user words
slavePnp.bar	[uint32_t; 4]	AMBA plug and play base address register
slavePnp.ident	uint32_t	AMBA plug and play config word
slavePnp.user	[uint32_t; 3]	AMBA plug and play user words
status	uint32_t	Status register
tagRamErrorInjection	uint32_t	Tag RAM error injection register
tlbCacheFlush	uint32_t	TLB/cache flush register

Interfaces

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DeviceIface	DeviceIface	
IOMMUAccessIface	MemAccessIface	IOMMU memory access interfaces
MasterAhbIface	AhbIface	Master AHB interfaces
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	
SlaveAhbIface	AhbIface	

Registers



Register support is currently experimental!

Register Bank Regs

Register CTRL

Description

Control register

Reset value

0x00000000

Warm reset mask

0x001fffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-											PGSZ			LB	SP	ITR				DP	SIV	HPROT		AU	WP	DM	GS	CE	PM		EN	
-											rw			rw	ro	rw				rw	rw	rw		rw	rw	rw	rw	rw	rw		rw	
-											0			0	0	0				0	0	0		0	0	0	0	0	0		0	

Field	Mask	Reset	Description
PGSZ	0x001c0000	0x0	Page size
LB	0x00020000	0x0	Lookup bus
SP	0x00010000	0x0	SPLIT support
ITR	0x0000f000	0x0	IOMMU translation range
DP	0x00000800	0x0	Disable prefetch
SIV	0x00000400	0x0	Save invalid IOPTE
HPROT	0x00000300	0x0	HPROT encoding
AU	0x00000080	0x0	Always update

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Field	Mask	Reset	Description
WP	0x00000040	0x0	Write protection only
DM	0x00000020	0x0	Diagnostic mode
GS	0x00000010	0x0	Group-set-addressing
CE	0x00000008	0x0	Cache/TLB enable
PM	0x00000006	0x0	Protection mode
EN	0x00000001	0x0	Enable

Register FLUSH

Description

TLB/cache flush register

Reset value

0x00000000

Warm reset mask

0x000000f3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								FGRP				-		GF	F
-																								rw				-		rw	rw
-																								0				-		0	0

Field	Mask	Reset	Description
FGRP	0x000000f0	0x0	Flush group
GF	0x00000002	0x0	Group flush
F	0x00000001	0x0	Flush

Register STATUS

Description

Status register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																										PE	DE	FC	FL	AD	TE
-																										rw	rw	rw	rw	rw	rw
-																										-	-	-	-	-	-

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
PE	0x00000020	-	Parity error
DE	0x00000010	-	Diagnostic mode enabled
FC	0x00000008	-	Flush completed
FL	0x00000004	-	Flush started
AD	0x00000002	-	Access denied
TE	0x00000001	-	Translation error

Register IMASK

Description

Interrupt mask register

Reset value

0x00000000

Warm reset mask

0x0000002f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																										PEI	-	FCI	FLI	ADI	TEI
-																										rw	-	rw	rw	rw	rw
-																										0	-	0	0	0	0

Field	Mask	Reset	Description
PEI	0x00000020	0x0	Parity error interrupt
FCI	0x00000008	0x0	Flush completed interrupt
FLI	0x00000004	0x0	Flush started interrupt
ADI	0x00000002	0x0	Access denied interrupt
TEI	0x00000001	0x0	Translation error interrupt

Register AHBFAS

Description

AHB failing access register

Reset value

0x00000000

Warm reset mask

0xffffffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FADDR																											FW	FMASTER		
ro																											ro	ro		
0																											0	0		

Field	Mask	Reset	Description
FADDR	0xfffffffe0	0x0	Failing address
FW	0x00000010	0x0	Failing write
FMASTER	0x0000000f	0x0	Failing master

Register DIAGCTRL

Description

Diagnostic cache access register

Reset value

0x00000000

Warm reset mask

0xc037ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA	RW	-								DP	TP	-	SETADDR																		
rw	rw	-								ro	ro	-	rw																		
0	0	-								0	0	-	0																		

Field	Mask	Reset	Description
DA	0x80000000	0x0	Diagnostic access
RW	0x40000000	0x0	Read/write
DP	0x00200000	0x0	Data parity error
TP	0x00100000	0x0	Tag parity error
SETADDR	0x0007ffff	0x0	Cache set address

Register DIAGT

Description

Diagnostic cache access tag register

Reset value

0x00000000

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAG																															V
rw																															rw
0																															0

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
TAG	0xfffffffe	0x0	Cache tag
V	0x00000001	0x0	Valid

Register DERRI

Description

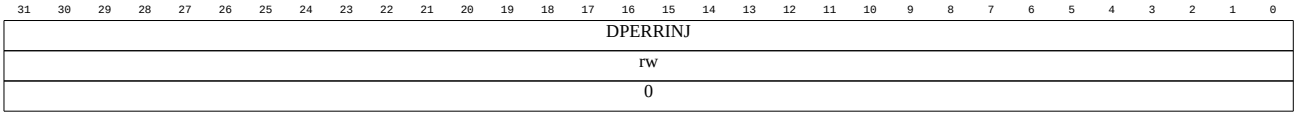
Data RAM error injection register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
DPERRINJ	0xffffffff	0x0	Data RAM parity error injection

Register TERRI

Description

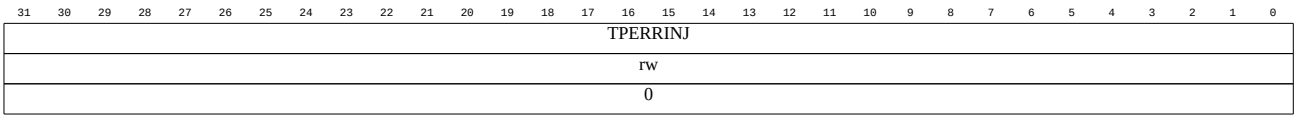
Tag RAM error injection register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TPERRINJ	0xffffffff	0x0	Tag RAM parity error injection

Register CAP

Description

Capability register

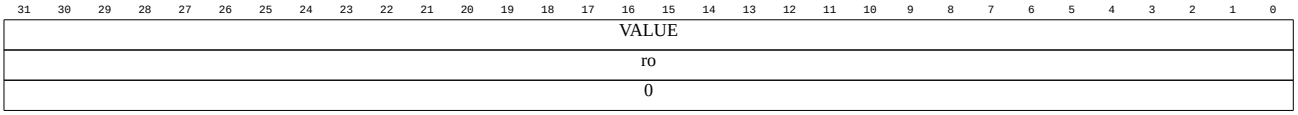
The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	Capability register value

Register CAP

Description

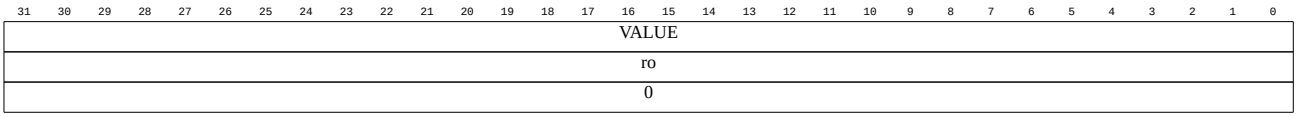
Capability register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	Capability register value

Register CAP

Description

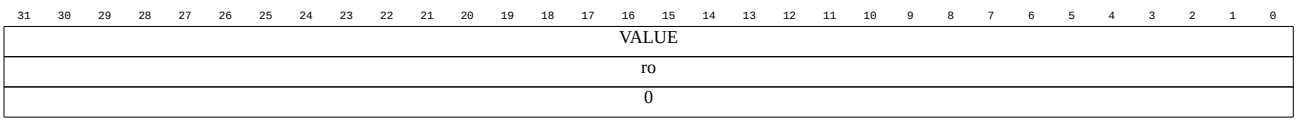
Capability register

Reset value

0x00000000

Warm reset mask

0xffffffff



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Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	Capability register value

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

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Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

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Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

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31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

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Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5	4	3 2 1 0
VENDOR	DEVICE	-	BS	GROUP
ro	ro	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register MSTCFG

Description

Master configuration register

Reset value

0x00000000

Warm reset mask

0xfffff01f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VENDOR								DEVICE												-								BS		GROUP	
ro								ro												-								rw		rw	
0								0												-								0		0	

Field	Mask	Reset	Description
VENDOR	0xff000000	0x0	GRLIB plug and play vendor ID
DEVICE	0x00fff000	0x0	GRLIB plug and play device ID
BS	0x00000010	0x0	Bus select for master
GROUP	0x0000000f	0x0	Group assignment for master

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register GRPCTRL

Description

Group control register

Reset value

0x00000000

Warm reset mask

0xfffffff3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																												-		P	AG
rw																												-		rw	rw
0																												-		0	0

Field	Mask	Reset	Description
BASE	0xfffffff0	0x0	Base address
P	0x00000002	0x0	Pass-through
AG	0x00000001	0x0	Active group

Register DIAGD

Description

Diagnostic cache access data register

Reset value

0x00000000

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDATA																															
rw																															
0																															

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
CDATA	0xffffffff	0x0	Cache data word

Register DIAGD

Description

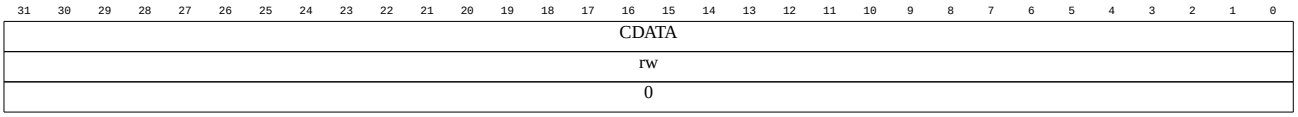
Diagnostic cache access data register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CDATA	0xffffffff	0x0	Cache data word

Register DIAGD

Description

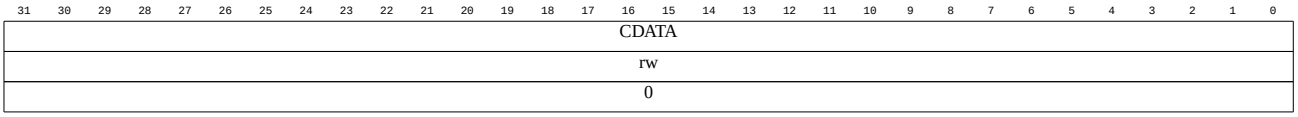
Diagnostic cache access data register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CDATA	0xffffffff	0x0	Cache data word

Register DIAGD

Description

Diagnostic cache access data register

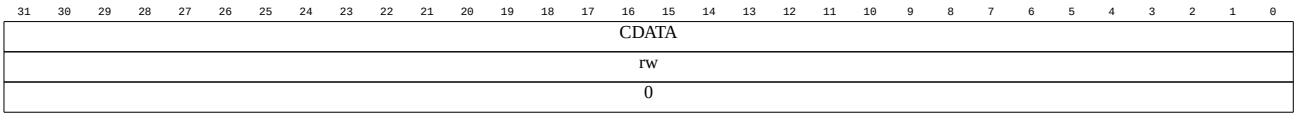
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CDATA	0xffffffff	0x0	Cache data word

Register DIAGD

Description

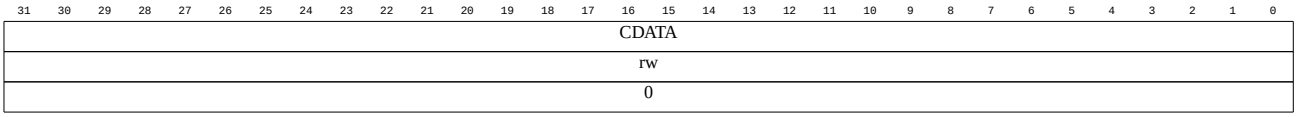
Diagnostic cache access data register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CDATA	0xffffffff	0x0	Cache data word

Register DIAGD

Description

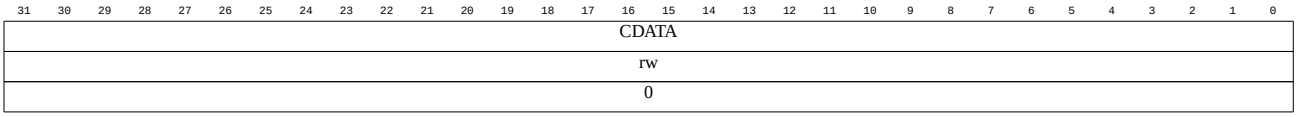
Diagnostic cache access data register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CDATA	0xffffffff	0x0	Cache data word

Register DIAGD

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

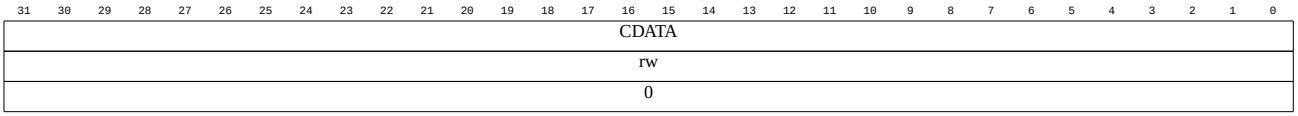
Diagnostic cache access data register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CDATA	0xffffffff	0x0	Cache data word

Register DIAGD

Description

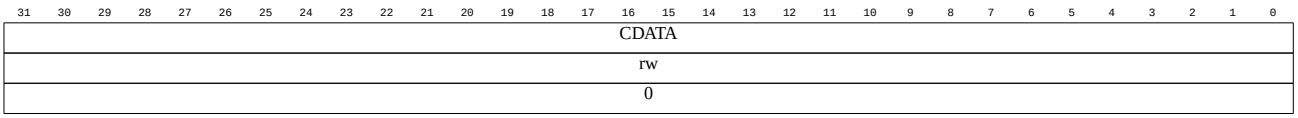
Diagnostic cache access data register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CDATA	0xffffffff	0x0	Cache data word

Register ASMPCTRL

Description

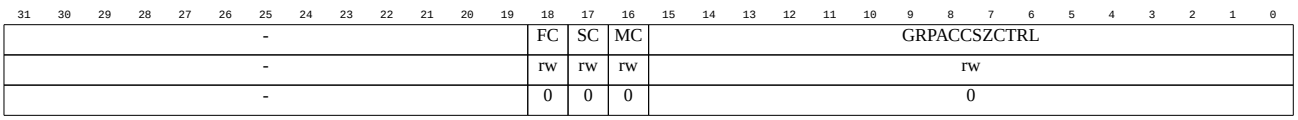
ASMP access control register

Reset value

0x00000000

Warm reset mask

0x0007ffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
FC	0x00040000	0x0	Flush register access control
SC	0x00020000	0x0	Status register access control
MC	0x00010000	0x0	Mask register access control
GRPACCSZCTRL	0x0000ffff	0x0	Group control register access control

Register ASMPCTRL

Description

ASMP access control register

Reset value

0x00000000

Warm reset mask

0x0007ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-													FC	SC	MC	GRPACCSZCTRL															
-													rw	rw	rw	rw															
-													0	0	0	0															

Field	Mask	Reset	Description
FC	0x00040000	0x0	Flush register access control
SC	0x00020000	0x0	Status register access control
MC	0x00010000	0x0	Mask register access control
GRPACCSZCTRL	0x0000ffff	0x0	Group control register access control

Register ASMPCTRL

Description

ASMP access control register

Reset value

0x00000000

Warm reset mask

0x0007ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-													FC	SC	MC	GRPACCSZCTRL															
-													rw	rw	rw	rw															
-													0	0	0	0															

Field	Mask	Reset	Description
FC	0x00040000	0x0	Flush register access control

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
SC	0x00020000	0x0	Status register access control
MC	0x00010000	0x0	Mask register access control
GRPACCSZCTRL	0x0000ffff	0x0	Group control register access control

Register ASMPCTRL

Description

ASMP access control register

Reset value

0x00000000

Warm reset mask

0x0007ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-													FC	SC	MC	GRPACCSZCTRL															
-													rw	rw	rw	rw															
-													0	0	0	0															

Field	Mask	Reset	Description
FC	0x00040000	0x0	Flush register access control
SC	0x00020000	0x0	Status register access control
MC	0x00010000	0x0	Mask register access control
GRPACCSZCTRL	0x0000ffff	0x0	Group control register access control

Commands

Name	Description
delete	Dispose instance of GRIOMMU

9.8.5. Limitations

- Read and write combining is not simulated
- Bus select is ignored, only one memory space is used for memory and processor.
- APV and TLB caches are not implemented at the moment.
- Flushes are instantaneous. This means that the FLI and FCI will only result in one actual interrupt being raised.

9.9. GRPCI2

The GRPCI2 model is available in the GrPci2 plugin.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

9.9.1. Loading the Plugin

```
import GrPci2
```

9.9.2. Configuration

9.9.3. @GRPCI2 Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GRPCI2
new	Create new instance of GRPCI2

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.9.4. GRPCI2 Reference

Properties

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
AHB2PCI	uint32_t	AHB to PCI mapping for PCI I/O
AHB2PCIColdResetValue	uint32_t	AHB to PCI mapping for PCI I/O
AHB2PCIForcedBits	uint32_t	AHB to PCI mapping for PCI I/O
AHB2PCIForcedFlippedBits	uint32_t	AHB to PCI mapping for PCI I/O
AHB2PCIReadMask	uint32_t	AHB to PCI mapping for PCI I/O
AHB2PCIResetMask	uint32_t	AHB to PCI mapping for PCI I/O
AHB2PCIResetValue	uint32_t	AHB to PCI mapping for PCI I/O
AHB2PCIWriteMask	uint32_t	AHB to PCI mapping for PCI I/O
AHBM2PCI	[uint32_t; 16]	AHB master to PCI memory address mapping register
BCIM	uint32_t	PCI master prefetch burst limit
BCIMColdResetValue	uint32_t	PCI master prefetch burst limit
BCIMForcedBits	uint32_t	PCI master prefetch burst limit
BCIMForcedFlippedBits	uint32_t	PCI master prefetch burst limit
BCIMReadMask	uint32_t	PCI master prefetch burst limit
BCIMResetMask	uint32_t	PCI master prefetch burst limit
BCIMResetValue	uint32_t	PCI master prefetch burst limit
BCIMWriteMask	uint32_t	PCI master prefetch burst limit
CTRL	uint32_t	Control register
CTRLColdResetValue	uint32_t	Control register
CTRLForcedBits	uint32_t	Control register
CTRLForcedFlippedBits	uint32_t	Control register
CTRLReadMask	uint32_t	Control register
CTRLResetMask	uint32_t	Control register
CTRLResetValue	uint32_t	Control register
CTRLWriteMask	uint32_t	Control register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
DMABASE	uint32_t	DMA descriptor base address
DMABASEColdResetValue	uint32_t	DMA descriptor base address
DMABASEForcedBits	uint32_t	DMA descriptor base address

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DMABASEForcedFlippedBits	uint32_t	DMA descriptor base address
DMABASEReadMask	uint32_t	DMA descriptor base address
DMABASEResetMask	uint32_t	DMA descriptor base address
DMABASEResetValue	uint32_t	DMA descriptor base address
DMABASEWriteMask	uint32_t	DMA descriptor base address
DMACHAN	uint32_t	DMA channel active
DMACHANColdResetValue	uint32_t	DMA channel active
DMACHANForcedBits	uint32_t	DMA channel active
DMACHANForcedFlippedBits	uint32_t	DMA channel active
DMACHANReadMask	uint32_t	DMA channel active
DMACHANResetMask	uint32_t	DMA channel active
DMACHANResetValue	uint32_t	DMA channel active
DMACHANWriteMask	uint32_t	DMA channel active
DMACTRL	uint32_t	GRPCI2 DMA control and status register
DMACTRLColdResetValue	uint32_t	GRPCI2 DMA control and status register
DMACTRLForcedBits	uint32_t	GRPCI2 DMA control and status register
DMACTRLForcedFlippedBits	uint32_t	GRPCI2 DMA control and status register
DMACTRLReadMask	uint32_t	GRPCI2 DMA control and status register
DMACTRLResetMask	uint32_t	GRPCI2 DMA control and status register
DMACTRLResetValue	uint32_t	GRPCI2 DMA control and status register
DMACTRLWriteMask	uint32_t	GRPCI2 DMA control and status register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ObjectID	uint64_t	Unique ObjectID.
PCI2AHB	[uint32_t; 6]	PCI BAR to AHB address mapping registers
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
STATCAP	uint32_t	Status and Capability register
STATCAPColdResetValue	uint32_t	Status and Capability register
STATCAPForcedBits	uint32_t	Status and Capability register
STATCAPForcedFlippedBits	uint32_t	Status and Capability register
STATCAPReadMask	uint32_t	Status and Capability register
STATCAPResetMask	uint32_t	Status and Capability register
STATCAPResetValue	uint32_t	Status and Capability register
STATCAPWriteMask	uint32_t	Status and Capability register
TimeSource	*void	Time source object
config.Irq	uint8_t	PCI irq number
config.littleEndian	uint8_t	Endianess of memory interface.
ioMem	temu_IfaceRef/ <unknown>	PCI i/o space object
irqCtrl	temu_IfaceRef/ <unknown>	Upward interrupt controller (i.e. on AMBA bus)
pciBus	*void	PCI bus object
pciDevices	temu_IfaceRefArray	PCI devices
pciMem	temu_IfaceRef/ <unknown>	PCI memory space object
processorMem	temu_IfaceRef/ <unknown>	Access to the processor’s memory space

Interfaces

Name	Type	Description
ApbIface	ApbIface	APB P&P interface
ConfigAccessIface	MemAccessIface	PCI config access interface.
IrqIface	IrqCtrlIface	PCI IRQ interface
MemAccessIface	MemAccessIface	Memory access interface (registers)
PCIBridgeIface	temu::PCIBridgeIface	PCI bridge interface.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
PCIMemAccessIface	MemAccessIface	PCI memory access interfaces
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.

Registers



Register support is currently experimental!

Register Bank Regs

Register CTRL

Description

Control register

Reset value

0x00000000

Warm reset mask

0xefff0fff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RE	MR	TR	-	SI	PE	ER	EI	BusNumber								-				DFA	IB	CB	DIF	DeviceINTMask				HostINTMask			
rw	rw	rw	-	rw	rw	rw	rw	rw								-				rw	rw	rw	rw	rw				rw			
0	0	0	-	0	0	0	0	0								-				0	0	0	0	0				0			

Field	Mask	Reset	Description
RE	0x80000000	0x0	PCI reset
MR	0x40000000	0x0	PCI master reset
TR	0x20000000	0x0	PCI target reset
SI	0x08000000	0x0	System error interrupt enable
PE	0x04000000	0x0	Parity error response enable
ER	0x02000000	0x0	Abort error response enable
EI	0x01000000	0x0	Error interrupt enable
BusNumber	0x00ff0000	0x0	Bus number for configuration cycles
DFA	0x00000800	0x0	Disable internal AHB-slave/DMA fair arbitration
IB	0x00000400	0x0	IO burst enable
CB	0x00000200	0x0	Configuration burst enable
DIF	0x00000100	0x0	Device interrupt force
DeviceINTMask	0x000000f0	0x0	Device interrupt mask
HostINTMask	0x0000000f	0x0	Host interrupt mask

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register STATCAP

Description

Status and Capability register

Reset value

0x00000000

Warm reset mask

0xffa00f1f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Host	MST	TAR	DMA	DI	HI	IRQmode		Trace	-	FH	CFGDO	CFGER	CoreInterruptStatus							HostInterruptStatus				-			FDEPTH			FNUM	
ro	ro	ro	ro	ro	ro	ro		ro	-	ro	rw	rw	rw							ro				-			ro			ro	
0	0	0	0	0	0	0		0	-	0	-	-	-							0				-			0			0	

Field	Mask	Reset	Description
Host	0x80000000	0x0	System host indicator
MST	0x40000000	0x0	Master implemented
TAR	0x20000000	0x0	Target implemented
DMA	0x10000000	0x0	DMA implemented
DI	0x08000000	0x0	Device drives PCI INTA
HI	0x04000000	0x0	Device samples PCI INTA..D
IRQmode	0x03000000	0x0	APB IRQ mode
Trace	0x00800000	0x0	PCI trace buffer implemented
FH	0x00200000	0x0	Fake device in system slot
CFGDO	0x00100000	-	PCI configuration access done
CFGER	0x00080000	-	Error during PCI configuration access
CoreInterruptStatus	0x0007f000	-	Core interrupt status
HostInterruptStatus	0x00000f00	0x0	Host interrupt status
FDEPTH	0x0000001c	0x0	FIFO depth
FNUM	0x00000003	0x0	Number of FIFOs

Register BCIM

Description

PCI master prefetch burst limit

Reset value

0x000000ff

Warm reset mask

0xffff00ff

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AHB_master_unmask																-								burst_length							
rw																-								rw							
0																-								255							

Field	Mask	Reset	Description
AHB_master_unmask	0xffff0000	0x0	Limit prefetch burst
burst_length	0x000000ff	0xff	Maximum number of beats per burst

Register AHB2PCI

Description

AHB to PCI mapping for PCI I/O

Reset value

0x00000000

Warm reset mask

0xffff0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AHB_to_PCI_IO																-															
rw																-															
0																-															

Field	Mask	Reset	Description
AHB_to_PCI_IO	0xffff0000	0x0	AHB to PCI IO base address

Register DMACTRL

Description

GRPCI2 DMA control and status register

Reset value

0x80000000

Warm reset mask

0x8000007f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SAFE							-									CHIRQ				MA	TA	PE	AE	DE	NumDMAChans			ACTIVE	DIS	IE	EN
rw							-									rw				rw	rw	rw	rw	rw	rw			ro	rw	rw	rw
1							-									-				-	-	-	-	-	0			0	0	0	0

Field	Mask	Reset	Description
SAFE	0x80000000	0x1	Arming of control field updates
CHIRQ	0x000ff000	-	Channel IRQ status
MA	0x00000800	-	Master abort

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Field	Mask	Reset	Description
TA	0x00000400	-	Target abort
PE	0x00000200	-	Parity error
AE	0x00000100	-	AHB data error
DE	0x00000080	-	Descriptor error
NumDMAChans	0x00000070	0x0	Number of DMA channels
ACTIVE	0x00000008	0x0	DMA is active
DIS	0x00000004	0x0	DMA disable
IE	0x00000002	0x0	Interrupt enable
EN	0x00000001	0x0	DMA enable

Register DMABASE

Description

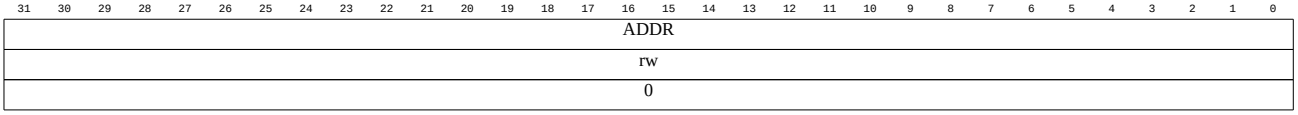
DMA descriptor base address

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	DMA descriptor base address

Register DMACHAN

Description

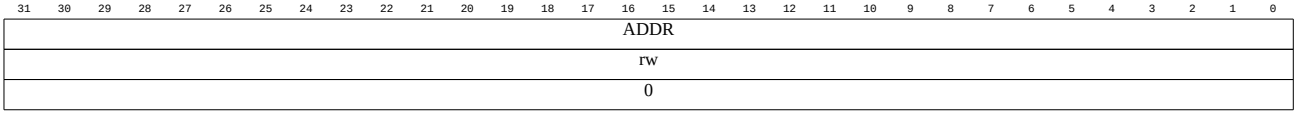
DMA channel active

Reset value

0x00000000

Warm reset mask

0xffffffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	DMA channel active descriptor base address

Register PCI2AHB

Description

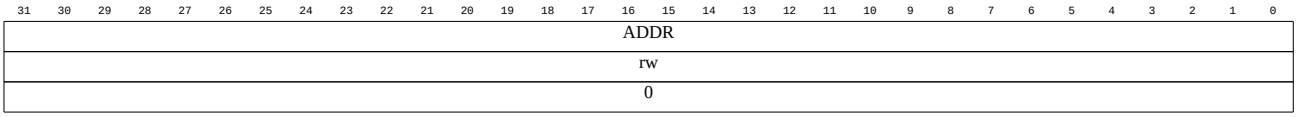
PCI BAR to AHB address mapping registers

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	PCI BAR to AHB address mapping

Register PCI2AHB

Description

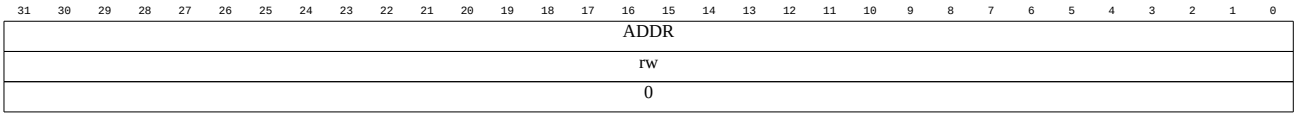
PCI BAR to AHB address mapping registers

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	PCI BAR to AHB address mapping

Register PCI2AHB

Description

PCI BAR to AHB address mapping registers

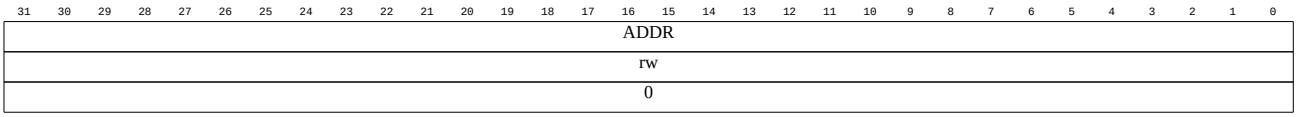
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	PCI BAR to AHB address mapping

Register PCI2AHB

Description

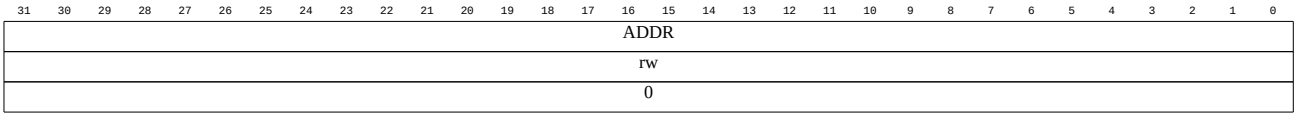
PCI BAR to AHB address mapping registers

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	PCI BAR to AHB address mapping

Register PCI2AHB

Description

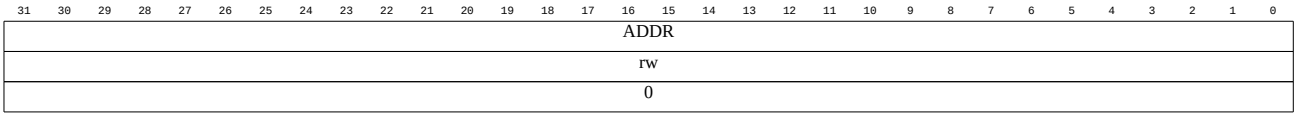
PCI BAR to AHB address mapping registers

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	PCI BAR to AHB address mapping

Register PCI2AHB

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

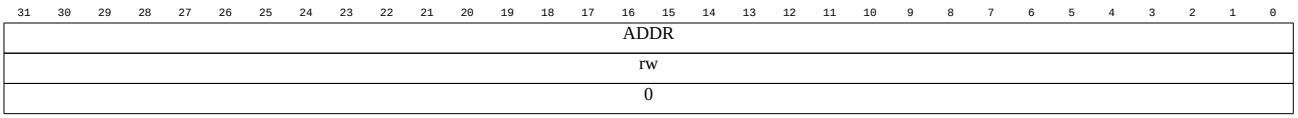
PCI BAR to AHB address mapping registers

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	PCI BAR to AHB address mapping

Register AHBM2PCI

Description

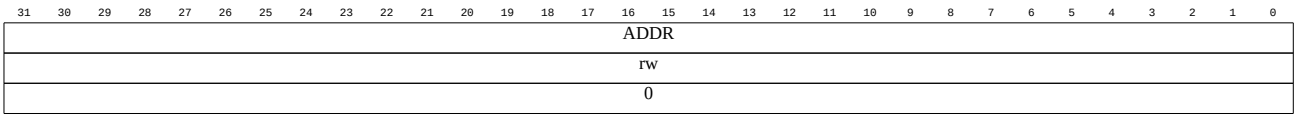
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

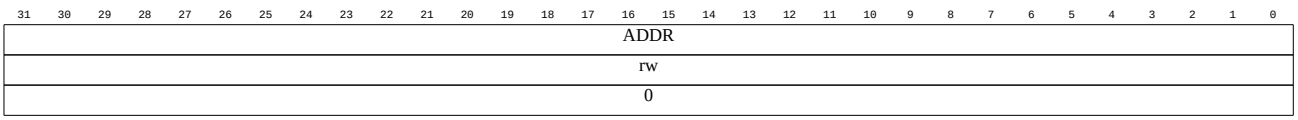
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

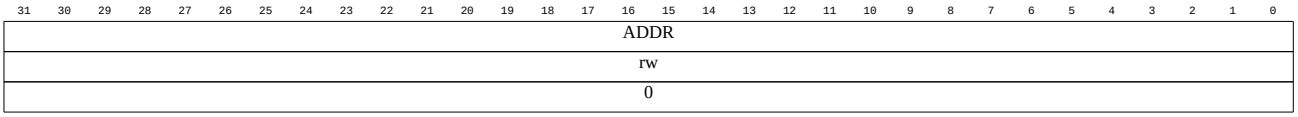
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

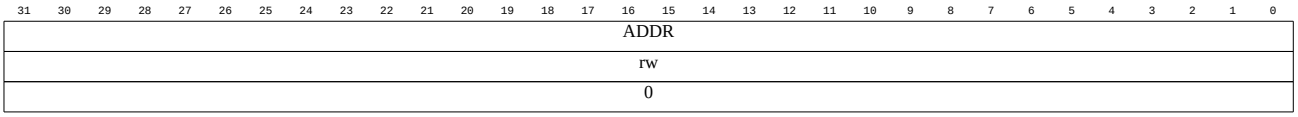
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

AHB master to PCI memory address mapping register

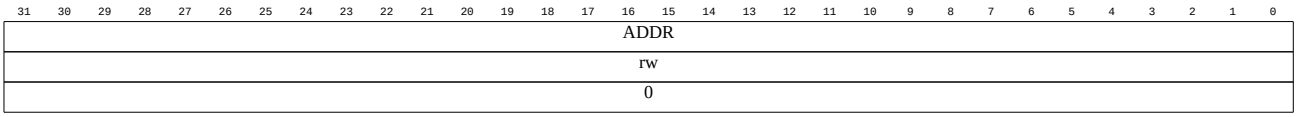
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

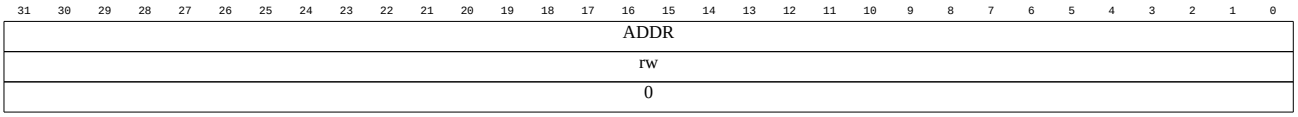
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

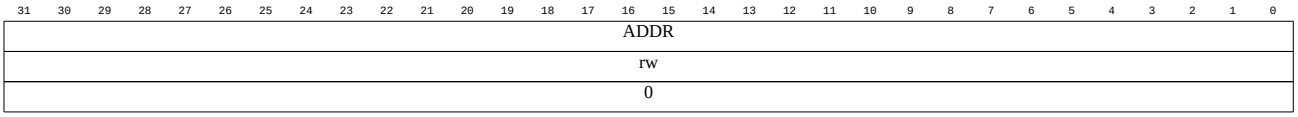
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

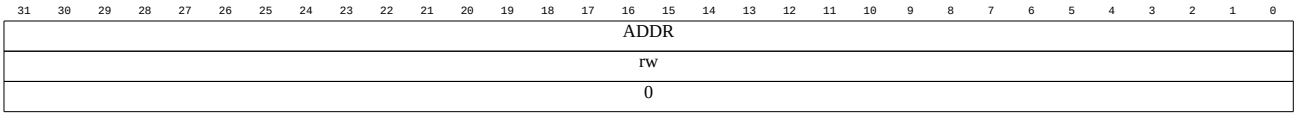
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

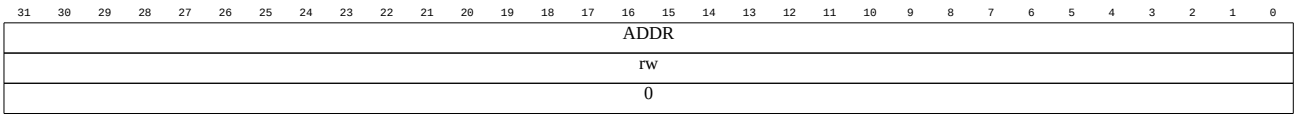
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

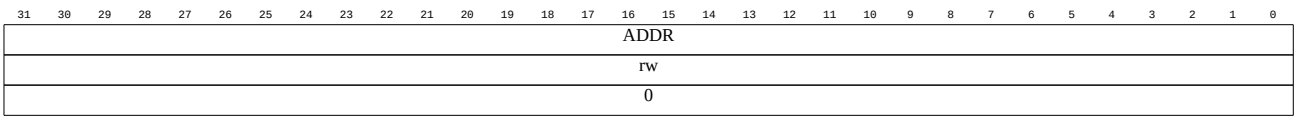
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

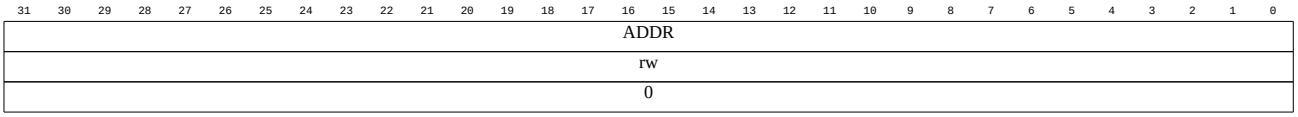
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

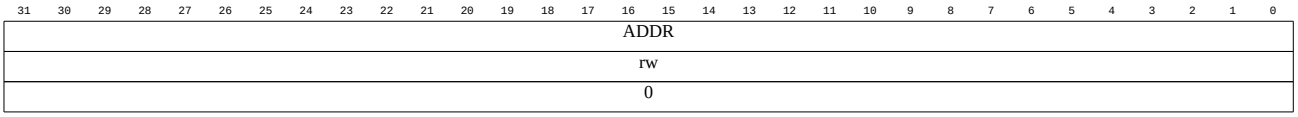
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

AHB master to PCI memory address mapping register

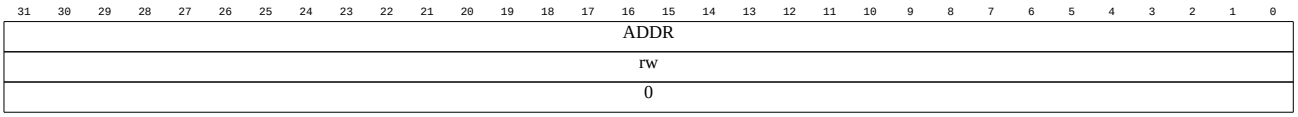
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

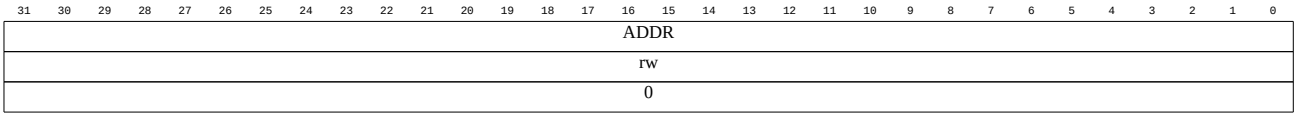
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

Description

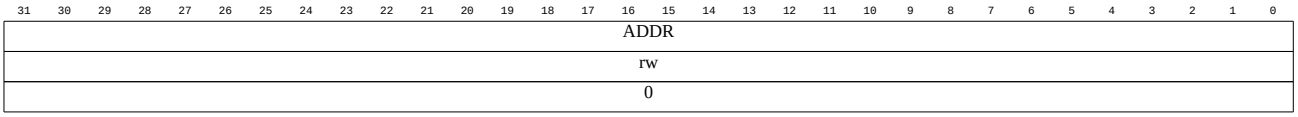
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Register AHBM2PCI

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

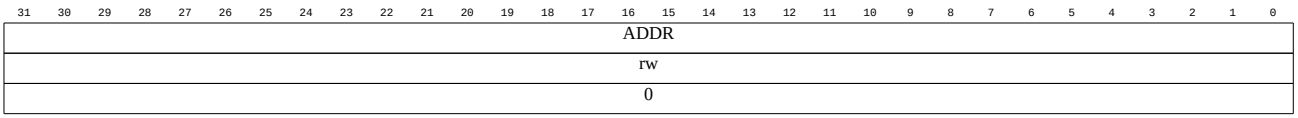
AHB master to PCI memory address mapping register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
ADDR	0xffffffff	0x0	AHB master to PCI memory address mapping

Commands

Name	Description
delete	Dispose instance of GRPCI2

9.9.5. Limitations

- The device currently only supports one AHB master. Since most systems only have one (e.g. an AHB2AHB bridge), this limitation should not be a major issue.

9.10. GRSPW1

The GRSPW1 is part of the GRLIB IP library. It is available in libTEMUGrspw1.so.

9.10.1. Loading the Plugin

```
import Grspw1
```

9.10.2. Configuration

To work correctly, the device must be connected to an interrupt controller, a memory and another SpaceWire device.

There are several configuration parameters in the GrSpw1 device. They are summarized in the following table:

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Description
config.infiniteSpeed	With this set, messages are sent immediately instead of being scheduled for the future based on the message length. This is the default option.
config.transmitter.frequency	Specify the SpaceWire transmitter frequency in Hz. Affects transfer speed when infinite speed is disabled.
config.transmitter.dataRate	SpaceWire port datarate: 1=single, 2=double, etc. Affects transfer speed when infinite speed is disabled.
config.interrupt	Influences the interrupt that is raised with the IRQ controller (setting this property also updates the APB PnP info).
config.realCrcCheck	Set to use real crc check instead of packet crc flags. Real crc costs in terms of performance.

9.10.3. @Grspw1 Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @Grspw1

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Description
new	Create new instance of Grspw1

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.10.4. Grspw1 Reference

Properties

Name	Type	Description
CLKDIVColdResetValue	uint32_t	Clock divisor register
CLKDIVForcedBits	uint32_t	Clock divisor register
CLKDIVForcedFlippedBits	uint32_t	Clock divisor register
CLKDIVReadMask	uint32_t	Clock divisor register
CLKDIVResetMask	uint32_t	Clock divisor register
CLKDIVResetValue	uint32_t	Clock divisor register
CLKDIVWriteMask	uint32_t	Clock divisor register
CTRLColdResetValue	uint32_t	Control register
CTRLForcedBits	uint32_t	Control register
CTRLForcedFlippedBits	uint32_t	Control register
CTRLReadMask	uint32_t	Control register
CTRLResetMask	uint32_t	Control register
CTRLResetValue	uint32_t	Control register
CTRLWriteMask	uint32_t	Control register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
DKEYColdResetValue	uint32_t	Destination key register
DKEYForcedBits	uint32_t	Destination key register
DKEYForcedFlippedBits	uint32_t	Destination key register
DKEYReadMask	uint32_t	Destination key register
DKEYResetMask	uint32_t	Destination key register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DKEYResetValue	uint32_t	Destination key register
DKEYWriteMask	uint32_t	Destination key register
DMACTRLColdResetValue	uint32_t	DMA channel 1 control/status register
DMACTRLForcedBits	uint32_t	DMA channel 1 control/status register
DMACTRLForcedFlippedBits	uint32_t	DMA channel 1 control/status register
DMACTRLReadMask	uint32_t	DMA channel 1 control/status register
DMACTRLResetMask	uint32_t	DMA channel 1 control/status register
DMACTRLResetValue	uint32_t	DMA channel 1 control/status register
DMACTRLWriteMask	uint32_t	DMA channel 1 control/status register
DMAMAXLENColdResetValue	uint32_t	DMA channel 1 RX maximum length register
DMAMAXLENForcedBits	uint32_t	DMA channel 1 RX maximum length register
DMAMAXLENForcedFlippedBits	uint32_t	DMA channel 1 RX maximum length register
DMAMAXLENReadMask	uint32_t	DMA channel 1 RX maximum length register
DMAMAXLENResetMask	uint32_t	DMA channel 1 RX maximum length register
DMAMAXLENResetValue	uint32_t	DMA channel 1 RX maximum length register
DMAMAXLENWriteMask	uint32_t	DMA channel 1 RX maximum length register
DMARXDESCColdResetValue	uint32_t	DMA channel 1 receive descriptor table address register
DMARXDESCForcedBits	uint32_t	DMA channel 1 receive descriptor table address register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DMARXDESCForcedFlippedBits	uint32_t	DMA channel 1 receive descriptor table address register
DMARXDESCReadMask	uint32_t	DMA channel 1 receive descriptor table address register
DMARXDESCResetMask	uint32_t	DMA channel 1 receive descriptor table address register
DMARXDESCResetValue	uint32_t	DMA channel 1 receive descriptor table address register
DMARXDESCWriteMask	uint32_t	DMA channel 1 receive descriptor table address register
DMATXDESCColdResetValue	uint32_t	DMA channel 1 transmit descriptor table address register
DMATXDESCForcedBits	uint32_t	DMA channel 1 transmit descriptor table address register
DMATXDESCForcedFlippedBits	uint32_t	DMA channel 1 transmit descriptor table address register
DMATXDESCReadMask	uint32_t	DMA channel 1 transmit descriptor table address register
DMATXDESCResetMask	uint32_t	DMA channel 1 transmit descriptor table address register
DMATXDESCResetValue	uint32_t	DMA channel 1 transmit descriptor table address register
DMATXDESCWriteMask	uint32_t	DMA channel 1 transmit descriptor table address register
LocalName	*char	Local name (in component, if applicable)

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
NODEADDRColdResetValue	uint32_t	Node address register
NODEADDRForcedBits	uint32_t	Node address register
NODEADDRForcedFlippedBits	uint32_t	Node address register
NODEADDRReadMask	uint32_t	Node address register
NODEADDRResetMask	uint32_t	Node address register
NODEADDRResetValue	uint32_t	Node address register
NODEADDRWriteMask	uint32_t	Node address register
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
STSColdResetValue	uint32_t	Status / Interrupt-source register
STSForcedBits	uint32_t	Status / Interrupt-source register
STSForcedFlippedBits	uint32_t	Status / Interrupt-source register
STSReadMask	uint32_t	Status / Interrupt-source register
STSResetMask	uint32_t	Status / Interrupt-source register
STSResetValue	uint32_t	Status / Interrupt-source register
STSWriteMask	uint32_t	Status / Interrupt-source register
TDRColdResetValue	uint32_t	Timer and disconnect register
TDRForcedBits	uint32_t	Timer and disconnect register
TDRForcedFlippedBits	uint32_t	Timer and disconnect register
TDRReadMask	uint32_t	Timer and disconnect register
TDRResetMask	uint32_t	Timer and disconnect register
TDRResetValue	uint32_t	Timer and disconnect register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
TDRWriteMask	uint32_t	Timer and disconnect register
TIMEColdResetValue	uint32_t	Time register
TIMEForcedBits	uint32_t	Time register
TIMEForcedFlippedBits	uint32_t	Time register
TIMEReadMask	uint32_t	Time register
TIMEResetMask	uint32_t	Time register
TIMEResetValue	uint32_t	Time register
TIMEWriteMask	uint32_t	Time register
TimeSource	*void	Time source object
config.infiniteSpeed	uint8_t	Set to use infinite speed for transfers.
config.interrupt	uint8_t	The interrupt index
config.realCrcCheck	uint8_t	Set to use real crc check instead of packet crc flags
config.transmitter.dataRate	uint8_t	SpaceWire port datarate: 1=single, 2=double,...
config.transmitter.frequency	uint32_t	SpaceWire transmitter frequency in Hz
internal.linkState	int32_t	Link state
internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
internal.tcBusy	uint8_t	Set while a time code transmission is pending
internal.txBusy	uint8_t	Set while a transmission is claimed by this device
internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
internal.uplinkNsPerByte	uint32_t	Transmitter speed
irqCtrl	temu_IfaceRef/ <unknown>	Irq controller
memAccess	temu_IfaceRef/ <unknown>	Memory used for DMA accesses
pnp.bar	uint32_t	Pnp BAR
pnp.config	uint32_t	Pnp configuration
regs.clockDiv	uint32_t	Clock divisor register
regs.control	uint32_t	Control register
regs.destKey	uint32_t	Destination key register
regs.dmaControl	uint32_t	DMA channel 1 control/status register
regs.dmaRxDescTableAddr	uint32_t	DMA channel 1 receive descriptor table address register
regs.dmaRxMaxLen	uint32_t	DMA channel 1 RX maximum length register
regs.dmaTxDescTableAddr	uint32_t	DMA channel 1 transmit descriptor table address register
regs.nodeAddress	uint32_t	Node address register
regs.statusIrqSrc	uint32_t	Status / Interrupt-source register
regs.time	uint32_t	Time register
regs.timeDisconnect	uint32_t	Timer and disconnect register
spwUplink	[temu_IfaceRef; 2]/ <unknown>	SpaceWire devices connected to the port

Interfaces

Name	Type	Description
ApbIface	ApbIface	Apb interface
DeviceIface	DeviceIface	Device interface
MemAccessIface	MemAccessIface	Memory Access Interface
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	
SpwPortIface	SpwPortIface	SpaceWire ports interfaces

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Registers



Register support is currently experimental!

Register Bank Regs

Register CTRL

Description

Control register

Reset value

0xe0000000

Warm reset mask

0xe4330f7f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RA	RX	RC	-		PO	-				PS	NP	-		RD	RE	-				TR	TT	LI	TQ	-	RS	PM	TI	IE	AS	LS	LD
ro	ro	ro	-		ro	-				rw	rw	-		rw	rw	-				rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw
1	1	1	-		0	-				0	0	-		0	0	-				0	0	0	0	-	0	0	0	0	0	0	0

Field	Mask	Reset	Description
RA	0x80000000	0x1	RMAP available
RX	0x40000000	0x1	RX unaligned access
RC	0x20000000	0x1	RMAP CRC available
PO	0x04000000	0x0	Number of ports minus one
PS	0x00200000	0x0	Port select
NP	0x00100000	0x0	No port force
RD	0x00020000	0x0	RMAP buffer disable
RE	0x00010000	0x0	RMAP enable
TR	0x00000800	0x0	Time RX enable
TT	0x00000400	0x0	Time TX enable
LI	0x00000200	0x0	Link error IRQ
TQ	0x00000100	0x0	Tick-out IRQ
RS	0x00000040	0x0	Reset
PM	0x00000020	0x0	Promiscuous mode
TI	0x00000010	0x0	Tick in
IE	0x00000008	0x0	Interrupt enable
AS	0x00000004	0x0	Autostart
LS	0x00000002	0x0	Link start

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Field	Mask	Reset	Description
LD	0x00000001	0x0	Link disable

Register STS

Description

Status / Interrupt-source register

Reset value

0x00000000

Warm reset mask

0x00e00200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-								LS			-											AP	EE	IA	WE	-	PE	DE	ER	CE	TO
-								ro			-											rw	rw	rw	rw	-	rw	rw	rw	rw	rw
-								0			-											0	-	-	-	-	-	-	-	-	-

Field	Mask	Reset	Description
LS	0x00e00000	0x0	Link state
AP	0x00000200	0x0	Active port
EE	0x00000100	-	Early EOP/EEP
IA	0x00000080	-	Invalid address
WE	0x00000040	-	Write synchronization error
PE	0x00000010	-	Parity error
DE	0x00000008	-	Disconnect error
ER	0x00000004	-	Escape error
CE	0x00000002	-	Credit error
TO	0x00000001	-	Tick out

Register NODEADDR

Description

Node address register

Reset value

0x000000fe

Warm reset mask

0x000000ff

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								NODEADDR							
-																								rw							
-																								254							

Field	Mask	Reset	Description
NODEADDR	0x000000ff	0xfe	Node address

Register CLKDIV

Description

Clock divisor register

Reset value

0x00000000

Warm reset mask

0x0000ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																CLKDIVSTART								CLKDIVRUN							
-																rw								rw							
-																0								0							

Field	Mask	Reset	Description
CLKDIVSTART	0x0000ff00	0x0	Clock divisor startup
CLKDIVRUN	0x000000ff	0x0	Clock divisor run

Register DKEY

Description

Destination key register

Reset value

0x00000000

Warm reset mask

0x000000ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								DESTKEY							
-																								rw							
-																								0							

Field	Mask	Reset	Description
DESTKEY	0x000000ff	0x0	Destination key

Register TIME

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Time register

Reset value

0x00000000

Warm reset mask

0x000000ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								TCTRL		TIMECNT					
-																								rw		rw					
-																								0		0					

Field	Mask	Reset	Description
TCTRL	0x000000c0	0x0	Time control flags
TIMECNT	0x0000003f	0x0	Time counter

Register TDR

Description

Timer and disconnect register

Reset value

0x00000000

Warm reset mask

0x003fffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-										DISCONNECT										TIMER64											
-										rw										rw											
-										0										0											

Field	Mask	Reset	Description
DISCONNECT	0x003ff000	0x0	Disconnect period
TIMER64	0x00000fff	0x0	6.4 us timer

Register DMACTRL

Description

DMA channel 1 control/status register

Reset value

0x00000000

Warm reset mask

0x00011e1f

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-															LE	-			NS	RD	RX	AT	RA	TA	PR	PS	AI	RI	TI	RE	TE	
-															rw	-			rw	rw	ro	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-															0	-			0	0	0	0	-	-	-	-	0	0	0	0	0	

Field	Mask	Reset	Description
LE	0x00010000	0x0	Link error disable
NS	0x00001000	0x0	No spill
RD	0x00000800	0x0	RX descriptors available
RX	0x00000400	0x0	RX active
AT	0x00000200	0x0	Abort TX
RA	0x00000100	-	RX AHB error
TA	0x00000080	-	TX AHB error
PR	0x00000040	-	Packet received
PS	0x00000020	-	Packet sent
AI	0x00000010	0x0	AHB error interrupt
RI	0x00000008	0x0	Receive interrupt
TI	0x00000004	0x0	Transmit interrupt
RE	0x00000002	0x0	Receiver enable
TE	0x00000001	0x0	Transmitter enable

Register DMAMAXLEN

Description

DMA channel 1 RX maximum length register

Reset value

0x00000000

Warm reset mask

0x01fffffc

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-							RXMAXLEN																							-	
-							rw																							-	
-							0																							-	

Field	Mask	Reset	Description
RXMAXLEN	0x01fffffc	0x0	Receiver packet maximum length in bytes

Register DMATXDESC

Description

DMA channel 1 transmit descriptor table address register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0xfffffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESCBASEADDR																						DESCSEL						-			
rw																						rw						-			
0																						0						-			

Field	Mask	Reset	Description
DESCBASEADDR	0xfffffc00	0x0	Descriptor table base address
DESCSEL	0x000003f0	0x0	Descriptor selector

Register DMARXDESC

Description

DMA channel 1 receive descriptor table address register

Reset value

0x00000000

Warm reset mask

0xfffffff8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESCBASEADDR																						DESCSEL							-		
rw																						rw							-		
0																						0							-		

Field	Mask	Reset	Description
DESCBASEADDR	0xfffffc00	0x0	Descriptor table base address
DESCSEL	0x000003f8	0x0	Descriptor selector

Commands

Name	Description
delete	Dispose instance of Grspw1

9.10.5. Limitations

The following deviations from real hardware are known to exist with this model:

- No spill is currently not implemented.
- Althougth the device already provides two spacewire ports, dual port is not yet implemented. This correspond to a device where the port VHDL parameter is set to 1. Therefore, in the control

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register, *PO = 0* and *PS / NP* are not available. Let us know if you need this feature implemented.

- The link interface currently effectively uses only *ErrorReset*, *Ready*, *Connecting* and Run states. These are the only values that will be visible on the status register.
- RMAPEN signals not available.

9.10.6. Examples

This example show how to create two Grspw1 devices and connect them:

Listing 24. Creating and Connecting GRSPW1 Devices

```
import BusModels
import TEMUGrspw1
Grspw1.new name=grspw0
Grspw1.new name=grspw1
spw-connect port1=grspw0:SpwPortIface[0] port2=grspw1:SpwPortIface[0]
```

9.11. GRSPW2

The Grspw2 model is part of the GRLIB IP library feature. It is available in the Grspw2 plugin.

9.11.1. Loading the Plugin

```
import Grspw2
```

9.11.2. Configuration

To work correctly, the device must be connected to an interrupt controller, a memory and another SpaceWire device.

There are several configuration parameters in the GrSpw2 device. These are summarized in the following table:

Name	Description
config.infiniteSpeed	With this set, messages are sent immediately instead of being scheduled for the future based on the message length. This is the default option.
config.transmitter.frequency	Specify the SpaceWire transmitter frequency in Hz. Affects transfer speed when infinite speed is disabled.
config.transmitter.dataRate	SpaceWire port datarate: 1=single, 2=double, etc. Affects transfer speed when infinite speed is disabled.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Description
config.dma.rxdescnum	Specifies the amount of rx description (0=128, 1=256, 2=512, 3=1024). This affect the regs.dmaRxDescTableAddr
config.dma.txdescnum	Specifies the amount of tx descriptors (0=64, 1=128, 2=256, 3=512). This affect the regs.dmaTxDescTableAddr
config.interrupt	Influences the interrupt that is raised with the IRQ controller (setting this property also updates the APB PnP info).
config.realCrcCheck	Set to use real crc check instead of packet crc flags. Real crc costs in terms of performance.

9.11.3. @Grspw2 Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @Grspw2
new	Create new instance of Grspw2

Command new Arguments

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Required	Description
name	string	yes	Name of object to create

9.11.4. Grspw2 Reference

Properties

Name	Type	Description
CLKDIVColdResetValue	uint32_t	Clock divisor register
CLKDIVForcedBits	uint32_t	Clock divisor register
CLKDIVForcedFlippedBits	uint32_t	Clock divisor register
CLKDIVReadMask	uint32_t	Clock divisor register
CLKDIVResetMask	uint32_t	Clock divisor register
CLKDIVResetValue	uint32_t	Clock divisor register
CLKDIVWriteMask	uint32_t	Clock divisor register
CTRLColdResetValue	uint32_t	Control register
CTRLForcedBits	uint32_t	Control register
CTRLForcedFlippedBits	uint32_t	Control register
CTRLReadMask	uint32_t	Control register
CTRLResetMask	uint32_t	Control register
CTRLResetValue	uint32_t	Control register
CTRLWriteMask	uint32_t	Control register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
DEFADDRColdResetValue	uint32_t	Node address register
DEFADDRForcedBits	uint32_t	Node address register
DEFADDRForcedFlippedBits	uint32_t	Node address register
DEFADDRReadMask	uint32_t	Node address register
DEFADDRResetMask	uint32_t	Node address register
DEFADDRResetValue	uint32_t	Node address register
DEFADDRWriteMask	uint32_t	Node address register
DKEYColdResetValue	uint32_t	Destination key register
DKEYForcedBits	uint32_t	Destination key register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DKEYForcedFlippedBits	uint32_t	Destination key register
DKEYReadMask	uint32_t	Destination key register
DKEYResetMask	uint32_t	Destination key register
DKEYResetValue	uint32_t	Destination key register
DKEYWriteMask	uint32_t	Destination key register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
STSColdResetValue	uint32_t	Status / interrupt-source register
STSForcedBits	uint32_t	Status / interrupt-source register
STSForcedFlippedBits	uint32_t	Status / interrupt-source register
STSReadMask	uint32_t	Status / interrupt-source register
STSResetMask	uint32_t	Status / interrupt-source register
STSResetValue	uint32_t	Status / interrupt-source register
STSWriteMask	uint32_t	Status / interrupt-source register
TCColdResetValue	uint32_t	Time register
TCForcedBits	uint32_t	Time register
TCForcedFlippedBits	uint32_t	Time register
TCReadMask	uint32_t	Time register
TCResetMask	uint32_t	Time register
TCResetValue	uint32_t	Time register
TCWriteMask	uint32_t	Time register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
TimeSource	*void	Time source object
config.dma.rxdescnum	uint8_t	Number of rx descriptors
config.dma.txdescnum	uint8_t	Number of tx descriptors
config.infiniteSpeed	uint8_t	Set to use infinite speed for transfers.
config.interrupt	uint8_t	The interrupt index
config.realCrcCheck	uint8_t	Set to use real crc check instead of packet crc flags
config.transmitter.dataRate	uint8_t	SpaceWire port datarate: 1=single, 2=double,...
config.transmitter.frequency	uint32_t	SpaceWire transmitter frequency in Hz
internal.linkState	int32_t	Link state
internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
internal.tcBusy	uint8_t	Set while a time code transmission is pending
internal.txBusy	uint8_t	Set while a transmission is claimed by this device
internal.txCurrChan	uint8_t	Channel scheduled for transmission
internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
internal.uplinkNsPerByte	uint32_t	Transmitter speed
irqCtrl	temu_IfaceRef/ <unknown>	Irq controller
memAccess	temu_IfaceRef/ <unknown>	Memory used for DMA accesses
pnp.bar	uint32_t	Pnp BAR
pnp.config	uint32_t	Pnp configuration

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
regs.clockDiv	uint32_t	Clock divisor register
regs.control	uint32_t	Control register
regs.destKey	uint32_t	Destination key register
regs.dmaAddr	[uint32_t; 4]	DMA address register
regs.dmaControl	[uint32_t; 4]	DMA control/status register
regs.dmaRxDescTableAddr	[uint32_t; 4]	DMA receive descriptor table address register
regs.dmaRxMaxLen	[uint32_t; 4]	DMA RX maximum length register
regs.dmaTxDescTableAddr	[uint32_t; 4]	DMA transmit descriptor table address register
regs.nodeAddress	uint32_t	Node address register
regs.statusIrqSrc	uint32_t	Status / interrupt-source register
regs.time	uint32_t	Time register
spwUplink	[temu_IfaceRef; 2]/ <unknown>	SpaceWire devices connected to the port

Interfaces

Name	Type	Description
ApbIface	ApbIface	Apb interface
DeviceIface	DeviceIface	Device interface
MemAccessIface	MemAccessIface	Memory Access Interface
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	
SpwPortIface	SpwPortIface	SpaceWire ports interfaces

Registers



Register support is currently experimental!

Register Bank Regs

Register CTRL

Description

Control register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0xc8000000

Warm reset mask

0xfc033f7f

31	30	29	28 27	26	25 24 23 22 21 20 19 18	17	16	15 14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RA	RX	RC	NCH	PO	-	RD	RE	-	TL	TF	TR	TT	LI	TQ	-	RS	PM	TI	IE	AS	LS	LD
ro	ro	ro	ro	ro	-	rw	rw	-	rw	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw
1	1	0	1	0	-	0	0	-	0	0	0	0	0	0	-	0	0	0	0	0	0	0

Field	Mask	Reset	Description
RA	0x80000000	0x1	RMAP available
RX	0x40000000	0x1	RX unaligned access
RC	0x20000000	0x0	RMAP CRC available
NCH	0x18000000	0x1	Number of DMA channels minus one
PO	0x04000000	0x0	Number of ports minus one
RD	0x00020000	0x0	RMAP buffer disable
RE	0x00010000	0x0	RMAP enable
TL	0x00002000	0x0	Transmitter enable lock control
TF	0x00001000	0x0	Time-code control flag filter
TR	0x00000800	0x0	Time RX enable
TT	0x00000400	0x0	Time TX enable
LI	0x00000200	0x0	Link error IRQ
TQ	0x00000100	0x0	Tick-out IRQ
RS	0x00000040	0x0	Reset
PM	0x00000020	0x0	Promiscuous mode
TI	0x00000010	0x0	Tick in
IE	0x00000008	0x0	Interrupt enable
AS	0x00000004	0x0	Autostart
LS	0x00000002	0x0	Link start
LD	0x00000001	0x0	Link disable

Register STS

Description

Status / interrupt-source register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0x0f000000

31 30 29 28	27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9	8	7	6 5	4	3	2	1	0
-	NRXD	NTXD	-	EE	IA	-	PE	DE	ER	CE	TO
-	ro	ro	-	rw	rw	-	rw	rw	rw	rw	rw
-	0	0	-	-	-	-	-	-	-	-	-

Field	Mask	Reset	Description
NRXD	0x0c000000	0x0	Number of receive descriptors
NTXD	0x03000000	0x0	Number of transmit descriptors
EE	0x00000100	-	Early EOP/EEP
IA	0x00000080	-	Invalid address
PE	0x00000010	-	Parity error
DE	0x00000008	-	Disconnect error
ER	0x00000004	-	Escape error
CE	0x00000002	-	Credit error
TO	0x00000001	-	Tick out

Register DEFADDR

Description

Node address register

Reset value

0x000000fe

Warm reset mask

0x0000ffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
-	DEFMASK	DEFADDR
-	rw	rw
-	0	254

Field	Mask	Reset	Description
DEFMASK	0x0000ff00	0x0	Default mask
DEFADDR	0x000000ff	0xfe	Default address

Register CLKDIV

Description

Clock divisor register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00002727

Warm reset mask

0x0000ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																CLKDIVSTART								CLKDIVRUN							
-																rw								rw							
-																39								39							

Field	Mask	Reset	Description
CLKDIVSTART	0x0000ff00	0x27	Clock divisor startup
CLKDIVRUN	0x000000ff	0x27	Clock divisor run

Register DKEY

Description

Destination key register

Reset value

0x00000000

Warm reset mask

0x000000ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								DESTKEY							
-																								rw							
-																								0							

Field	Mask	Reset	Description
DESTKEY	0x000000ff	0x0	Destination key

Register TC

Description

Time register

Reset value

0x00000000

Warm reset mask

0x000000ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																										TCTRL				TIMECNT			
-																										rw				rw			
-																										0				0			

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
TCTRL	0x000000c0	0x0	Time control flags
TIMECNT	0x0000003f	0x0	Time counter

Register DMACTRL

Description

DMA control/status register

Reset value

0x00000000

Warm reset mask

0x0001fe1f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-								EP	TR	-		RP	TP	TL	LE	SP	SA	EN	NS	RD	RX	AT	RA	TA	PR	PS	AI	RI	TI	RE	TE
-								rw	rw	-		rw	rw	rw	rw	rw	rw	rw	rw	rw	ro	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-								-	-	-		-	-	-	0	0	0	0	0	0	0	0	-	-	-	-	0	0	0	0	0

Field	Mask	Reset	Description
EP	0x00800000	-	EEP termination
TR	0x00400000	-	Truncated
RP	0x00080000	-	Receive packet IRQ
TP	0x00040000	-	Transmit packet IRQ
TL	0x00020000	-	Transmitter enable lock
LE	0x00010000	0x0	Link error disable
SP	0x00008000	0x0	Strip PID
SA	0x00004000	0x0	Strip address
EN	0x00002000	0x0	Enable address
NS	0x00001000	0x0	No spill
RD	0x00000800	0x0	RX descriptors available
RX	0x00000400	0x0	RX active
AT	0x00000200	0x0	Abort TX
RA	0x00000100	-	RX AHB error
TA	0x00000080	-	TX AHB error
PR	0x00000040	-	Packet received
PS	0x00000020	-	Packet sent
AI	0x00000010	0x0	AHB error interrupt

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
RI	0x00000008	0x0	Receive interrupt
TI	0x00000004	0x0	Transmit interrupt
RE	0x00000002	0x0	Receiver enable
TE	0x00000001	0x0	Transmitter enable

Register DMACTRL

Description

DMA control/status register

Reset value

0x00000000

Warm reset mask

0x0001fe1f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-								EP	TR	-		RP	TP	TL	LE	SP	SA	EN	NS	RD	RX	AT	RA	TA	PR	PS	AI	RI	TI	RE	TE
-								rw	rw	-		rw	rw	rw	rw	rw	rw	rw	rw	rw	ro	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-								-	-	-		-	-	-	0	0	0	0	0	0	0	0	-	-	-	-	0	0	0	0	0

Field	Mask	Reset	Description
EP	0x00800000	-	EEP termination
TR	0x00400000	-	Truncated
RP	0x00080000	-	Receive packet IRQ
TP	0x00040000	-	Transmit packet IRQ
TL	0x00020000	-	Transmitter enable lock
LE	0x00010000	0x0	Link error disable
SP	0x00008000	0x0	Strip PID
SA	0x00004000	0x0	Strip address
EN	0x00002000	0x0	Enable address
NS	0x00001000	0x0	No spill
RD	0x00000800	0x0	RX descriptors available
RX	0x00000400	0x0	RX active
AT	0x00000200	0x0	Abort TX
RA	0x00000100	-	RX AHB error
TA	0x00000080	-	TX AHB error
PR	0x00000040	-	Packet received

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
PS	0x00000020	-	Packet sent
AI	0x00000010	0x0	AHB error interrupt
RI	0x00000008	0x0	Receive interrupt
TI	0x00000004	0x0	Transmit interrupt
RE	0x00000002	0x0	Receiver enable
TE	0x00000001	0x0	Transmitter enable

Register DMACTRL

Description

DMA control/status register

Reset value

0x00000000

Warm reset mask

0x0001fe1f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-								EP	TR	-		RP	TP	TL	LE	SP	SA	EN	NS	RD	RX	AT	RA	TA	PR	PS	AI	RI	TI	RE	TE
-								rw	rw	-		rw	rw	rw	rw	rw	rw	rw	rw	rw	ro	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-								-	-	-		-	-	-	0	0	0	0	0	0	0	0	-	-	-	-	0	0	0	0	0

Field	Mask	Reset	Description
EP	0x00800000	-	EEP termination
TR	0x00400000	-	Truncated
RP	0x00080000	-	Receive packet IRQ
TP	0x00040000	-	Transmit packet IRQ
TL	0x00020000	-	Transmitter enable lock
LE	0x00010000	0x0	Link error disable
SP	0x00008000	0x0	Strip PID
SA	0x00004000	0x0	Strip address
EN	0x00002000	0x0	Enable address
NS	0x00001000	0x0	No spill
RD	0x00000800	0x0	RX descriptors available
RX	0x00000400	0x0	RX active
AT	0x00000200	0x0	Abort TX
RA	0x00000100	-	RX AHB error

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
TA	0x00000080	-	TX AHB error
PR	0x00000040	-	Packet received
PS	0x00000020	-	Packet sent
AI	0x00000010	0x0	AHB error interrupt
RI	0x00000008	0x0	Receive interrupt
TI	0x00000004	0x0	Transmit interrupt
RE	0x00000002	0x0	Receiver enable
TE	0x00000001	0x0	Transmitter enable

Register DMACTRL

Description

DMA control/status register

Reset value

0x00000000

Warm reset mask

0x0001fe1f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-								EP	TR	-		RP	TP	TL	LE	SP	SA	EN	NS	RD	RX	AT	RA	TA	PR	PS	AI	RI	TI	RE	TE
-								rw	rw	-		rw	rw	rw	rw	rw	rw	rw	rw	rw	ro	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-								-	-	-		-	-	-	0	0	0	0	0	0	0	0	-	-	-	-	0	0	0	0	0

Field	Mask	Reset	Description
EP	0x00800000	-	EEP termination
TR	0x00400000	-	Truncated
RP	0x00080000	-	Receive packet IRQ
TP	0x00040000	-	Transmit packet IRQ
TL	0x00020000	-	Transmitter enable lock
LE	0x00010000	0x0	Link error disable
SP	0x00008000	0x0	Strip PID
SA	0x00004000	0x0	Strip address
EN	0x00002000	0x0	Enable address
NS	0x00001000	0x0	No spill
RD	0x00000800	0x0	RX descriptors available
RX	0x00000400	0x0	RX active

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
AT	0x00000200	0x0	Abort TX
RA	0x00000100	-	RX AHB error
TA	0x00000080	-	TX AHB error
PR	0x00000040	-	Packet received
PS	0x00000020	-	Packet sent
AI	0x00000010	0x0	AHB error interrupt
RI	0x00000008	0x0	Receive interrupt
TI	0x00000004	0x0	Transmit interrupt
RE	0x00000002	0x0	Receiver enable
TE	0x00000001	0x0	Transmitter enable

Register DMAMAXLEN

Description

DMA RX maximum length register

Reset value

0x00000000

Warm reset mask

0x01fffffc

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-							RXMAXLEN																							-	
-							rw																							-	
-							0																							-	

Field	Mask	Reset	Description
RXMAXLEN	0x01fffffc	0x0	RX maximum length

Register DMAMAXLEN

Description

DMA RX maximum length register

Reset value

0x00000000

Warm reset mask

0x01fffffc

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-							RXMAXLEN																							-	
-							rw																							-	
-							0																							-	

Field	Mask	Reset	Description
RXMAXLEN	0x01fffffc	0x0	RX maximum length

Register DMAMAXLEN

Description

DMA RX maximum length register

Reset value

0x00000000

Warm reset mask

0x01fffffc

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-							RXMAXLEN																							-	
-							rw																							-	
-							0																							-	

Field	Mask	Reset	Description
RXMAXLEN	0x01fffffc	0x0	RX maximum length

Register DMAMAXLEN

Description

DMA RX maximum length register

Reset value

0x00000000

Warm reset mask

0x01fffffc

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-							RXMAXLEN																							-	
-							rw																							-	
-							0																							-	

Field	Mask	Reset	Description
RXMAXLEN	0x01fffffc	0x0	RX maximum length

Register DMATXDESC

Description

DMA transmit descriptor table address register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0xfffffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESCBASEADDR																						DESCSEL						-			
rw																						rw						-			
0																						0						-			

Field	Mask	Reset	Description
DESCBASEADDR	0xfffffc00	0x0	Descriptor table base address
DESCSEL	0x000003f0	0x0	Descriptor selector

Register DMATXDESC

Description

DMA transmit descriptor table address register

Reset value

0x00000000

Warm reset mask

0xfffffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESCBASEADDR																						DESCSEL						-			
rw																						rw						-			
0																						0						-			

Field	Mask	Reset	Description
DESCBASEADDR	0xfffffc00	0x0	Descriptor table base address
DESCSEL	0x000003f0	0x0	Descriptor selector

Register DMATXDESC

Description

DMA transmit descriptor table address register

Reset value

0x00000000

Warm reset mask

0xfffffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESCBASEADDR																						DESCSEL						-			
rw																						rw						-			
0																						0						-			

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
DESCBASEADDR	0xfffffc00	0x0	Descriptor table base address
DESCSEL	0x000003f0	0x0	Descriptor selector

Register DMATXDESC

Description

DMA transmit descriptor table address register

Reset value

0x00000000

Warm reset mask

0xfffffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESCBASEADDR																						DESCSEL						-			
rw																						rw						-			
0																						0						-			

Field	Mask	Reset	Description
DESCBASEADDR	0xfffffc00	0x0	Descriptor table base address
DESCSEL	0x000003f0	0x0	Descriptor selector

Register DMARXDESC

Description

DMA receive descriptor table address register

Reset value

0x00000000

Warm reset mask

0xfffffff8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESCBASEADDR																						DESCSEL							-		
rw																						rw							-		
0																						0							-		

Field	Mask	Reset	Description
DESCBASEADDR	0xfffffc00	0x0	Descriptor table base address
DESCSEL	0x000003f8	0x0	Descriptor selector

Register DMARXDESC

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

DMA receive descriptor table address register

Reset value

0x00000000

Warm reset mask

0xffffffff8

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3	2 1 0
DESCBASEADDR	DESCSEL	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
DESCBASEADDR	0xfffffc00	0x0	Descriptor table base address
DESCSEL	0x000003f8	0x0	Descriptor selector

Register DMARXDESC

Description

DMA receive descriptor table address register

Reset value

0x00000000

Warm reset mask

0xffffffff8

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3	2 1 0
DESCBASEADDR	DESCSEL	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
DESCBASEADDR	0xfffffc00	0x0	Descriptor table base address
DESCSEL	0x000003f8	0x0	Descriptor selector

Register DMARXDESC

Description

DMA receive descriptor table address register

Reset value

0x00000000

Warm reset mask

0xffffffff8

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3	2 1 0
DESCBASEADDR	DESCSEL	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
DESCBASEADDR	0xfffffc00	0x0	Descriptor table base address
DESCSEL	0x000003f8	0x0	Descriptor selector

Register DMAADDR

Description

DMA address register

Reset value

0x00000000

Warm reset mask

0x0000ffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
-	MASK	ADDR
-	rw	rw
-	0	0

Field	Mask	Reset	Description
MASK	0x0000ff00	0x0	Mask
ADDR	0x000000ff	0x0	Address

Register DMAADDR

Description

DMA address register

Reset value

0x00000000

Warm reset mask

0x0000ffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
-	MASK	ADDR
-	rw	rw
-	0	0

Field	Mask	Reset	Description
MASK	0x0000ff00	0x0	Mask
ADDR	0x000000ff	0x0	Address

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register DMAADDR

Description

DMA address register

Reset value

0x00000000

Warm reset mask

0x0000ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																MASK								ADDR							
-																rw								rw							
-																0								0							

Field	Mask	Reset	Description
MASK	0x0000ff00	0x0	Mask
ADDR	0x000000ff	0x0	Address

Register DMAADDR

Description

DMA address register

Reset value

0x00000000

Warm reset mask

0x0000ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																MASK								ADDR							
-																rw								rw							
-																0								0							

Field	Mask	Reset	Description
MASK	0x0000ff00	0x0	Mask
ADDR	0x000000ff	0x0	Address

Commands

Name	Description
delete	Dispose instance of Grspw2

9.11.5. Limitations

The following deviations from real hardware are known to exist with this model:

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

- The device already provides two ports, dual port is not yet implemented. Let us know if you need this feature implemented.
- The link interface currently effectively uses only *ErrorReset*, *Ready*, *Connecting* and *Run* states. These are the only values that will be visible on the status register.
- RMAPEN and PNPEN signals not available.

9.11.6. Examples

This example shows how to create two Grspw2 devices and connect them:

Listing 25. Creating and Connecting GRSPW2 Devices

```
import BusModels
import TEMUGrspw2
Grspw2.new name=grspw0
Grspw2.new name=grspw1
spw-connect port1=grspw0:SpwPortIface[0] port2=grspw1:SpwPortIface[0]
```

9.12. IRQAMP

The IRQAMP is part of the GRLIB device library from Gaisler. It is a multiprocessor capable interrupt controller.

The controller supports among things the routing of interrupts to different processor cores, and also broadcasted interrupts.

The device supports the boot address registers.

9.12.1. Loading the Plugin

```
import IrqAMp
```

9.12.2. Configuration

9.12.3. @IRQAMP Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @IRQAMP
new	Create new instance of IRQAMP

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.12.4. IRQAMP Reference

Properties

Name	Type	Description
ASMPCTRL	uint32_t	Asymmetric multiprocessing control register
ASMPCTRLColdResetValue	uint32_t	Asymmetric multiprocessing control register
ASMPCTRLForcedBits	uint32_t	Asymmetric multiprocessing control register
ASMPCTRLForcedFlippedBits	uint32_t	Asymmetric multiprocessing control register
ASMPCTRLReadMask	uint32_t	Asymmetric multiprocessing control register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ASMPCTRLResetMask	uint32_t	Asymmetric multiprocessing control register
ASMPCTRLResetValue	uint32_t	Asymmetric multiprocessing control register
ASMPCTRLWriteMask	uint32_t	Asymmetric multiprocessing control register
BRDCSTColdResetValue	uint32_t	Broadcast register
BRDCSTForcedBits	uint32_t	Broadcast register
BRDCSTForcedFlippedBits	uint32_t	Broadcast register
BRDCSTReadMask	uint32_t	Broadcast register
BRDCSTResetMask	uint32_t	Broadcast register
BRDCSTResetValue	uint32_t	Broadcast register
BRDCSTWriteMask	uint32_t	Broadcast register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
ERRSTAT	uint32_t	Error mode status register
ERRSTATColdResetValue	uint32_t	Error mode status register
ERRSTATForcedBits	uint32_t	Error mode status register
ERRSTATForcedFlippedBits	uint32_t	Error mode status register
ERRSTATReadMask	uint32_t	Error mode status register
ERRSTATResetMask	uint32_t	Error mode status register
ERRSTATResetValue	uint32_t	Error mode status register
ERRSTATWriteMask	uint32_t	Error mode status register
ICLEARColdResetValue	uint32_t	Interrupt clear register
ICLEARForcedBits	uint32_t	Interrupt clear register
ICLEARForcedFlippedBits	uint32_t	Interrupt clear register
ICLEARReadMask	uint32_t	Interrupt clear register
ICLEARResetMask	uint32_t	Interrupt clear register
ICLEARResetValue	uint32_t	Interrupt clear register
ICLEARWriteMask	uint32_t	Interrupt clear register
ICSELR	[uint32_t; 2]	Interrupt controller select register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ILEVELColdResetValue	uint32_t	Interrupt level register
ILEVELForcedBits	uint32_t	Interrupt level register
ILEVELForcedFlippedBits	uint32_t	Interrupt level register
ILEVELReadMask	uint32_t	Interrupt level register
ILEVELResetMask	uint32_t	Interrupt level register
ILEVELResetValue	uint32_t	Interrupt level register
ILEVELWriteMask	uint32_t	Interrupt level register
IPENDColdResetValue	uint32_t	Interrupt pending register
IPENDForcedBits	uint32_t	Interrupt pending register
IPENDForcedFlippedBits	uint32_t	Interrupt pending register
IPENDReadMask	uint32_t	Interrupt pending register
IPENDResetMask	uint32_t	Interrupt pending register
IPENDResetValue	uint32_t	Interrupt pending register
IPENDWriteMask	uint32_t	Interrupt pending register
ITCNT	[uint32_t; 16]	Interrupt timestamp counter register
ITSTAMPAC	[uint32_t; 16]	Interrupt acknowledge timestamp register
ITSTAMPAS	[uint32_t; 16]	Interrupt assertion timestamp register
ITSTMPC	[uint32_t; 16]	Interrupt timestamp control register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
MPSTATColdResetValue	uint32_t	Multiprocessor status register
MPSTATForcedBits	uint32_t	Multiprocessor status register
MPSTATForcedFlippedBits	uint32_t	Multiprocessor status register
MPSTATReadMask	uint32_t	Multiprocessor status register
MPSTATResetMask	uint32_t	Multiprocessor status register
MPSTATResetValue	uint32_t	Multiprocessor status register
MPSTATWriteMask	uint32_t	Multiprocessor status register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
PBOOT	uint32_t	Processor boot register
PBOOTColdResetValue	uint32_t	Processor boot register
PBOOTForcedBits	uint32_t	Processor boot register
PBOOTForcedFlippedBits	uint32_t	Processor boot register
PBOOTReadMask	uint32_t	Processor boot register
PBOOTResetMask	uint32_t	Processor boot register
PBOOTResetValue	uint32_t	Processor boot register
PBOOTWriteMask	uint32_t	Processor boot register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
acknowledgedInterrupts	[uint64_t; 16]	
bootAddress	[uint32_t; 16]	Processor boot address register
broadcast	uint32_t	Broadcast register
config.bootReg	uint8_t	Enable boot address registers
config.enExtIrq	uint8_t	
config.hasErrorModeStatusRegister	uint8_t	Enable error mode status register
config.hasProcessorBootRegister	uint8_t	Enable processor boot register
config.interruptLogMask	uint64_t	
config.irqMapping	uint8_t	Enable interrupt mapping
config.legacyCpuControlDisabled	uint8_t	
config.littleEndian	uint8_t	Endianess of memory interface.
config.logInterrupts	uint8_t	
config.nCpu	uint8_t	
config.numberOfTimeStamps	uint8_t	Number of timestamp registers
config.traceReads	uint8_t	
config.traceWrites	uint8_t	

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
cpu	[temu_IfaceRef; 16]/ <unknown>	Processors
dynamicReset	[temu_IfaceRef; 16]/ <unknown>	Dynamic reset address interface (typically implemented by CPU)
extIntAck	[uint32_t; 16]	Processor extended interrupt acknowledge register
force	[uint32_t; 16]	Processor interrupt force register
interruptMap	[uint32_t; 8]	Interrupt map register
irqClear	uint32_t	Interrupt clear register
irqCtrl	[temu_IfaceRef; 16]/ <unknown>	Upstream interrupt controllers
irqLevel	uint32_t	Interrupt level register
irqPending	uint32_t	Interrupt pending register
irqSignalStatus	[uint16_t; 16]	
irqTimestampMap	[uint32_t; 32]	Auxiliary helper properties to map IRQ numbers to timestamp counters
mask	[uint32_t; 16]	Processor interrupt mask register
mpStatus	uint32_t	Multiprocessor status register
pnp.bar	uint32_t	
pnp.config	uint32_t	
raisedInterrupts	[uint64_t; 16]	
stats.extIrqWhileAsserted	uint64_t	Extended IRQs raised while the eirq line was already asserted and unacked

Interfaces

Name	Type	Description
ApbIface	ApbIface	
DeviceIface	DeviceIface	
IrqClientIface	IrqClientIface	uptree interrupt handlers (e.g. CPUs)
IrqIface	IrqCtrlIface	

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LegacyDisableIface	SignalIface	Signal interface to toggle legacy mode.
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Ports

Prop	Iface	Description
irqCtrl	IrqClientIface	irq port

Registers



Register support is currently experimental!

Register Bank Regs

Register ILEVEL

Description

Interrupt level register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																IL															-
-																rw															-
-																0															-

Field	Mask	Reset	Description
IL	0x0000fffe	0x0	Interrupt level

Register IPEND

Description

Interrupt pending register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIP																IP															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIP	0xffff0000	0x0	Extended interrupt pending
IP	0x0000fffe	0x0	Interrupt pending

Register IFORCE0

Description

Interrupt force register for processor 0

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																IF															-
-																rw															-
-																0															-

Field	Mask	Reset	Description
IF	0x0000fffe	0x0	Interrupt force

Register ICLEAR

Description

Interrupt clear register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIC																IC															-
wo																wo															-
-																-															-

Field	Mask	Reset	Description
EIC	0xffff0000	-	Extended interrupt clear

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IC	0x0000fffe	-	Interrupt clear

Register MPSTAT

Description

Multiprocessor status register

Reset value

0x00000000

Warm reset mask

0xfc0f000f

31 30 29 28	27	26	25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
NCPU	BA	ER	-	EIRQ	-	STATUS
ro	ro	ro	-	ro	-	rw
0	0	0	-	0	-	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x0	Number of CPUs minus one
BA	0x08000000	0x0	Broadcast available
ER	0x04000000	0x0	Extended boot registers available
EIRQ	0x000f0000	0x0	Extended IRQ
STATUS	0x0000000f	0x0	Power-down status of CPU

Register BRDCST

Description

Broadcast register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
-	BM	-
-	rw	-
-	0	-

Field	Mask	Reset	Description
BM	0x0000fffe	0x0	Broadcast mask

Register ERRSTAT

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Description

Error mode status register

Reset value

0x00000000

Warm reset mask

0x0000000f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																												ERRMODE			
-																												rw			
-																												0			

Field	Mask	Reset	Description
ERRMODE	0x0000000f	0x0	Error mode status

Register ASMPCTRL

Description

Asymmetric multiprocessing control register

Reset value

0x30000000

Warm reset mask

0xf0000003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCTRL				-																										ICF	L
ro				-																										rw	rw
3				-																										0	0

Field	Mask	Reset	Description
NCTRL	0xf0000000	0x3	Number of internal controllers
ICF	0x00000002	0x0	Inter-controller force
L	0x00000001	0x0	Lock

Register PBOOT

Description

Processor boot register

Reset value

0x00000000

Warm reset mask

0x00000000

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31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RESET	BOOT
wo	wo
-	-

Field	Mask	Reset	Description
RESET	0xffff0000	-	Reset processors
BOOT	0x0000ffff	-	Boot processors

Register ICSELR

Description

Interrupt controller select register

Reset value

0x00000000

Warm reset mask

0xffff0000

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ICSEL0	ICSEL1	ICSEL2	ICSEL3	-
rw	rw	rw	rw	-
0	0	0	0	-

Field	Mask	Reset	Description
ICSEL0	0xf0000000	0x0	Interrupt controller select for processor n
ICSEL1	0x0f000000	0x0	Interrupt controller select for processor n+1
ICSEL2	0x00f00000	0x0	Interrupt controller select for processor n+2
ICSEL3	0x000f0000	0x0	Interrupt controller select for processor n+3

Register ICSELR

Description

Interrupt controller select register

Reset value

0x00000000

Warm reset mask

0xffff0000

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ICSEL0	ICSEL1	ICSEL2	ICSEL3	-
rw	rw	rw	rw	-
0	0	0	0	-

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Field	Mask	Reset	Description
ICSEL0	0xf0000000	0x0	Interrupt controller select for processor n
ICSEL1	0x0f000000	0x0	Interrupt controller select for processor n+1
ICSEL2	0x00f00000	0x0	Interrupt controller select for processor n+2
ICSEL3	0x000f0000	0x0	Interrupt controller select for processor n+3

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

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Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

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31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0x0000fffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17	16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
IFC	-	IF	-
rw	-	rw	-
-	-	0	-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17	16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
IFC	-	IF	-
rw	-	rw	-
-	-	0	-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17	16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
IFC	-	IF	-
rw	-	rw	-
-	-	0	-

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PEXTACK

Description

Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																											EID				
-																											ro				
-																											0				

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

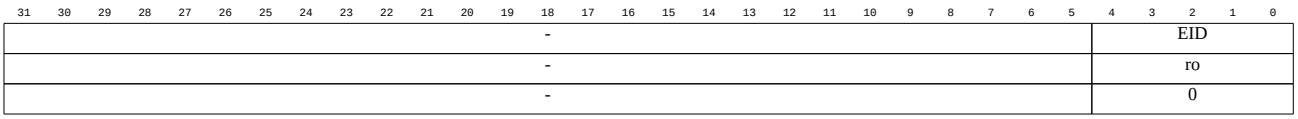
Reset value

0x00000000

Warm reset mask

0x0000001f

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Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

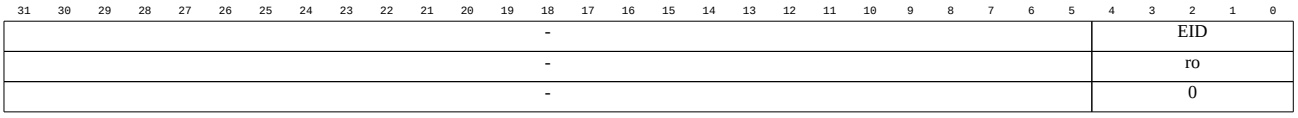
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

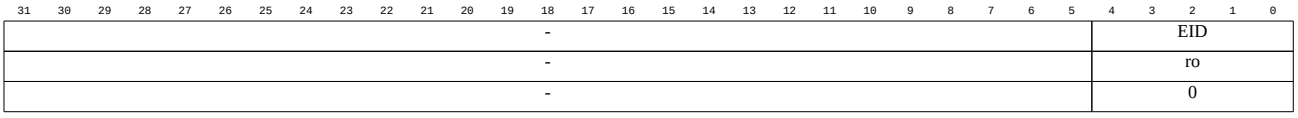
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

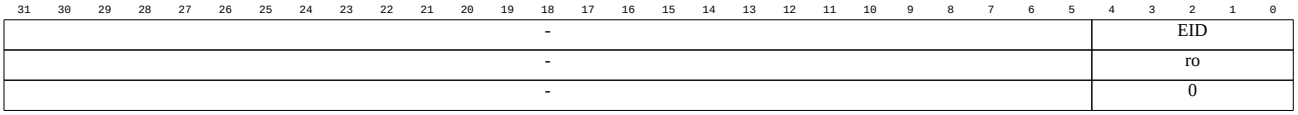
The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

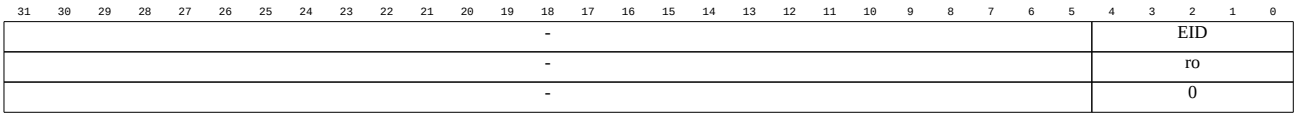
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

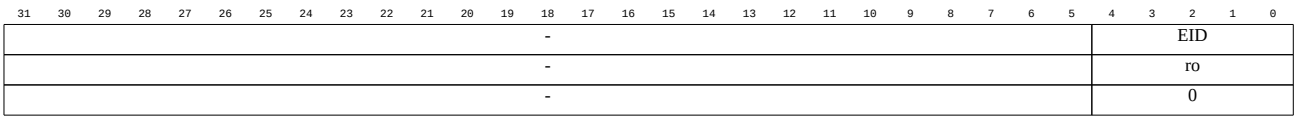
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



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Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

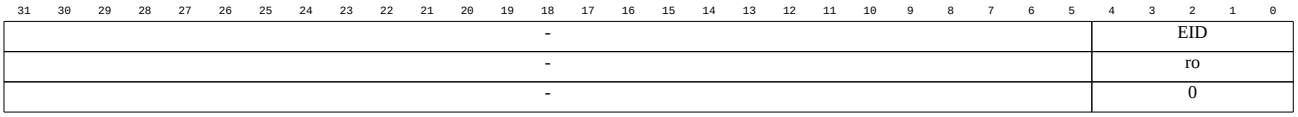
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

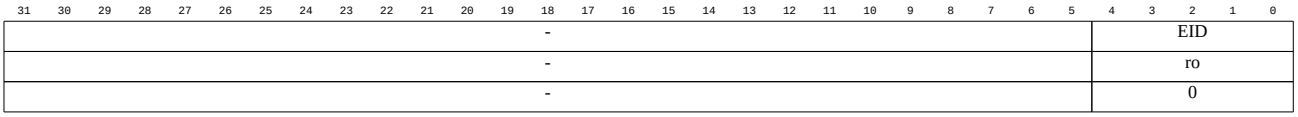
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

Reset value

0x00000000

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Warm reset mask

0x0000001f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																											EID				
-																											ro				
-																											0				

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																											EID				
-																											ro				
-																											0				

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																											EID				
-																											ro				
-																											0				

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

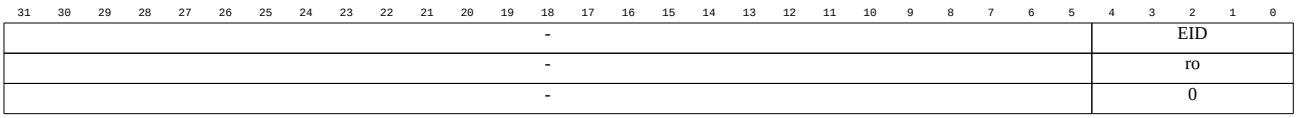
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



31 … 5	4 … 0
-	EID
-	ro
-	0

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

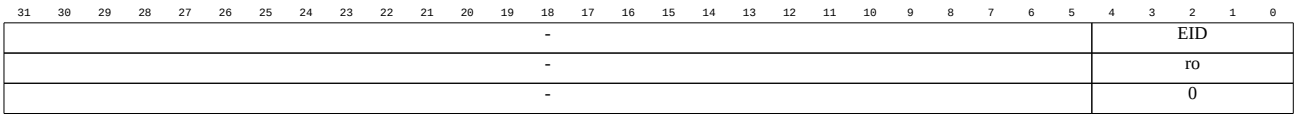
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



31 … 5	4 … 0
-	EID
-	ro
-	0

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

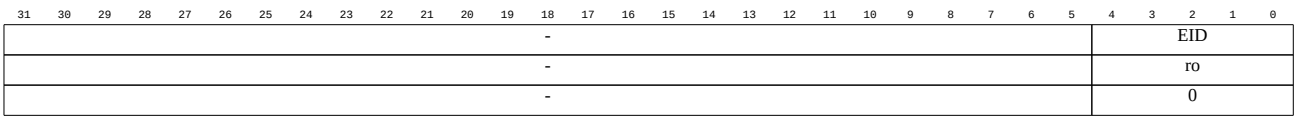
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



31 … 5	4 … 0
-	EID
-	ro
-	0

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

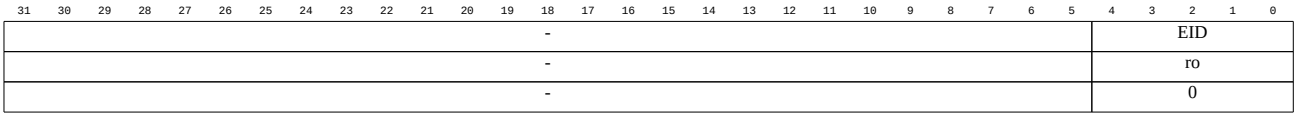
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register ITCNT

Description

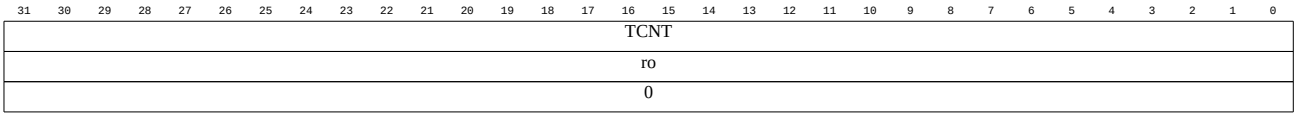
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

Interrupt timestamp counter register

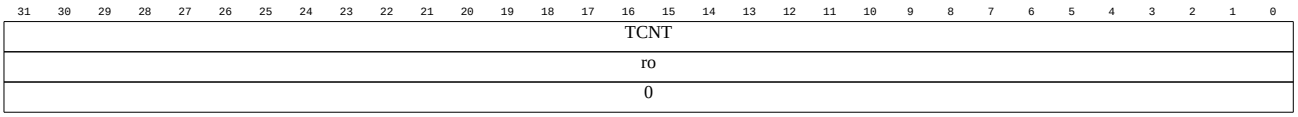
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

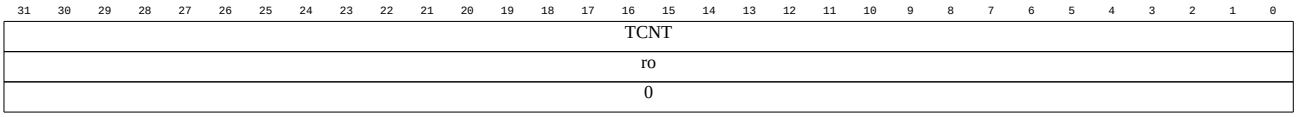
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

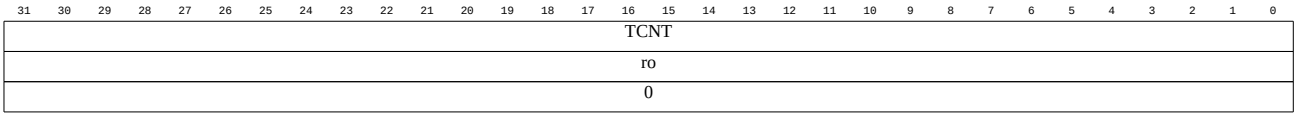
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

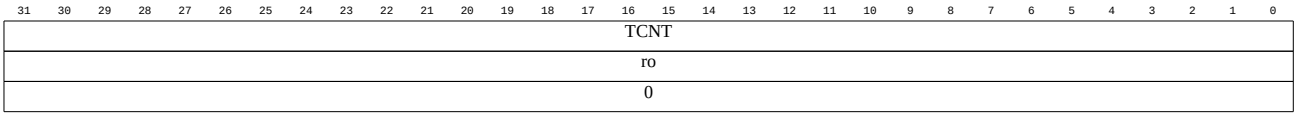
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

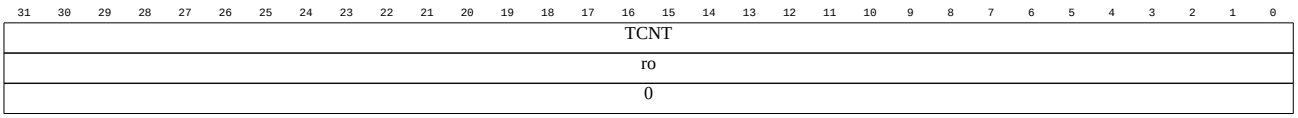
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

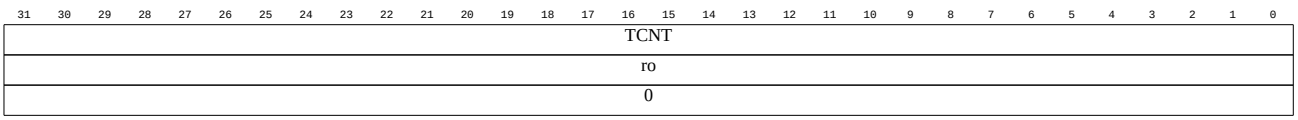
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



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Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

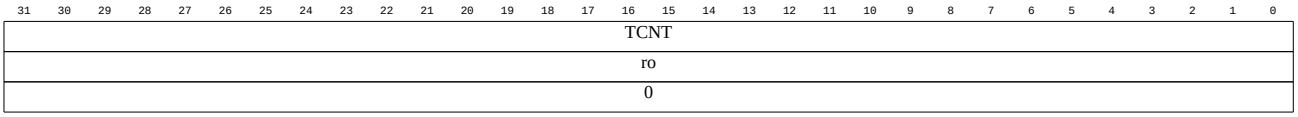
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

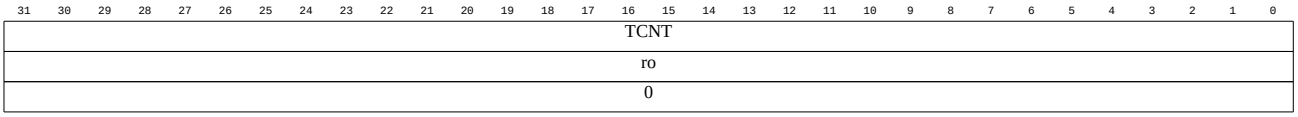
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

Interrupt timestamp counter register

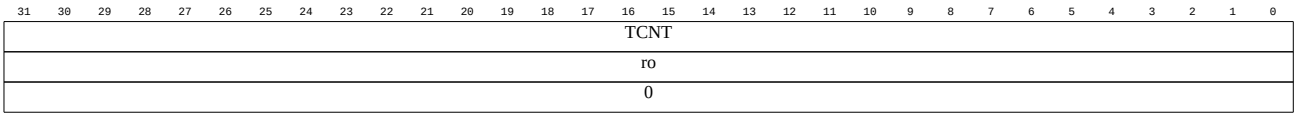
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

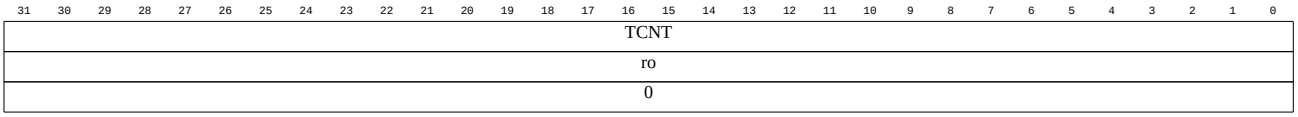
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

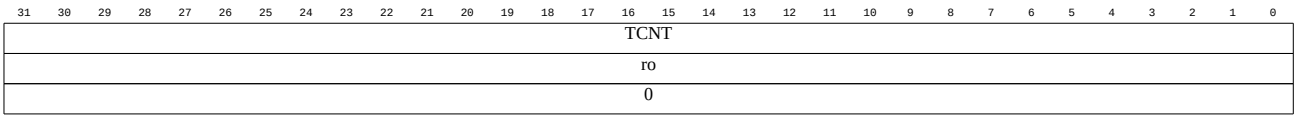
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

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Description

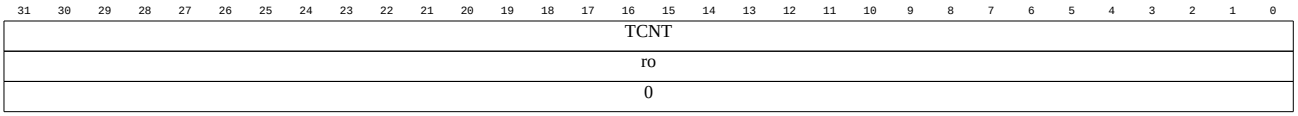
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

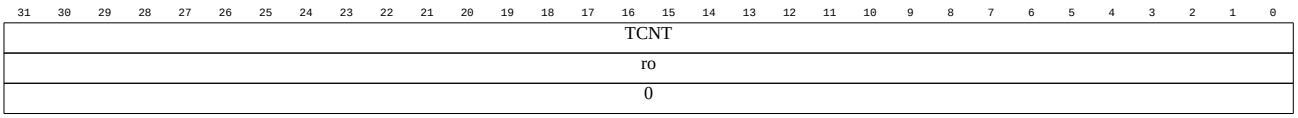
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

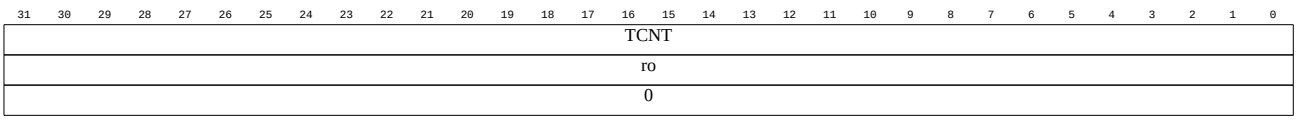
Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff



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Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITCNT

Description

Interrupt timestamp counter register

Reset value

0x00000000

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCNT																															
ro																															
0																															

Field	Mask	Reset	Description
TCNT	0xffffffff	0x0	Timestamp counter

Register ITSTMPC

Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSTAMP					S1	S2	-																			KS	TSISEL				
ro					rw	rw	-																			rw	rw				
2					-	-	-																			0	0				

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

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Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

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Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

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Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

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Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTMPC

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Interrupt timestamp control register

Reset value

0x10000000

Warm reset mask

0xf800003f

31 30 29 28 27	26	25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5	4 3 2 1 0
TSTAMP	S1	S2	-	KS	TSISEL
ro	rw	rw	-	rw	rw
2	-	-	-	0	0

Field	Mask	Reset	Description
TSTAMP	0xf8000000	0x2	Number of timestamp register sets
S1	0x04000000	-	Assertion stamped
S2	0x02000000	-	Acknowledge stamped
KS	0x00000020	0x0	Keep stamp
TSISEL	0x0000001f	0x0	Timestamp interrupt select

Register ITSTAMPAS

Description

Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
TASSERTION
ro
0

Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

Interrupt assertion timestamp register

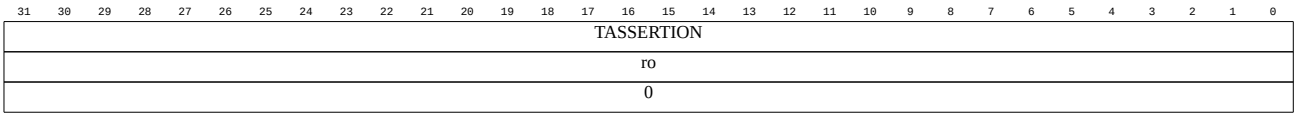
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

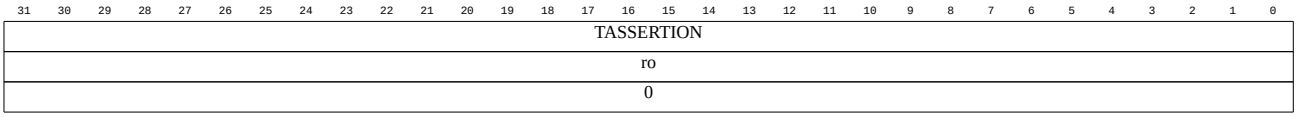
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

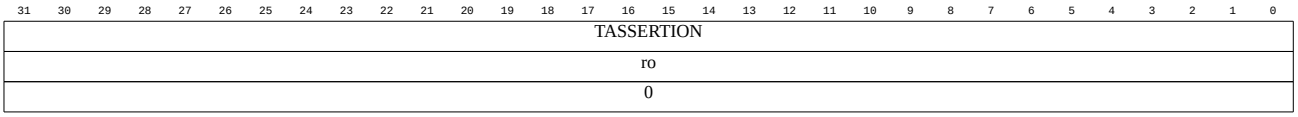
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

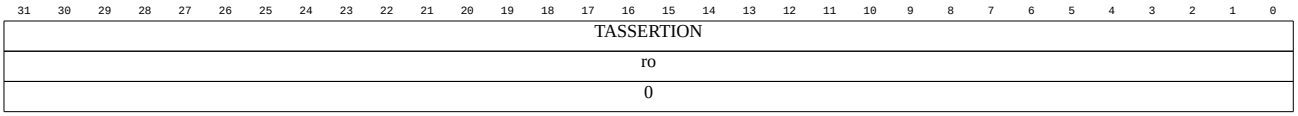
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

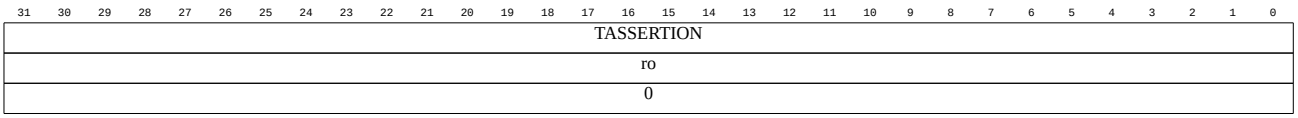
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

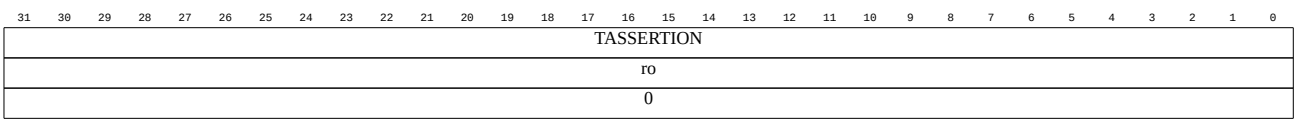
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

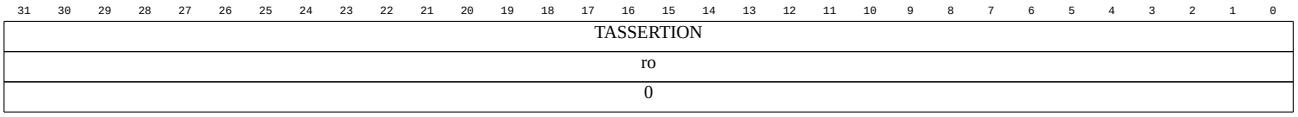
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

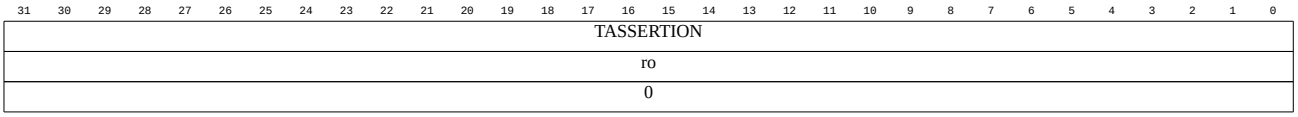
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

Interrupt assertion timestamp register

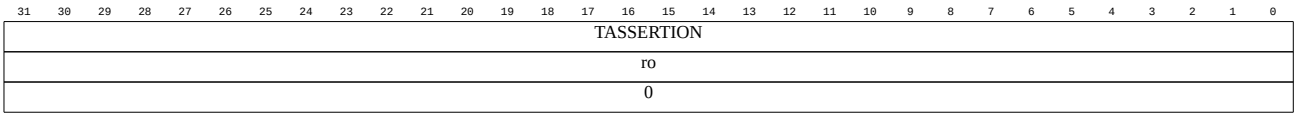
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

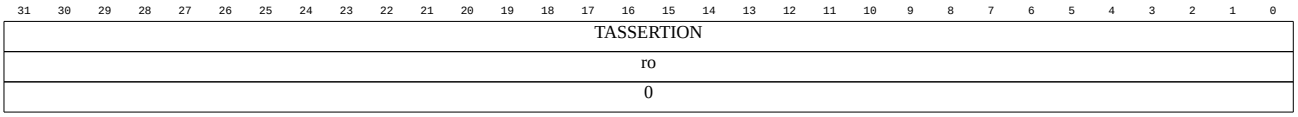
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

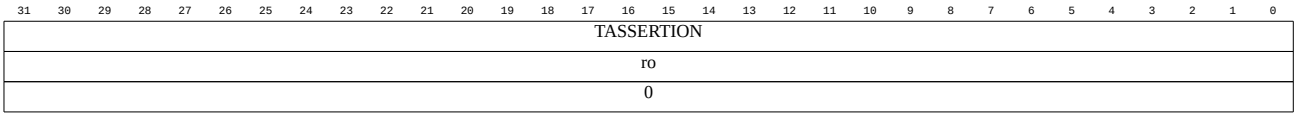
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

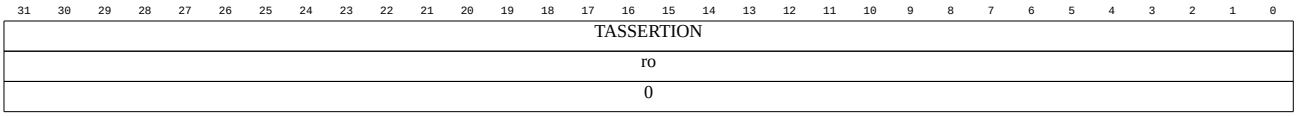
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

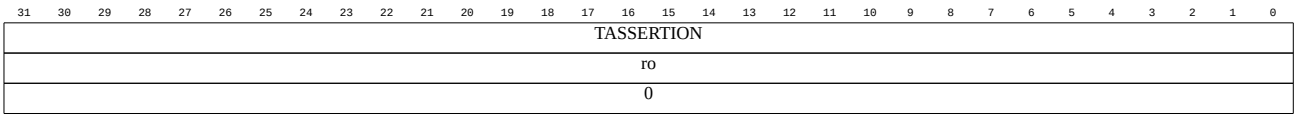
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

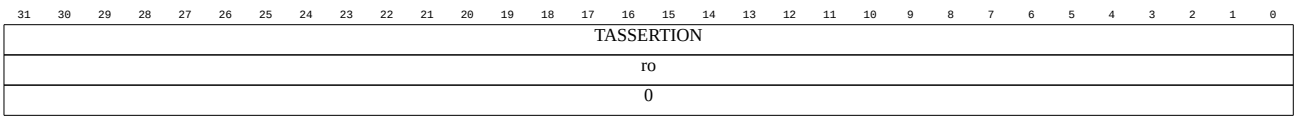
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAS

Description

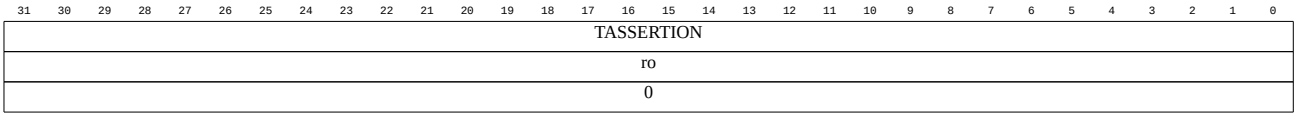
Interrupt assertion timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TASSERTION	0xffffffff	0x0	Timestamp of assertion

Register ITSTAMPAC

Description

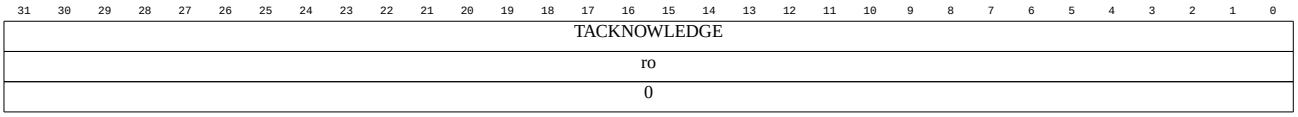
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

Interrupt acknowledge timestamp register

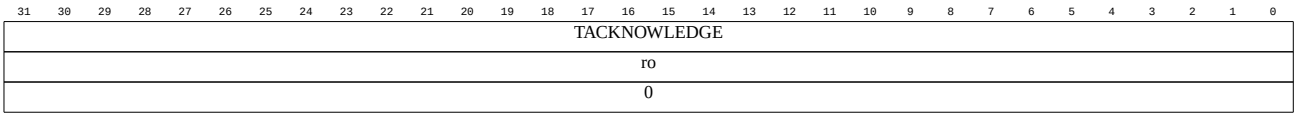
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

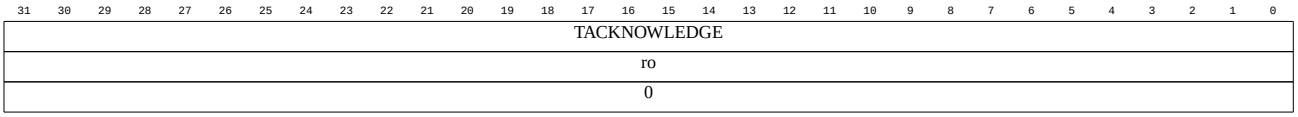
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

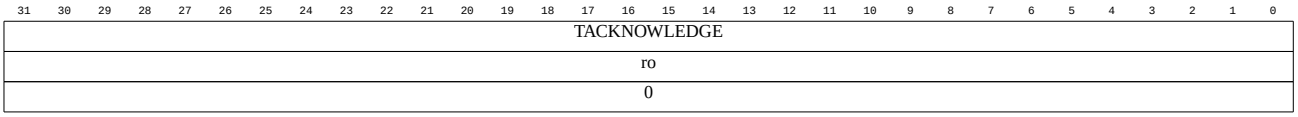
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

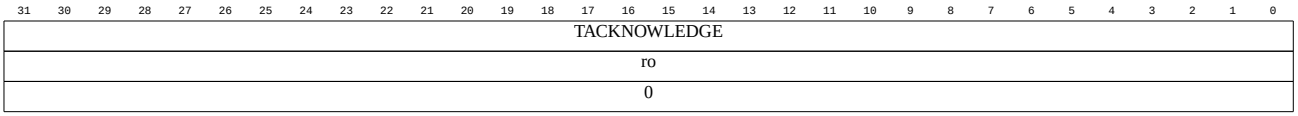
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

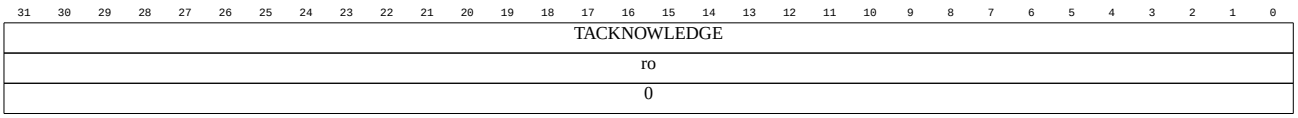
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

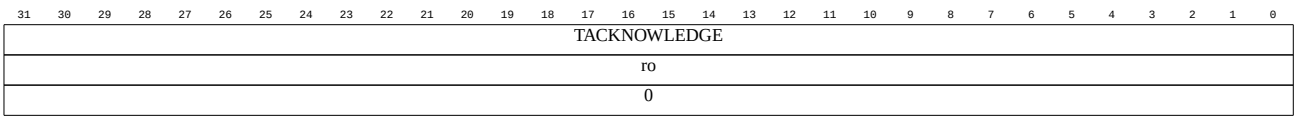
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



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Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

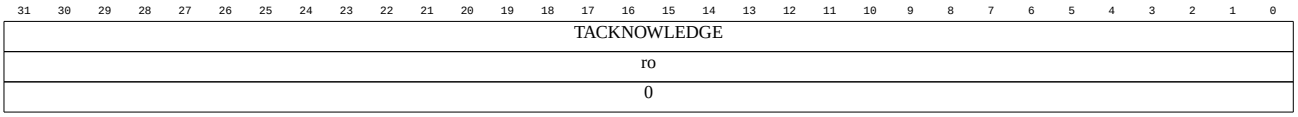
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

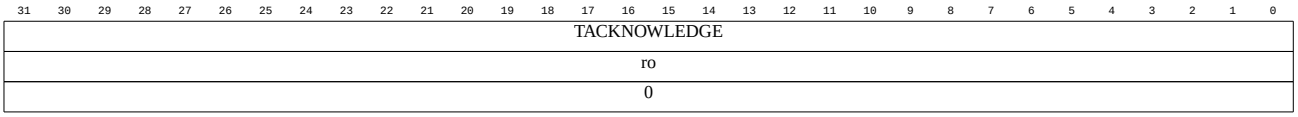
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

Interrupt acknowledge timestamp register

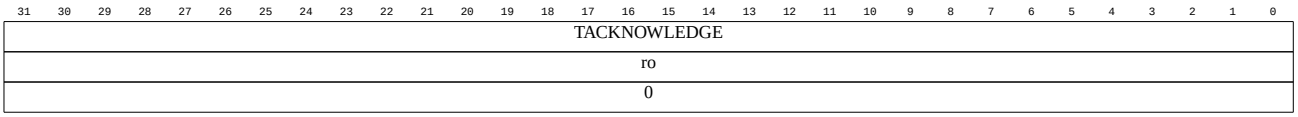
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

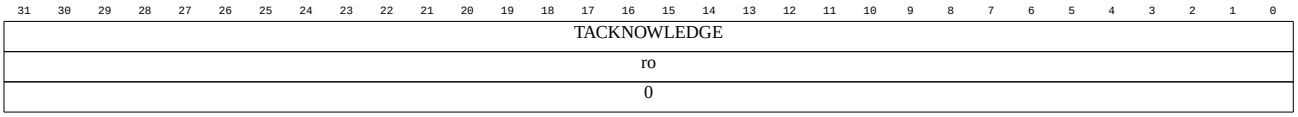
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

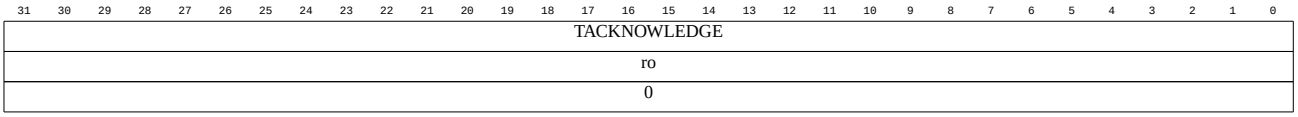
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

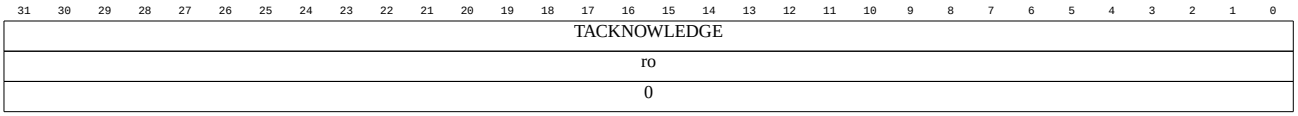
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

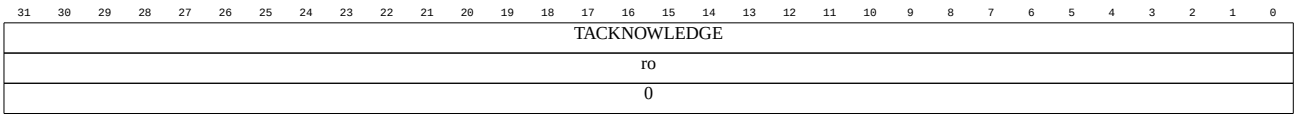
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

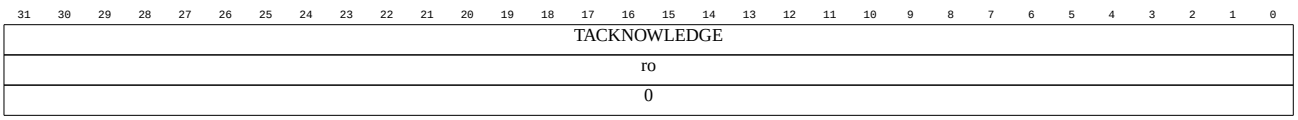
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register ITSTAMPAC

Description

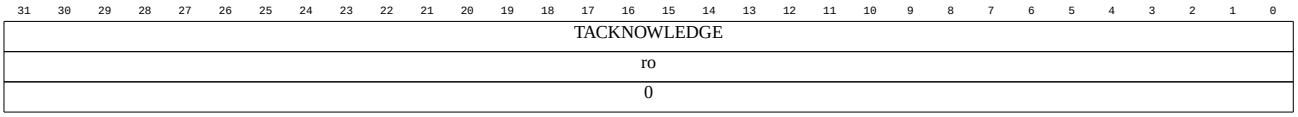
Interrupt acknowledge timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TACKNOWLEDGE	0xffffffff	0x0	Timestamp of acknowledge

Register BADDR

Description

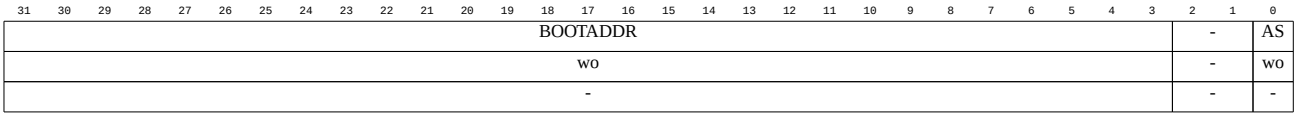
Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

Processor boot address register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0x00000000

31 … 3	2 … 1	0
BOOTADDR	-	AS
WO	-	WO
-	-	-

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000

31 … 3	2 … 1	0
BOOTADDR	-	AS
WO	-	WO
-	-	-

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000

31 … 3	2 … 1	0
BOOTADDR	-	AS
WO	-	WO
-	-	-

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
WO																													-		WO
-																													-		-

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
WO																													-		WO
-																													-		-

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

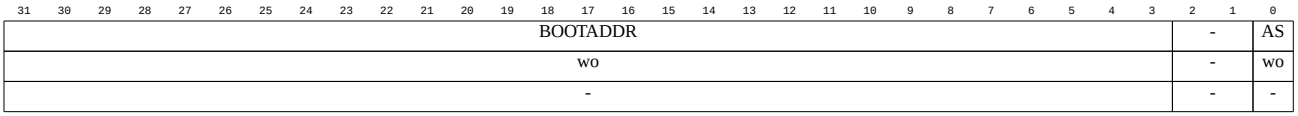
Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

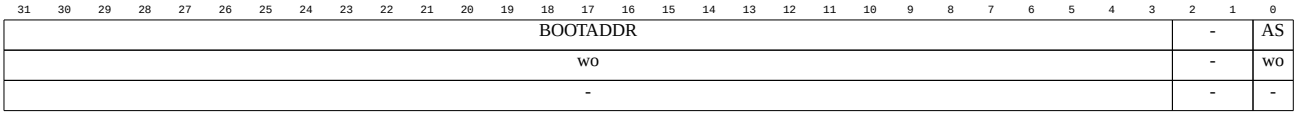
Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

Processor boot address register

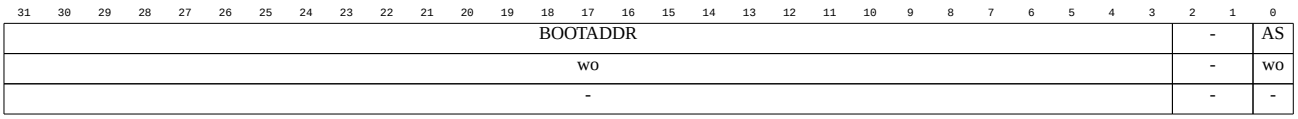
Reset value

0x00000000

Warm reset mask

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.



Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

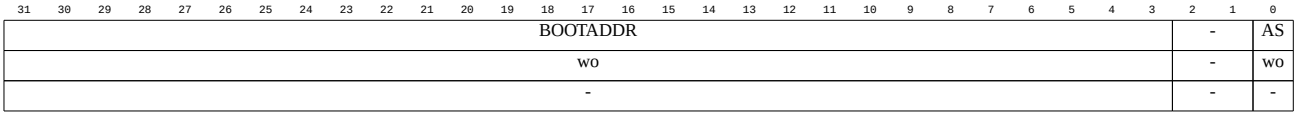
Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

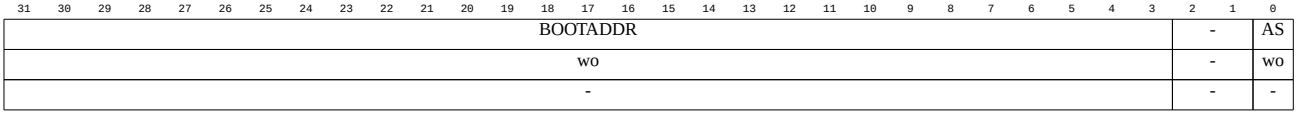
Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register BADDR

Description

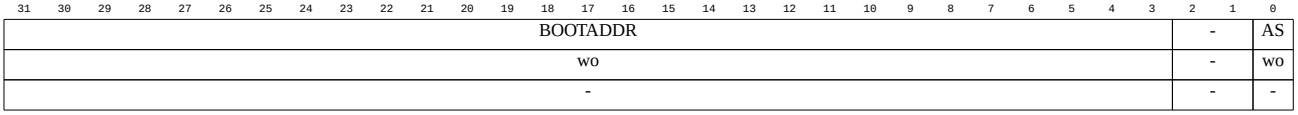
Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

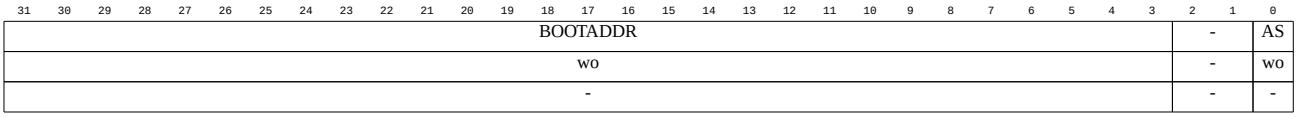
Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

Processor boot address register

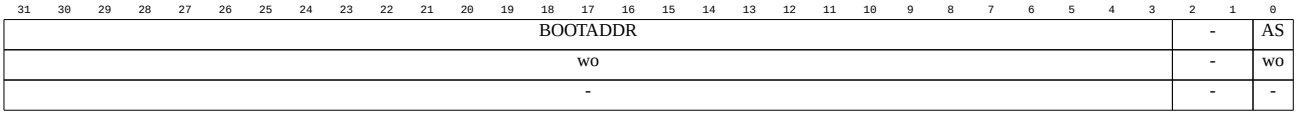
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0x00000000



31 … 2	1	0
BOOTADDR	-	AS
WO	-	WO
-	-	-

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

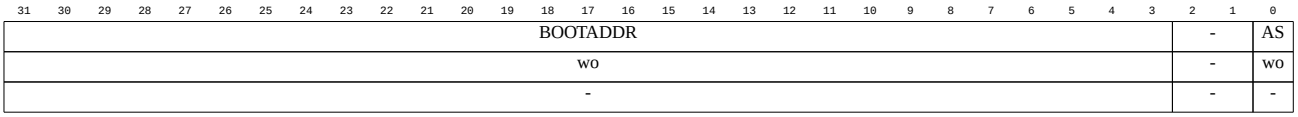
Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000



31 … 2	1	0
BOOTADDR	-	AS
WO	-	WO
-	-	-

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register BADDR

Description

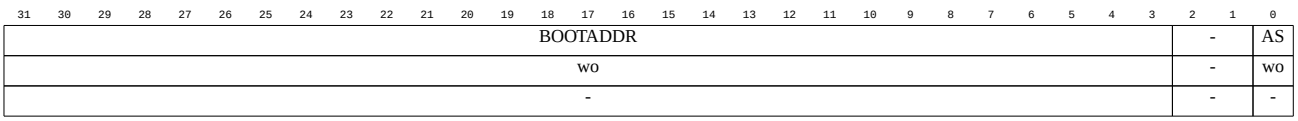
Processor boot address register

Reset value

0x00000000

Warm reset mask

0x00000000



31 … 2	1	0
BOOTADDR	-	AS
WO	-	WO
-	-	-

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	-	Processor boot address
AS	0x00000001	-	Auto start

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Commands

Name	Description
delete	Dispose instance of IRQAMP

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Description
raiseExternalIrq	Raise interrupt

Command raiseExternalIrq Arguments

Name	Type	Required	Description
irq	int	yes	Interrupt number

9.12.5. Limitations

The following deviations from real hardware are known to exist with this model:

- Broadcasted interrupts are broadcasted at the current time to all CPUs. If triggered by a non-synchronised event, the interrupt is raised at different times on the different cores. Depending on the IRQ frequency and the configured quanta length, this may result in problems for some software.
- The model does not verify that register writes come from the correct CPU at the moment.

9.13. IRQMP

The IrqMP is part of the GRLIB device library from Gaisler. It is a multiprocessor capable interrupt controller.

The controller supports routing interrupts to different processor cores and broadcasted interrupts.

9.13.1. Loading the Plugin

```
import IrqMp
```

9.13.2. Configuration

config.nCpu
: Number of processors supported.

config.enExtIrq
: Enable extended IRQs.

pnp.config
: Plug and play configuration word for APB plug-and-play.

cpu
: Up to 16 CPUs supported. IfaceRef property should be connected to the different CPUs.

9.13.3. @IrqMp Reference

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @IrqMp
new	Create new instance of IrqMp

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.13.4. IrqMp Reference

Properties

Name	Type	Description
BRDCSTColdResetValue	uint32_t	Broadcast register
BRDCSTForcedBits	uint32_t	Broadcast register
BRDCSTForcedFlippedBits	uint32_t	Broadcast register
BRDCSTReadMask	uint32_t	Broadcast register
BRDCSTResetMask	uint32_t	Broadcast register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BRDCSTResetValue	uint32_t	Broadcast register
BRDCSTWriteMask	uint32_t	Broadcast register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
ICLEARColdResetValue	uint32_t	Interrupt clear register
ICLEARForcedBits	uint32_t	Interrupt clear register
ICLEARForcedFlippedBits	uint32_t	Interrupt clear register
ICLEARReadMask	uint32_t	Interrupt clear register
ICLEARResetMask	uint32_t	Interrupt clear register
ICLEARResetValue	uint32_t	Interrupt clear register
ICLEARWriteMask	uint32_t	Interrupt clear register
IFORCEColdResetValue	uint32_t	Interrupt force register for processor 0
IFORCEForcedBits	uint32_t	Interrupt force register for processor 0
IFORCEForcedFlippedBits	uint32_t	Interrupt force register for processor 0
IFORCEReadMask	uint32_t	Interrupt force register for processor 0
IFORCEResetMask	uint32_t	Interrupt force register for processor 0
IFORCEResetValue	uint32_t	Interrupt force register for processor 0
IFORCEWriteMask	uint32_t	Interrupt force register for processor 0
ILEVELColdResetValue	uint32_t	Interrupt level register
ILEVELForcedBits	uint32_t	Interrupt level register
ILEVELForcedFlippedBits	uint32_t	Interrupt level register
ILEVELReadMask	uint32_t	Interrupt level register
ILEVELResetMask	uint32_t	Interrupt level register
ILEVELResetValue	uint32_t	Interrupt level register
ILEVELWriteMask	uint32_t	Interrupt level register
IPENDColdResetValue	uint32_t	Interrupt pending register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
IPENDForcedBits	uint32_t	Interrupt pending register
IPENDForcedFlippedBits	uint32_t	Interrupt pending register
IPENDReadMask	uint32_t	Interrupt pending register
IPENDResetMask	uint32_t	Interrupt pending register
IPENDResetValue	uint32_t	Interrupt pending register
IPENDWriteMask	uint32_t	Interrupt pending register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
MPSTATColdResetValue	uint32_t	Multiprocessor status register
MPSTATForcedBits	uint32_t	Multiprocessor status register
MPSTATForcedFlippedBits	uint32_t	Multiprocessor status register
MPSTATReadMask	uint32_t	Multiprocessor status register
MPSTATResetMask	uint32_t	Multiprocessor status register
MPSTATResetValue	uint32_t	Multiprocessor status register
MPSTATWriteMask	uint32_t	Multiprocessor status register
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
bootAddress	[uint32_t; 16]	Processor boot address register
broadcast	uint32_t	Broadcast register
config.bootReg	uint8_t	Enable boot address registers
config.enExtIrq	uint8_t	
config.irqMapping	uint8_t	Enable interrupt mapping
config.littleEndian	uint8_t	Endianess of memory interface.
config.logInterrupts	uint8_t	
config.nCpu	uint8_t	
config.traceReads	uint8_t	
config.traceWrites	uint8_t	

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
cpu	[temu_IfaceRef; 16]/ <unknown>	Processors
extIntAck	[uint32_t; 16]	Processor extended interrupt acknowledge register
force	[uint32_t; 16]	Processor interrupt force register
interruptMap	[uint32_t; 8]	Interrupt map register
irqClear	uint32_t	Interrupt clear register
irqCtrl	[temu_IfaceRef; 16]/ <unknown>	Upstream interrupt controllers (e.g. processor)
irqForce0	uint32_t	Interrupt force register for processor 0
irqLevel	uint32_t	Interrupt level register
irqPending	uint32_t	Interrupt pending register
irqSignalStatus	[uint16_t; 16]	
mask	[uint32_t; 16]	Processor interrupt mask register
mpStatus	uint32_t	Multiprocessor status register
pnp.bar	uint32_t	
pnp.config	uint32_t	

Interfaces

Name	Type	Description
ApbIface	ApbIface	
DeviceIface	DeviceIface	
IrqClientIface	IrqClientIface	uptree interrupt handlers (e.g. CPUs)
IrqIface	IrqCtrlIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Ports

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Prop	Iface	Description
irqCtrl	IrqClientIface	irq port

Registers



Register support is currently experimental!

Register Bank Regs

Register ILEVEL

Description

Interrupt level register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																IL															-
-																rw															-
-																0															-

Field	Mask	Reset	Description
IL	0x0000fffe	0x0	Interrupt level

Register IPEND

Description

Interrupt pending register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIP																IP															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIP	0xffff0000	0x0	Extended interrupt pending
IP	0x0000fffe	0x0	Interrupt pending

Register IFORCE

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Interrupt force register for processor 0

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																IF															-
-																rw															-
-																0															-

Field	Mask	Reset	Description
IF	0x0000fffe	0x0	Interrupt force for processor 0

Register ICLEAR

Description

Interrupt clear register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIC																IC															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIC	0xffff0000	0x0	Extended interrupt clear
IC	0x0000fffe	0x0	Interrupt clear

Register MPSTAT

Description

Multiprocessor status register

Reset value

0x00000000

Warm reset mask

0xfc0fffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31 30 29 28	27	26	25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
NCPU	BA	ER	-	EIRQ	STATUS
ro	ro	ro	-	ro	rw
0	0	0	-	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x0	Number of CPUs minus one
BA	0x08000000	0x0	Broadcast available
ER	0x04000000	0x0	Extended boot registers available
EIRQ	0x000f0000	0x0	Extended IRQ
STATUS	0x0000ffff	0x0	Power-down status of CPU

Register BRDCST

Description

Broadcast register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
-	BM	-
-	rw	-
-	0	-

Field	Mask	Reset	Description
BM	0x0000fffe	0x0	Broadcast mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

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31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

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Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

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Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIM																IM															-
rw																rw															-
0																0															-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIMASK

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Description

Processor interrupt mask register

Reset value

0x00000000

Warm reset mask

0xfffffffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
EIM	IM	-
rw	rw	-
0	0	-

Field	Mask	Reset	Description
EIM	0xffff0000	0x0	Extended interrupt mask
IM	0x0000fffe	0x0	Interrupt mask

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
IFC	-	IF	-
rw	-	rw	-
-	-	0	-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

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Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

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Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	`0xfffe0000`	`-`	Interrupt force clear
IF	`0x0000fffe`	`0x0`	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	`0xfffe0000`	`-`	Interrupt force clear
IF	`0x0000fffe`	`0x0`	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

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Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

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Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

Register PIFORCE

Description

Processor interrupt force register

Reset value

0x00000000

Warm reset mask

0x0000fffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFC															-	IF															-
rw															-	rw															-
-															-	0															-

Field	Mask	Reset	Description
IFC	0xfffe0000	-	Interrupt force clear
IF	0x0000fffe	0x0	Interrupt force

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register PEXTACK

Description

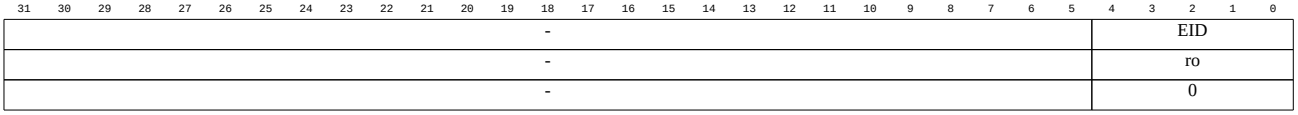
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

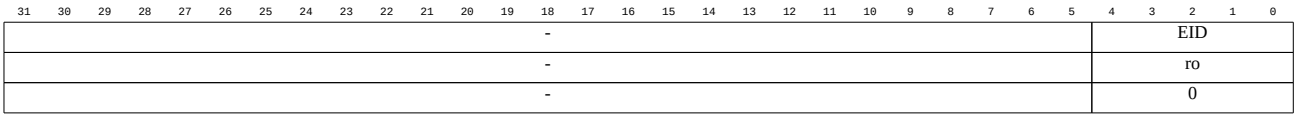
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	EID
-	ro
-	0

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	EID
-	ro
-	0

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	EID
-	ro
-	0

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

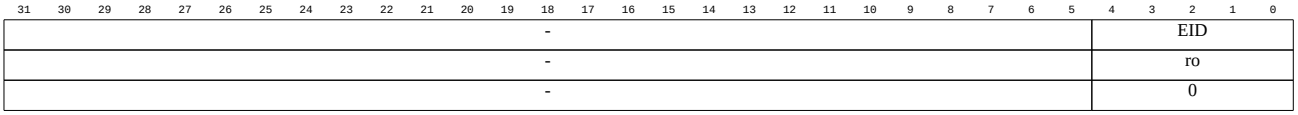
The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

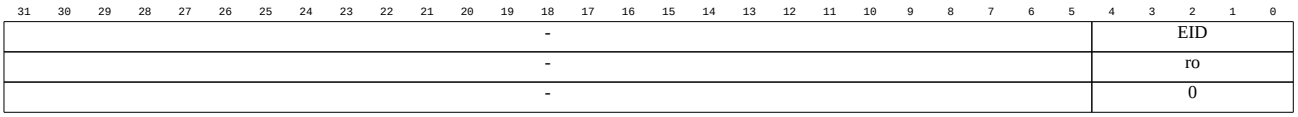
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

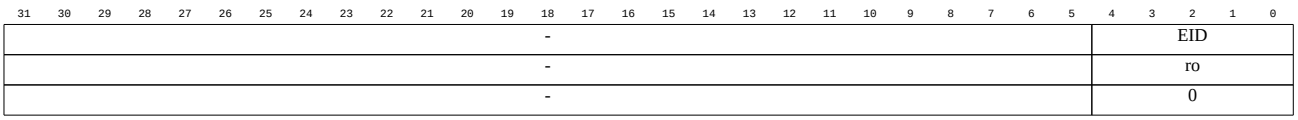
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

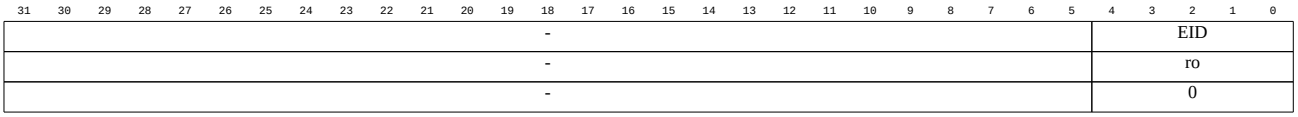
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

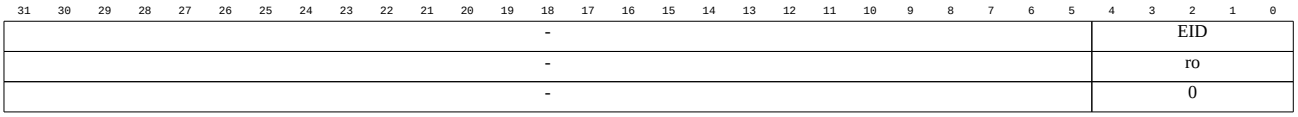
Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f



Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0x0000001f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																											EID				
-																											ro				
-																											0				

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																											EID				
-																											ro				
-																											0				

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

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Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																											EID				
-																											ro				
-																											0				

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

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Description

Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	EID
-	ro
-	0

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	EID
-	ro
-	0

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register PEXTACK

Description

Processor extended interrupt acknowledge register

Reset value

0x00000000

Warm reset mask

0x0000001f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	EID
-	ro
-	0

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
EID	0x0000001f	0x0	Extended interrupt ID

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3	2	1	0
BOOTADDR	-		AS
rw	-		rw
0	-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3	2	1	0
BOOTADDR	-		AS
rw	-		rw
0	-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3	2	1	0
BOOTADDR	-		AS
rw	-		rw
0	-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register BADDR

Description

Processor boot address register

Reset value

0x00000000

Warm reset mask

0xfffffff9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTADDR																													-		AS
rw																													-		rw
0																													-		0

Field	Mask	Reset	Description
BOOTADDR	0xfffffff8	0x0	Processor boot address
AS	0x00000001	0x0	Auto start

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQMAP0								IRQMAP1								IRQMAP2								IRQMAP3							
rw								rw								rw								rw							
0								0								0								0							

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Register IRQMAP

Description

Interrupt map register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
IRQMAP0	IRQMAP1	IRQMAP2	IRQMAP3
rw	rw	rw	rw
0	0	0	0

Field	Mask	Reset	Description
IRQMAP0	0xff000000	0x0	Interrupt map field n
IRQMAP1	0x00ff0000	0x0	Interrupt map field n+1
IRQMAP2	0x0000ff00	0x0	Interrupt map field n+2
IRQMAP3	0x000000ff	0x0	Interrupt map field n+3

Commands

Name	Description
delete	Dispose instance of IrqMp
raiseExternalIrq	Raise interrupt

Command raiseExternalIrq Arguments

Name	Type	Required	Description
irq	int	yes	Interrupt number

9.13.5. Limitations

The following deviations from real hardware are known to exist with this model:

- Broadcasted interrupts are broadcasted at the current time to all CPUs. If it was triggered by a non-synchronized event, the interrupt is raised at different times on the different cores. Consider the IRQ frequency and the configured quanta length.

9.14. FTMCTRL

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

The FtmCtrl device is part of the GRLIB IP library. It is available in `libTEMUFtmCtrl.so`.

9.14.1. Loading the Plugin

```
import FtmCtrl
```

9.14.2. Configuration

9.14.3. @FtmCtrl Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @FtmCtrl
new	Create new instance of FtmCtrl

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.14.4. FtmCtrl Reference

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
MCFG1ColdResetValue	uint32_t	Memory configuration register 1
MCFG1ForcedBits	uint32_t	Memory configuration register 1
MCFG1ForcedFlippedBits	uint32_t	Memory configuration register 1
MCFG1ReadMask	uint32_t	Memory configuration register 1
MCFG1ResetMask	uint32_t	Memory configuration register 1
MCFG1ResetValue	uint32_t	Memory configuration register 1
MCFG1WriteMask	uint32_t	Memory configuration register 1
MCFG2ColdResetValue	uint32_t	Memory configuration register 2
MCFG2ForcedBits	uint32_t	Memory configuration register 2
MCFG2ForcedFlippedBits	uint32_t	Memory configuration register 2
MCFG2ReadMask	uint32_t	Memory configuration register 2
MCFG2ResetMask	uint32_t	Memory configuration register 2
MCFG2ResetValue	uint32_t	Memory configuration register 2
MCFG2WriteMask	uint32_t	Memory configuration register 2

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
MCFG3ColdResetValue	uint32_t	Memory configuration register 3
MCFG3ForcedBits	uint32_t	Memory configuration register 3
MCFG3ForcedFlippedBits	uint32_t	Memory configuration register 3
MCFG3ReadMask	uint32_t	Memory configuration register 3
MCFG3ResetMask	uint32_t	Memory configuration register 3
MCFG3ResetValue	uint32_t	Memory configuration register 3
MCFG3WriteMask	uint32_t	Memory configuration register 3
MCFG4ColdResetValue	uint32_t	Memory configuration register4
MCFG4ForcedBits	uint32_t	Memory configuration register4
MCFG4ForcedFlippedBits	uint32_t	Memory configuration register4
MCFG4ReadMask	uint32_t	Memory configuration register4
MCFG4ResetMask	uint32_t	Memory configuration register4
MCFG4ResetValue	uint32_t	Memory configuration register4
MCFG4WriteMask	uint32_t	Memory configuration register4
MCFG5ColdResetValue	uint32_t	Memory configuration register 5
MCFG5ForcedBits	uint32_t	Memory configuration register 5
MCFG5ForcedFlippedBits	uint32_t	Memory configuration register 5
MCFG5ReadMask	uint32_t	Memory configuration register 5
MCFG5ResetMask	uint32_t	Memory configuration register 5
MCFG5ResetValue	uint32_t	Memory configuration register 5
MCFG5WriteMask	uint32_t	Memory configuration register 5
MCFG6ColdResetValue	uint32_t	Memory configuration register6

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
MCFG6ForcedBits	uint32_t	Memory configuration register6
MCFG6ForcedFlippedBits	uint32_t	Memory configuration register6
MCFG6ReadMask	uint32_t	Memory configuration register6
MCFG6ResetMask	uint32_t	Memory configuration register6
MCFG6ResetValue	uint32_t	Memory configuration register6
MCFG6WriteMask	uint32_t	Memory configuration register6
MCFG7ColdResetValue	uint32_t	Memory configuration register 7
MCFG7ForcedBits	uint32_t	Memory configuration register 7
MCFG7ForcedFlippedBits	uint32_t	Memory configuration register 7
MCFG7ReadMask	uint32_t	Memory configuration register 7
MCFG7ResetMask	uint32_t	Memory configuration register 7
MCFG7ResetValue	uint32_t	Memory configuration register 7
MCFG7WriteMask	uint32_t	Memory configuration register 7
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
ahb.pnp.bar	[uint32_t; 4]	
ahb.pnp.identReg	uint32_t	
ahb.pnp.userDef	[uint32_t; 3]	
apb.pnp.bar	uint32_t	
apb.pnp.config	uint32_t	
config.littleEndian	uint8_t	Endianess of memory interface.
mcfg1	uint32_t	Memory configuration register 1
mcfg2	uint32_t	Memory configuration register 2

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
mcfg3	uint32_t	Memory configuration register 3
mcfg4	uint32_t	Memory configuration register4
mcfg5	uint32_t	Memory configuration register 5
mcfg6	uint32_t	Memory configuration register6
mcfg7	uint32_t	Memory configuration register 7
memorySpace	temu_IfaceRef/ <unknown>	Memory space.
statCorrectable	temu_IfaceRef/ <unknown>	Statistics device for correctable/upset statistics.
statUncorrectable	temu_IfaceRef/ <unknown>	Statistics device for uncorrectable/faulty statistics.

Interfaces

Name	Type	Description
AhbIface	AhbIface	
ApbIface	ApbIface	
CorrectableErrorIface	MemAccessIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	
UncorrectableErrorIface	MemAccessIface	

Commands

Name	Description
delete	Dispose instance of FtmCtrl

9.14.5. Limitations

9.15. GR1553B

The Gr1553B device is part of the GRLIB IP library. It is available in `libTEMUGr1553B.so`.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

9.15.1. Loading the Plugin

```
import Gr1553B
```

9.15.2. Configuration

9.15.3. @Gr1553B Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @Gr1553B
new	Create new instance of Gr1553B

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.15.4. Gr1553B Reference

Properties

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BCACPColdResetValue	uint32_t	GR1553B BC asynchronous list current slot pointer
BCACPForcedBits	uint32_t	GR1553B BC asynchronous list current slot pointer
BCACPForcedFlippedBits	uint32_t	GR1553B BC asynchronous list current slot pointer
BCACPReadMask	uint32_t	GR1553B BC asynchronous list current slot pointer
BCACPResetMask	uint32_t	GR1553B BC asynchronous list current slot pointer
BCACPResetValue	uint32_t	GR1553B BC asynchronous list current slot pointer
BCACPWriteMask	uint32_t	GR1553B BC asynchronous list current slot pointer
BCAColdResetValue	uint32_t	GR1553B BC action register
BCAForcedBits	uint32_t	GR1553B BC action register
BCAForcedFlippedBits	uint32_t	GR1553B BC action register
BCANPColdResetValue	uint32_t	GR1553B BC asynchronous list next pointer register
BCANPForcedBits	uint32_t	GR1553B BC asynchronous list next pointer register
BCANPForcedFlippedBits	uint32_t	GR1553B BC asynchronous list next pointer register
BCANPReadMask	uint32_t	GR1553B BC asynchronous list next pointer register
BCANPResetMask	uint32_t	GR1553B BC asynchronous list next pointer register
BCANPResetValue	uint32_t	GR1553B BC asynchronous list next pointer register
BCANPWriteMask	uint32_t	GR1553B BC asynchronous list next pointer register
BCAReadMask	uint32_t	GR1553B BC action register
BCAResetMask	uint32_t	GR1553B BC action register
BCAResetValue	uint32_t	GR1553B BC action register
BCAWriteMask	uint32_t	GR1553B BC action register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BCBSColdResetValue	uint32_t	GR1553B BC per-RT bus swap register
BCBSForcedBits	uint32_t	GR1553B BC per-RT bus swap register
BCBSForcedFlippedBits	uint32_t	GR1553B BC per-RT bus swap register
BCBSReadMask	uint32_t	GR1553B BC per-RT bus swap register
BCBSResetMask	uint32_t	GR1553B BC per-RT bus swap register
BCBSResetValue	uint32_t	GR1553B BC per-RT bus swap register
BCBSWriteMask	uint32_t	GR1553B BC per-RT bus swap register
BCRPColdResetValue	uint32_t	GR1553B BC transfer-triggered IRQ ring position register
BCRPForcedBits	uint32_t	GR1553B BC transfer-triggered IRQ ring position register
BCRPForcedFlippedBits	uint32_t	GR1553B BC transfer-triggered IRQ ring position register
BCRPReadMask	uint32_t	GR1553B BC transfer-triggered IRQ ring position register
BCRPResetMask	uint32_t	GR1553B BC transfer-triggered IRQ ring position register
BCRPResetValue	uint32_t	GR1553B BC transfer-triggered IRQ ring position register
BCRPWriteMask	uint32_t	GR1553B BC transfer-triggered IRQ ring position register
BCSCColdResetValue	uint32_t	GR1553B BC status and config register
BCSCForcedBits	uint32_t	GR1553B BC status and config register
BCSCForcedFlippedBits	uint32_t	GR1553B BC status and config register
BCSCReadMask	uint32_t	GR1553B BC status and config register

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Name	Type	Description
BCSCResetMask	uint32_t	GR1553B BC status and config register
BCSCResetValue	uint32_t	GR1553B BC status and config register
BCSCWriteMask	uint32_t	GR1553B BC status and config register
BCTCPColdResetValue	uint32_t	GR1553B BC transfer list current slot pointer
BCTCPForcedBits	uint32_t	GR1553B BC transfer list current slot pointer
BCTCPForcedFlippedBits	uint32_t	GR1553B BC transfer list current slot pointer
BCTCPReadMask	uint32_t	GR1553B BC transfer list current slot pointer
BCTCPResetMask	uint32_t	GR1553B BC transfer list current slot pointer
BCTCPResetValue	uint32_t	GR1553B BC transfer list current slot pointer
BCTCPWriteMask	uint32_t	GR1553B BC transfer list current slot pointer
BCTColdResetValue	uint32_t	GR1553B BC timer register
BCTForcedBits	uint32_t	GR1553B BC timer register
BCTForcedFlippedBits	uint32_t	GR1553B BC timer register
BCTNPColdResetValue	uint32_t	GR1553B BC transfer list next pointer register
BCTNPForcedBits	uint32_t	GR1553B BC transfer list next pointer register
BCTNPForcedFlippedBits	uint32_t	GR1553B BC transfer list next pointer register
BCTNPReadMask	uint32_t	GR1553B BC transfer list next pointer register
BCTNPResetMask	uint32_t	GR1553B BC transfer list next pointer register
BCTNPResetValue	uint32_t	GR1553B BC transfer list next pointer register
BCTNPWriteMask	uint32_t	GR1553B BC transfer list next pointer register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BCTReadMask	uint32_t	GR1553B BC timer register
BCTResetMask	uint32_t	GR1553B BC timer register
BCTResetValue	uint32_t	GR1553B BC timer register
BCTWColdResetValue	uint32_t	GR1553B BC timer wake-up register
BCTWForcedBits	uint32_t	GR1553B BC timer wake-up register
BCTWForcedFlippedBits	uint32_t	GR1553B BC timer wake-up register
BCTWReadMask	uint32_t	GR1553B BC timer wake-up register
BCTWResetMask	uint32_t	GR1553B BC timer wake-up register
BCTWResetValue	uint32_t	GR1553B BC timer wake-up register
BCTWWriteMask	uint32_t	GR1553B BC timer wake-up register
BCTWriteMask	uint32_t	GR1553B BC timer register
BMCColdResetValue	uint32_t	GR1553B BM control register
BMCForcedBits	uint32_t	GR1553B BM control register
BMCForcedFlippedBits	uint32_t	GR1553B BM control register
BMCReadMask	uint32_t	GR1553B BM control register
BMCResetMask	uint32_t	GR1553B BM control register
BMCResetValue	uint32_t	GR1553B BM control register
BMCWriteMask	uint32_t	GR1553B BM control register
BMLBEColdResetValue	uint32_t	GR1553B BM log buffer end register
BMLBEForcedBits	uint32_t	GR1553B BM log buffer end register
BMLBEForcedFlippedBits	uint32_t	GR1553B BM log buffer end register
BMLBEReadMask	uint32_t	GR1553B BM log buffer end register
BMLBEResetMask	uint32_t	GR1553B BM log buffer end register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BMLBEResetValue	uint32_t	GR1553B BM log buffer end register
BMLBEWriteMask	uint32_t	GR1553B BM log buffer end register
BMLBPColdResetValue	uint32_t	GR1553B BM log buffer position register
BMLBPForcedBits	uint32_t	GR1553B BM log buffer position register
BMLBPForcedFlippedBits	uint32_t	GR1553B BM log buffer position register
BMLBPReadMask	uint32_t	GR1553B BM log buffer position register
BMLBPResetMask	uint32_t	GR1553B BM log buffer position register
BMLBPResetValue	uint32_t	GR1553B BM log buffer position register
BMLBPWriteMask	uint32_t	GR1553B BM log buffer position register
BMLBSColdResetValue	uint32_t	GR1553B BM log buffer start register
BMLBSForcedBits	uint32_t	GR1553B BM log buffer start register
BMLBSForcedFlippedBits	uint32_t	GR1553B BM log buffer start register
BMLBSReadMask	uint32_t	GR1553B BM log buffer start register
BMLBSResetMask	uint32_t	GR1553B BM log buffer start register
BMLBSResetValue	uint32_t	GR1553B BM log buffer start register
BMLBSWriteMask	uint32_t	GR1553B BM log buffer start register
BMRTAFColdResetValue	uint32_t	GR1553B BM RT address filter register
BMRTAFForcedBits	uint32_t	GR1553B BM RT address filter register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BMRTAFForcedFlippedBits	uint32_t	GR1553B BM RT address filter register
BMRTAFReadMask	uint32_t	GR1553B BM RT address filter register
BMRTAFResetMask	uint32_t	GR1553B BM RT address filter register
BMRTAFResetValue	uint32_t	GR1553B BM RT address filter register
BMRTAFWriteMask	uint32_t	GR1553B BM RT address filter register
BMRTMCColdResetValue	uint32_t	GR1553B BM RT mode code filter register
BMRTMCForcedBits	uint32_t	GR1553B BM RT mode code filter register
BMRTMCForcedFlippedBits	uint32_t	GR1553B BM RT mode code filter register
BMRTMCReadMask	uint32_t	GR1553B BM RT mode code filter register
BMRTMCResetMask	uint32_t	GR1553B BM RT mode code filter register
BMRTMCResetValue	uint32_t	GR1553B BM RT mode code filter register
BMRTMCWriteMask	uint32_t	GR1553B BM RT mode code filter register
BMRTSFColdResetValue	uint32_t	GR1553B BM RT subaddress filter register
BMRTSFForcedBits	uint32_t	GR1553B BM RT subaddress filter register
BMRTSFForcedFlippedBits	uint32_t	GR1553B BM RT subaddress filter register
BMRTSFReadMask	uint32_t	GR1553B BM RT subaddress filter register
BMRTSFResetMask	uint32_t	GR1553B BM RT subaddress filter register
BMRTSFResetValue	uint32_t	GR1553B BM RT subaddress filter register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BMRTSFWriteMask	uint32_t	GR1553B BM RT subaddress filter register
BMSColdResetValue	uint32_t	GR1553B BM status register
BMSForcedBits	uint32_t	GR1553B BM status register
BMSForcedFlippedBits	uint32_t	GR1553B BM status register
BMSReadMask	uint32_t	GR1553B BM status register
BMSResetMask	uint32_t	GR1553B BM status register
BMSResetValue	uint32_t	GR1553B BM status register
BMSWriteMask	uint32_t	GR1553B BM status register
BMTTCColdResetValue	uint32_t	GR1553B BM time tag control register
BMTTCForcedBits	uint32_t	GR1553B BM time tag control register
BMTTCForcedFlippedBits	uint32_t	GR1553B BM time tag control register
BMTTCReadMask	uint32_t	GR1553B BM time tag control register
BMTTCResetMask	uint32_t	GR1553B BM time tag control register
BMTTCResetValue	uint32_t	GR1553B BM time tag control register
BMTTCWriteMask	uint32_t	GR1553B BM time tag control register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
HCColdResetValue	uint32_t	GR1553B hardware configuration register
HCForcedBits	uint32_t	GR1553B hardware configuration register
HCForcedFlippedBits	uint32_t	GR1553B hardware configuration register
HCReadMask	uint32_t	GR1553B hardware configuration register
HCResetMask	uint32_t	GR1553B hardware configuration register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
HCResetValue	uint32_t	GR1553B hardware configuration register
HCWriteMask	uint32_t	GR1553B hardware configuration register
IRQColdResetValue	uint32_t	GR1553B IRQ register
IRQEColdResetValue	uint32_t	GR1553B IRQ enable register
IRQEForcedBits	uint32_t	GR1553B IRQ enable register
IRQEForcedFlippedBits	uint32_t	GR1553B IRQ enable register
IRQEReadMask	uint32_t	GR1553B IRQ enable register
IRQEResetMask	uint32_t	GR1553B IRQ enable register
IRQEResetValue	uint32_t	GR1553B IRQ enable register
IRQEWriteMask	uint32_t	GR1553B IRQ enable register
IRQForcedBits	uint32_t	GR1553B IRQ register
IRQForcedFlippedBits	uint32_t	GR1553B IRQ register
IRQReadMask	uint32_t	GR1553B IRQ register
IRQResetMask	uint32_t	GR1553B IRQ register
IRQResetValue	uint32_t	GR1553B IRQ register
IRQWriteMask	uint32_t	GR1553B IRQ register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
RTBSColdResetValue	uint32_t	GR1553B RT bus status bits register
RTBSForcedBits	uint32_t	GR1553B RT bus status bits register
RTBSForcedFlippedBits	uint32_t	GR1553B RT bus status bits register
RTBSReadMask	uint32_t	GR1553B RT bus status bits register

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Name	Type	Description
RTBSResetMask	uint32_t	GR1553B RT bus status bits register
RTBSResetValue	uint32_t	GR1553B RT bus status bits register
RTBSWriteMask	uint32_t	GR1553B RT bus status bits register
RTCColdResetValue	uint32_t	GR1553B RT config register
RTCForcedBits	uint32_t	GR1553B RT config register
RTCForcedFlippedBits	uint32_t	GR1553B RT config register
RTCReadMask	uint32_t	GR1553B RT config register
RTCResetMask	uint32_t	GR1553B RT config register
RTCResetValue	uint32_t	GR1553B RT config register
RTCWriteMask	uint32_t	GR1553B RT config register
RTELIPColdResetValue	uint32_t	GR1553B RT event log interrupt position register
RTELIPForcedBits	uint32_t	GR1553B RT event log interrupt position register
RTELIPForcedFlippedBits	uint32_t	GR1553B RT event log interrupt position register
RTELIPReadMask	uint32_t	GR1553B RT event log interrupt position register
RTELIPResetMask	uint32_t	GR1553B RT event log interrupt position register
RTELIPResetValue	uint32_t	GR1553B RT event log interrupt position register
RTELIPWriteMask	uint32_t	GR1553B RT event log interrupt position register
RTELMColdResetValue	uint32_t	GR1553B RT event log size mask register
RTELMForcedBits	uint32_t	GR1553B RT event log size mask register
RTELMForcedFlippedBits	uint32_t	GR1553B RT event log size mask register
RTELMReadMask	uint32_t	GR1553B RT event log size mask register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
RTELMResetMask	uint32_t	GR1553B RT event log size mask register
RTELMResetValue	uint32_t	GR1553B RT event log size mask register
RTELMWriteMask	uint32_t	GR1553B RT event log size mask register
RTELPColdResetValue	uint32_t	GR1553B RT event log position register
RTELPForcedBits	uint32_t	GR1553B RT event log position register
RTELPForcedFlippedBits	uint32_t	GR1553B RT event log position register
RTELPReadMask	uint32_t	GR1553B RT event log position register
RTELPResetMask	uint32_t	GR1553B RT event log position register
RTELPResetValue	uint32_t	GR1553B RT event log position register
RTELPWriteMask	uint32_t	GR1553B RT event log position register
RTMCCColdResetValue	uint32_t	GR1553B RT mode code control register
RTMCCForcedBits	uint32_t	GR1553B RT mode code control register
RTMCCForcedFlippedBits	uint32_t	GR1553B RT mode code control register
RTMCCReadMask	uint32_t	GR1553B RT mode code control register
RTMCCResetMask	uint32_t	GR1553B RT mode code control register
RTMCCResetValue	uint32_t	GR1553B RT mode code control register
RTMCCWriteMask	uint32_t	GR1553B RT mode code control register
RTSColdResetValue	uint32_t	GR1553B RT status register
RTSForcedBits	uint32_t	GR1553B RT status register
RTSForcedFlippedBits	uint32_t	GR1553B RT status register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
RTSReadMask	uint32_t	GR1553B RT status register
RTSResetMask	uint32_t	GR1553B RT status register
RTSResetValue	uint32_t	GR1553B RT status register
RTSTBAColdResetValue	uint32_t	GR1553B RT subaddress table base address register
RTSTBAForcedBits	uint32_t	GR1553B RT subaddress table base address register
RTSTBAForcedFlippedBits	uint32_t	GR1553B RT subaddress table base address register
RTSTBAReadMask	uint32_t	GR1553B RT subaddress table base address register
RTSTBAResetMask	uint32_t	GR1553B RT subaddress table base address register
RTSTBAResetValue	uint32_t	GR1553B RT subaddress table base address register
RTSTBAWriteMask	uint32_t	GR1553B RT subaddress table base address register
RTSWColdResetValue	uint32_t	GR1553B RT status words register
RTSWForcedBits	uint32_t	GR1553B RT status words register
RTSWForcedFlippedBits	uint32_t	GR1553B RT status words register
RTSWReadMask	uint32_t	GR1553B RT status words register
RTSWResetMask	uint32_t	GR1553B RT status words register
RTSWResetValue	uint32_t	GR1553B RT status words register
RTSWWriteMask	uint32_t	GR1553B RT status words register
RTSWriteMask	uint32_t	GR1553B RT status register
RTSYColdResetValue	uint32_t	GR1553B RT sync register
RTSYForcedBits	uint32_t	GR1553B RT sync register
RTSYForcedFlippedBits	uint32_t	GR1553B RT sync register
RTSYReadMask	uint32_t	GR1553B RT sync register

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Name	Type	Description
RTSYResetMask	uint32_t	GR1553B RT sync register
RTSYResetValue	uint32_t	GR1553B RT sync register
RTSYWriteMask	uint32_t	GR1553B RT sync register
RTTTCColdResetValue	uint32_t	GR1553B RT time tag control register
RTTTCForcedBits	uint32_t	GR1553B RT time tag control register
RTTTCForcedFlippedBits	uint32_t	GR1553B RT time tag control register
RTTTCReadMask	uint32_t	GR1553B RT time tag control register
RTTTCResetMask	uint32_t	GR1553B RT time tag control register
RTTTCResetValue	uint32_t	GR1553B RT time tag control register
RTTTCWriteMask	uint32_t	GR1553B RT time tag control register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
bus	temu_IfaceRef/ <unknown>	MIL-STD-1553 bus model.
config.infiniteSpeed	uint8_t	0 = milbus speed, 1+ = infinite speed
config.interrupt	uint8_t	The interrupt index
config.littleEndian	uint8_t	Endianess of memory interface.
internal.bc.busState	uint32_t	
internal.bc.tldesc.w0	uint32_t	
internal.bc.tldesc.w1	uint32_t	
internal.bc.tldesc.w2	uint32_t	
internal.bc.tldesc.w3	uint32_t	
internal.bc.tldescAddr	uint32_t	
internal.rt.Cmd	uint16_t	
internal.rt.CmdMcActivation	uint32_t	
internal.rt.CmdType	uint32_t	

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
internal.rt.State	uint32_t	
internal.rt.inhibitTerminalFlag	uint8_t	
internal.rt.previousCommand	uint16_t	
internal.rt.previousStatusWord	uint16_t	
internal.rt.statusFlags	uint16_t	
internal.rt.subAddrTableEntry.ctrlWord	uint32_t	
internal.rt.subAddrTableEntry.receiveDescPtr	uint32_t	
internal.rt.subAddrTableEntry.transmitDescPtr	uint32_t	
internal.rt.timeTagSetTime	uint64_t	
internal.rt.timeTagSetValue	uint16_t	
irqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller.
memAccess	temu_IfaceRef/ <unknown>	Memory access interface for accessing RAM (for DMA).
pnp.bar	uint32_t	
pnp.config	uint32_t	
regs.bc.action	uint32_t	GR1553B BC action register
regs.bc.asyncListCurrentSlot	uint32_t	GR1553B BC asynchronous list current slot pointer
regs.bc.asyncListNextPtr	uint32_t	GR1553B BC asynchronous list next pointer register
regs.bc.perRtBusSwap	uint32_t	GR1553B BC per-RT bus swap register
regs.bc.statCfg	uint32_t	GR1553B BC status and config register
regs.bc.timer	uint32_t	GR1553B BC timer register
regs.bc.timerWakeup	uint32_t	GR1553B BC timer wake-up register
regs.bc.transListCurrentSlot	uint32_t	GR1553B BC transfer list current slot pointer
regs.bc.transferListNextPtr	uint32_t	GR1553B BC transfer list next pointer register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
regs.bc.trigIrqRingPos	uint32_t	GR1553B BC transfer-triggered IRQ ring position register
regs.bm.ctrl	uint32_t	GR1553B BM control register
regs.bm.logBuffEnd	uint32_t	GR1553B BM log buffer end register
regs.bm.logBuffPos	uint32_t	GR1553B BM log buffer position register
regs.bm.logBuffStart	uint32_t	GR1553B BM log buffer start register
regs.bm.rtAddrFilt	uint32_t	GR1553B BM RT address filter register
regs.bm.rtMcFilt	uint32_t	GR1553B BM RT mode code filter register
regs.bm.rtSubAddrFilt	uint32_t	GR1553B BM RT subaddress filter register
regs.bm.stat	uint32_t	GR1553B BM status register
regs.bm.timeTagCtrl	uint32_t	GR1553B BM time tag control register
regs.hwConfig	uint32_t	GR1553B hardware configuration register
regs.irq	uint32_t	GR1553B IRQ register
regs.irqEnable	uint32_t	GR1553B IRQ enable register
regs.rt.busStatBits	uint32_t	GR1553B RT bus status bits register
regs.rt.cfg	uint32_t	GR1553B RT config register
regs.rt.eventLogIrqPos	uint32_t	GR1553B RT event log interrupt position register
regs.rt.eventLogPos	uint32_t	GR1553B RT event log position register
regs.rt.eventLogSizeMask	uint32_t	GR1553B RT event log size mask register
regs.rt.modeCodeCtrl	uint32_t	GR1553B RT mode code control register
regs.rt.statWord	uint32_t	GR1553B RT status words register
regs.rt.status	uint32_t	GR1553B RT status register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
regs.rt.subAddrTableBaseAddr	uint32_t	GR1553B RT subaddress table base address register
regs.rt.sync	uint32_t	GR1553B RT sync register
regs.rt.timeTagCtrl	uint32_t	GR1553B RT time tag control register

Interfaces

Name	Type	Description
ApbIface	ApbIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
Mil1553DevIface	Mil1553DevIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Commands

Name	Description
delete	Dispose instance of Gr1553B

9.15.5. Limitations

9.16. GRCLKGATE

The GRCLKGATE device is part of the GRLIB IP library. It is available in `libTEMUGrClkgate.so`.

9.16.1. Loading the Plugin

```
import GrClkgate
```

9.16.2. Configuration

9.16.3. @GRCLKGATE Reference

Properties

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GRCLKGATE
new	Create new instance of GRCLKGATE

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.16.4. GRCLKGATE Reference

Properties

Name	Type	Description
CLKENColdResetValue	uint32_t	Clock enable register
CLKENForcedBits	uint32_t	Clock enable register
CLKENForcedFlippedBits	uint32_t	Clock enable register
CLKENReadMask	uint32_t	Clock enable register
CLKENResetMask	uint32_t	Clock enable register
CLKENResetValue	uint32_t	Clock enable register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
CLKENWriteMask	uint32_t	Clock enable register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
OVERRIDEColdResetValue	uint32_t	CPU/FPU override register
OVERRIDEForcedBits	uint32_t	CPU/FPU override register
OVERRIDEForcedFlippedBits	uint32_t	CPU/FPU override register
OVERRIDEReadMask	uint32_t	CPU/FPU override register
OVERRIDEResetMask	uint32_t	CPU/FPU override register
OVERRIDEResetValue	uint32_t	CPU/FPU override register
OVERRIDEWriteMask	uint32_t	CPU/FPU override register
ObjectID	uint64_t	Unique ObjectID.
RESETColdResetValue	uint32_t	Reset register
RESETForcedBits	uint32_t	Reset register
RESETForcedFlippedBits	uint32_t	Reset register
RESETReadMask	uint32_t	Reset register
RESETResetMask	uint32_t	Reset register
RESETResetValue	uint32_t	Reset register
RESETWriteMask	uint32_t	Reset register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
UNLOCKColdResetValue	uint32_t	Clock unlock register
UNLOCKForcedBits	uint32_t	Clock unlock register
UNLOCKForcedFlippedBits	uint32_t	Clock unlock register
UNLOCKReadMask	uint32_t	Clock unlock register
UNLOCKResetMask	uint32_t	Clock unlock register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
UNLOCKResetValue	uint32_t	Clock unlock register
UNLOCKWriteMask	uint32_t	Clock unlock register
apb.pnp.bar	uint32_t	
apb.pnp.config	uint32_t	
clockEnableReg	uint32_t	Clock enable register
config.littleEndian	uint8_t	Endianess of memory interface.
coreResetReg	uint32_t	Reset register
overrideReg	uint32_t	CPU/FPU override register
unlockReg	uint32_t	Clock unlock register

Interfaces

Name	Type	Description
ApbIface	ApbIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Commands

Name	Description
delete	Dispose instance of GRCLKGATE

9.16.5. Limitations

The GRCLKGATE model is a non functional model.

The main purpose of the device is to save power by cutting off the clock to devices, and power consumption is not modelled in TEMU.

9.17. GRGPRBANK

The GRGPRBANK device is part of the GRLIB IP library. It is available in `libTEMUGRGPRBANK.so`.

9.17.1. Loading the Plugin

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

```
import GRGPRBANK
```

9.17.2. Configuration

9.17.3. @GRGPRBANK Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GRGPRBANK
new	Create new instance of GRGPRBANK

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.17.4. GRGPRBANK Reference

Properties

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
GPREG	[uint32_t; 64]	General purpose register
GPREG_MASK	[uint32_t; 64]	General purpose register mask
GPREG_RESET	[uint32_t; 64]	General purpose register reset value
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
config.littleEndian	uint8_t	Endianess of memory interface.
pnp.bar	uint32_t	AMBA plug and play base address register
pnp.config	uint32_t	AMBA plug and play config word

Interfaces

Name	Type	Description
ApbIface	ApbIface	AMBA plug and play interface.
DeviceIface	DeviceIface	Device interface.
MemAccessIface	MemAccessIface	Memory access interface.
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	Reset interface.

Registers



Register support is currently experimental!

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register Bank Regs

Register GPREG

Description

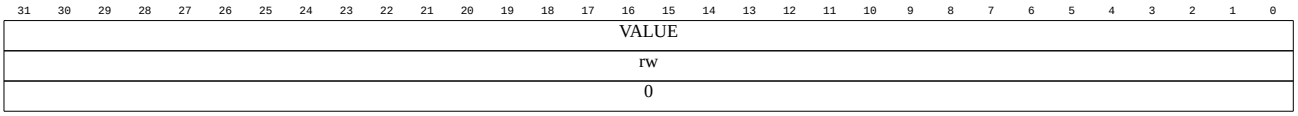
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

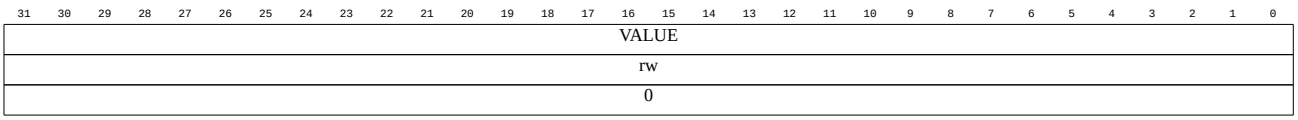
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

General purpose register

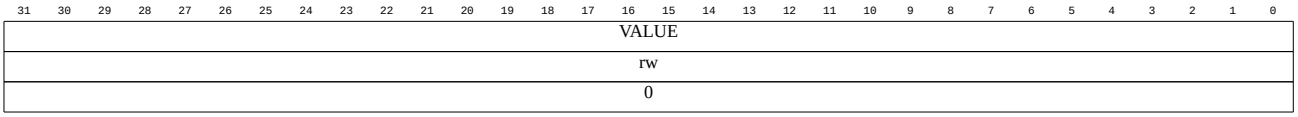
Reset value

0x00000000

Warm reset mask

0xffffffff

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Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

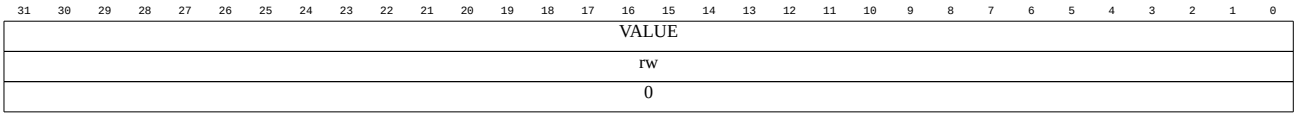
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

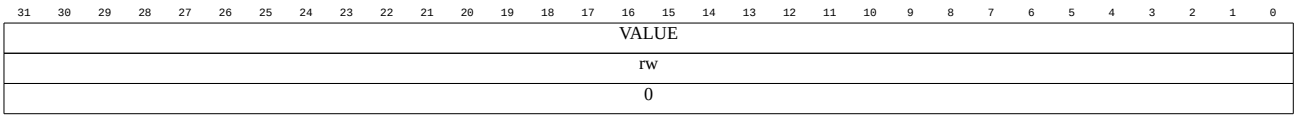
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

General purpose register

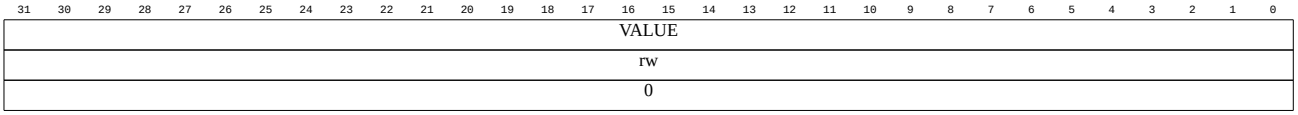
The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
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Description

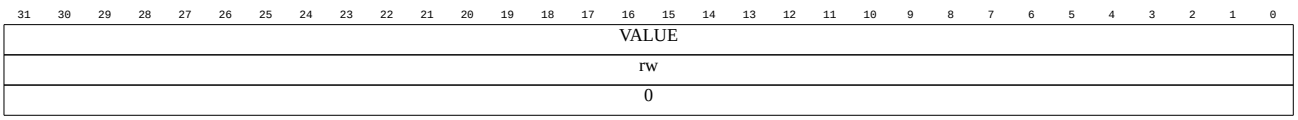
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

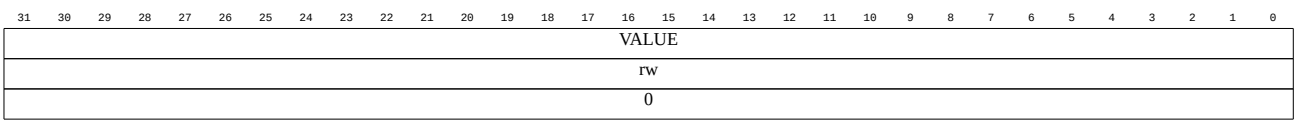
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



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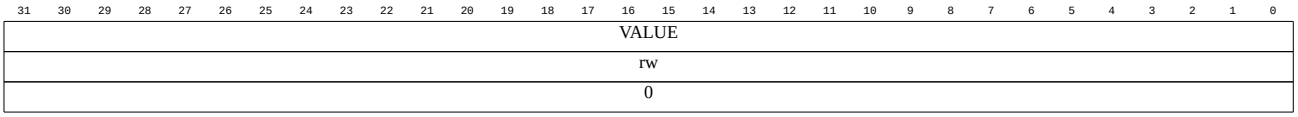
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

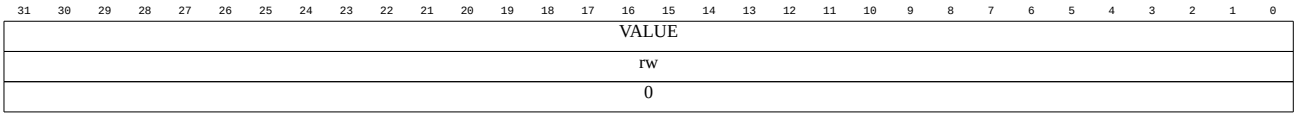
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

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General purpose register

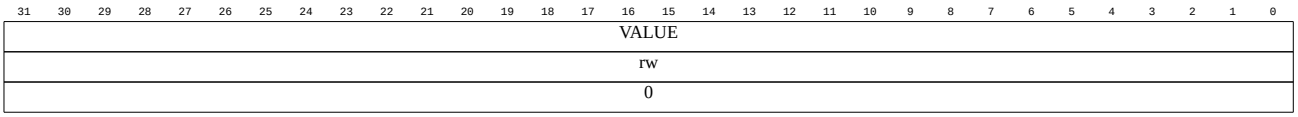
Reset value

0x00000000

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Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

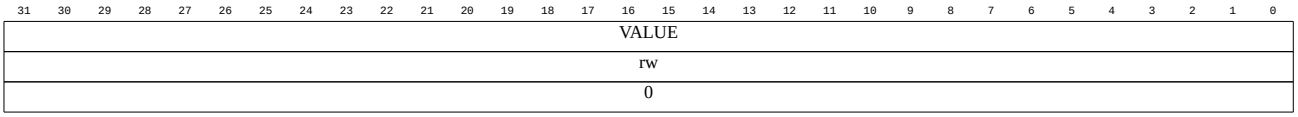
General purpose register

Reset value

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Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

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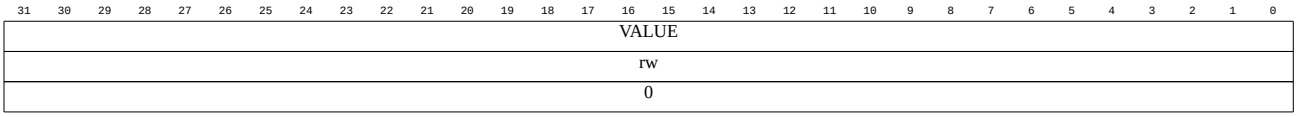
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

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Description

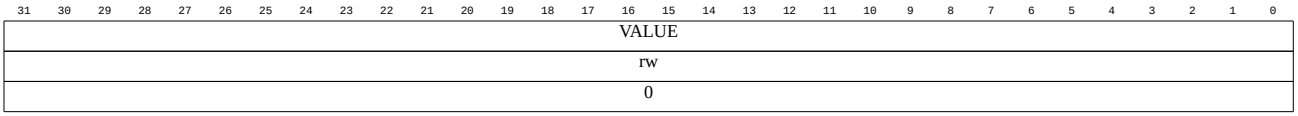
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

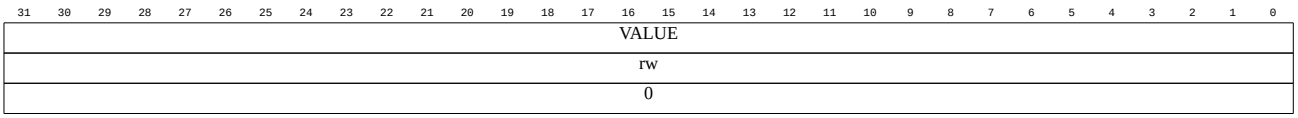
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

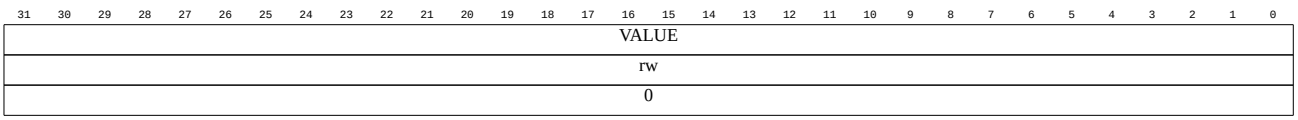
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



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VALUE	0xffffffff	0x0	General purpose register value

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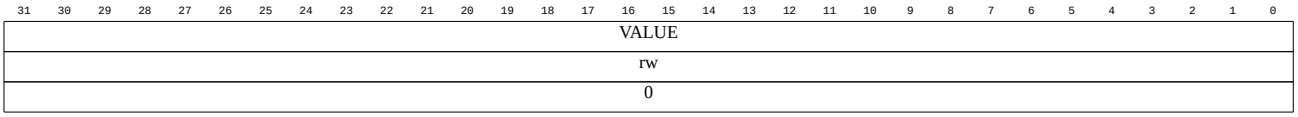
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

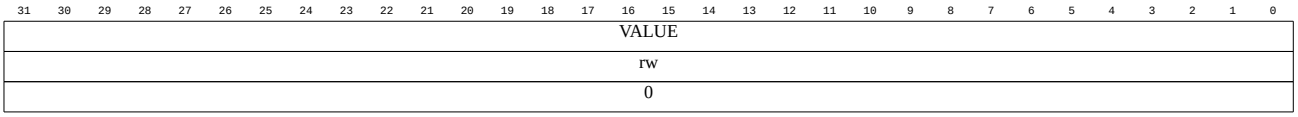
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

General purpose register

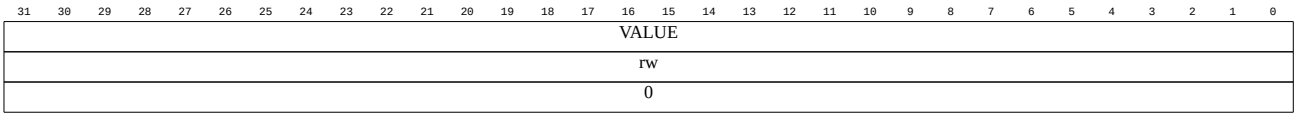
Reset value

0x00000000

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Warm reset mask

0xffffffff



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
rw																															
0																															

Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

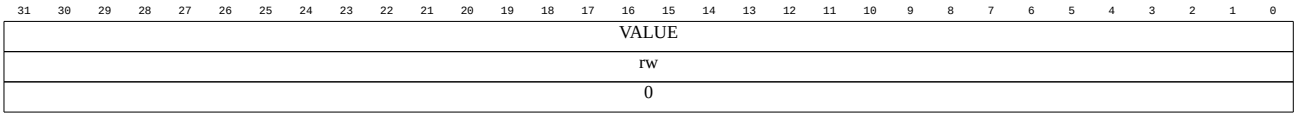
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
rw																															
0																															

Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

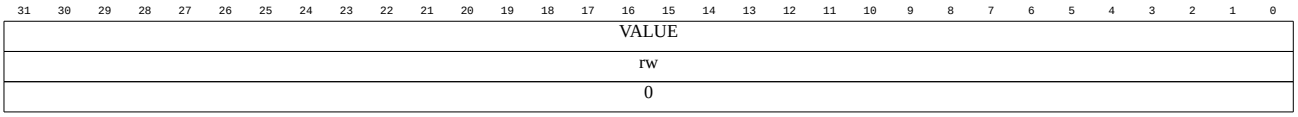
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
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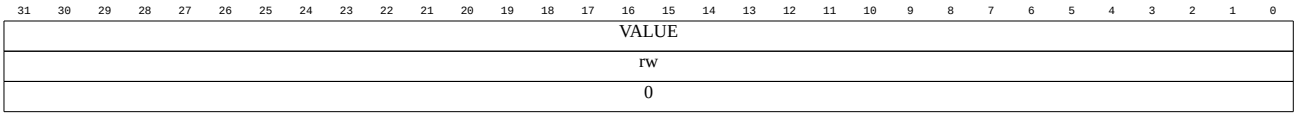
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

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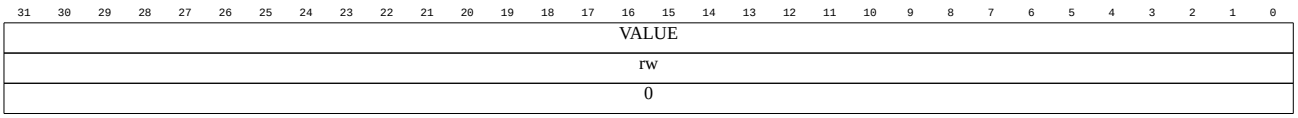
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
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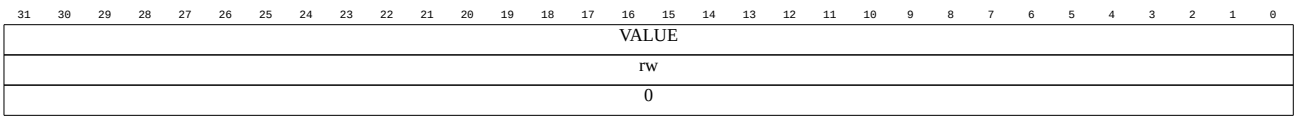
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



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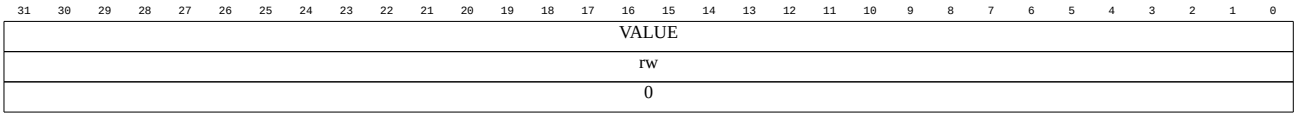
General purpose register

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Warm reset mask

0xffffffff



Field	Mask	Reset	Description
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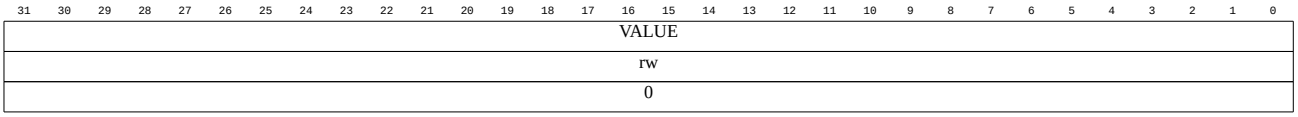
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

General purpose register

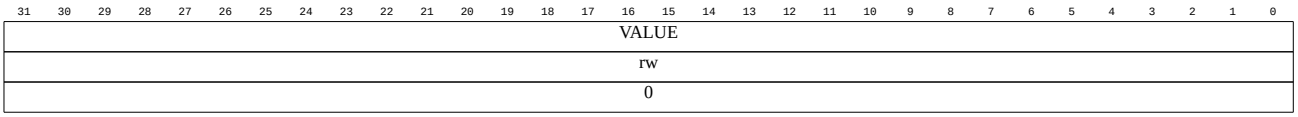
Reset value

0x00000000

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Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

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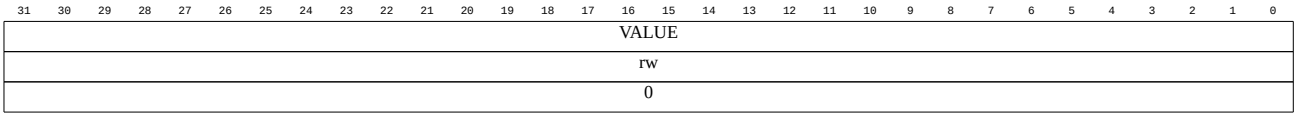
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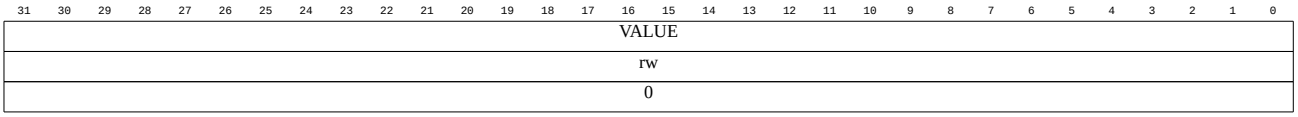
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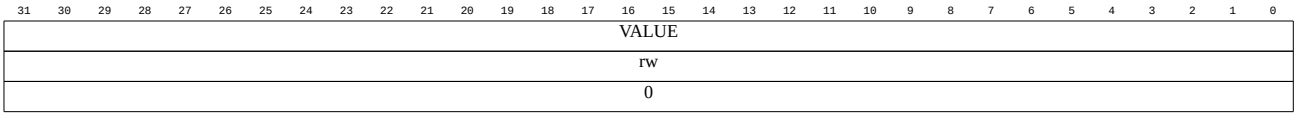
General purpose register

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Warm reset mask

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Field	Mask	Reset	Description
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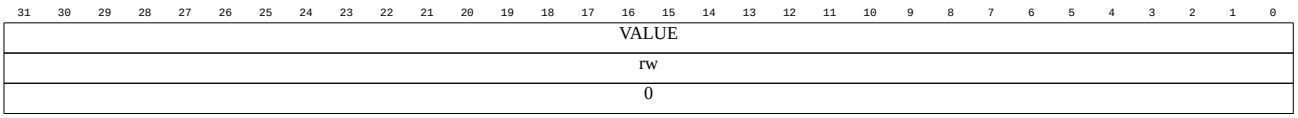
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Field	Mask	Reset	Description
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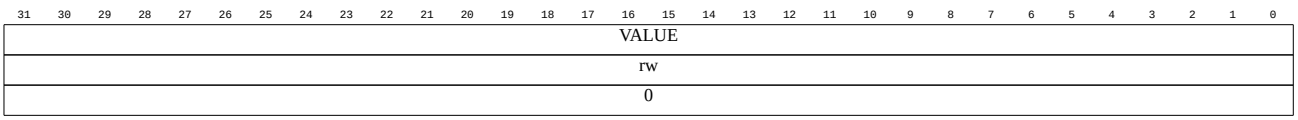
General purpose register

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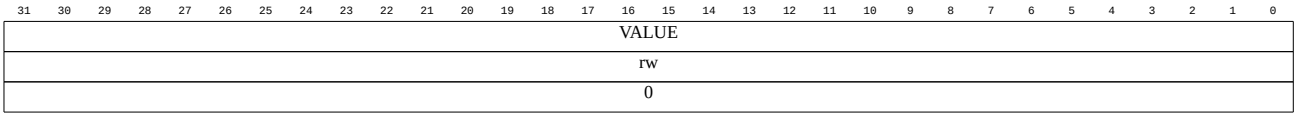
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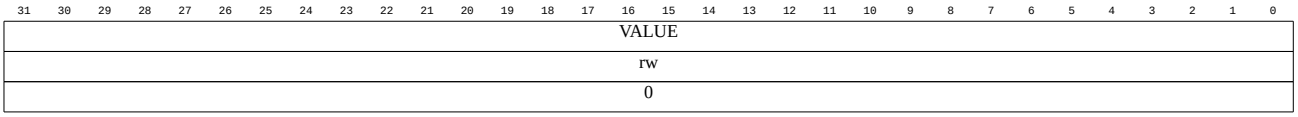
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Register GPREG

Description

General purpose register

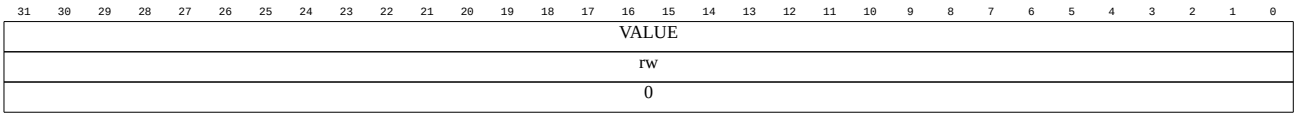
Reset value

0x00000000

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Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

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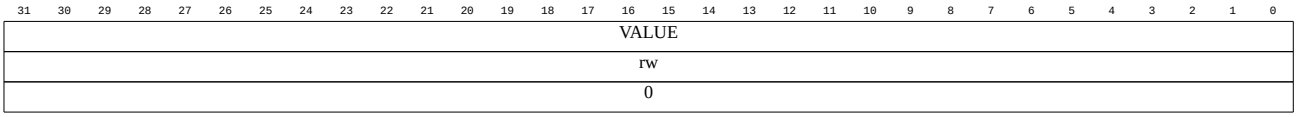
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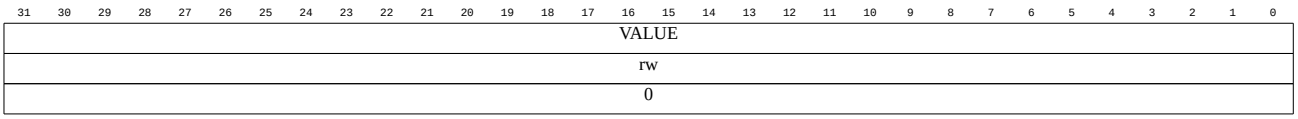
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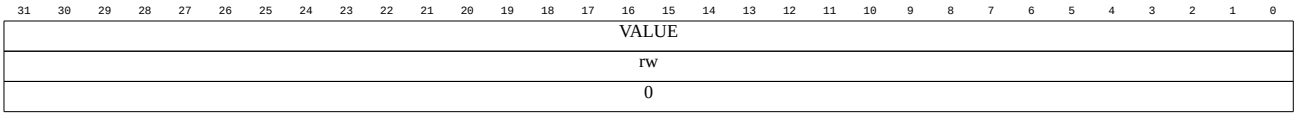
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Register GPREG

Description

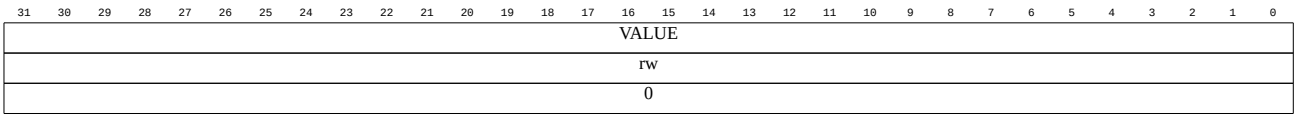
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

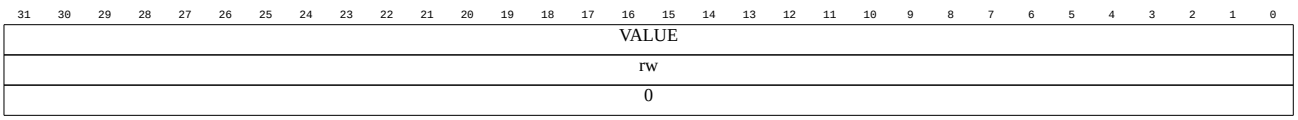
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



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Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

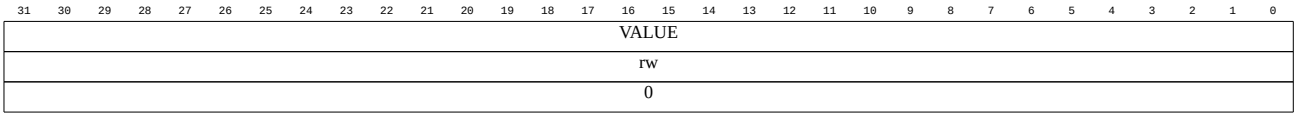
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

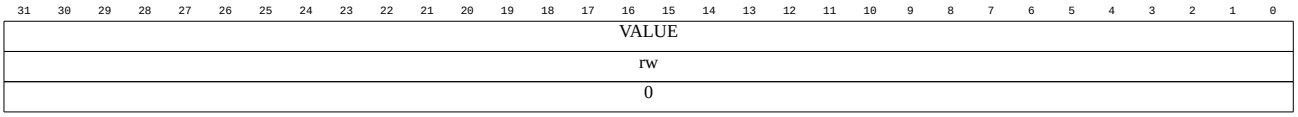
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

General purpose register

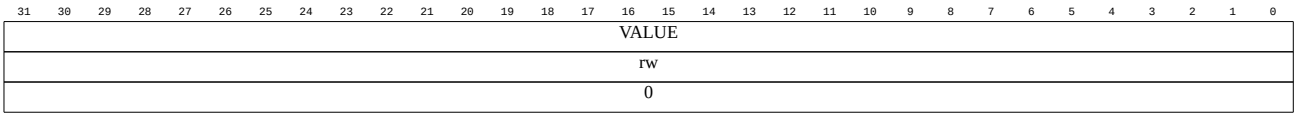
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

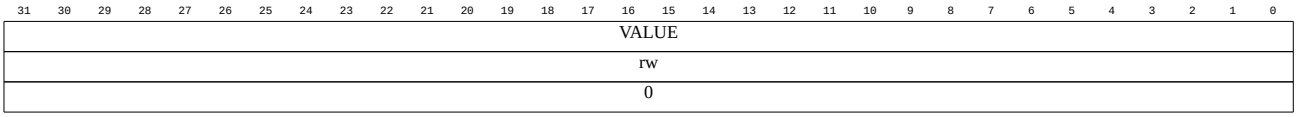
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

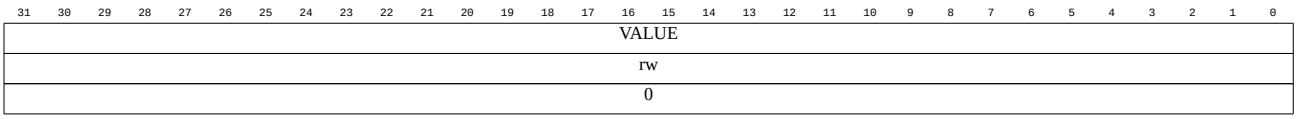
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

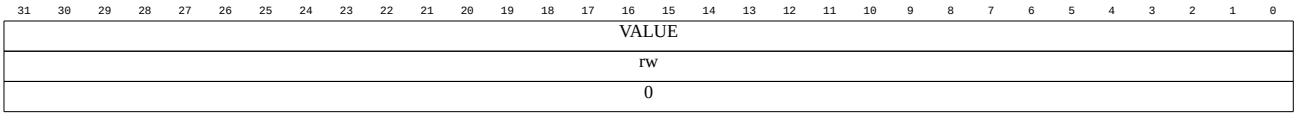
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

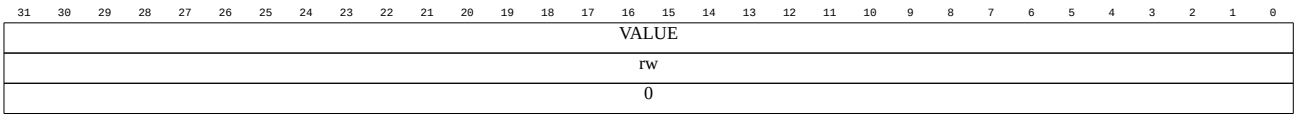
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

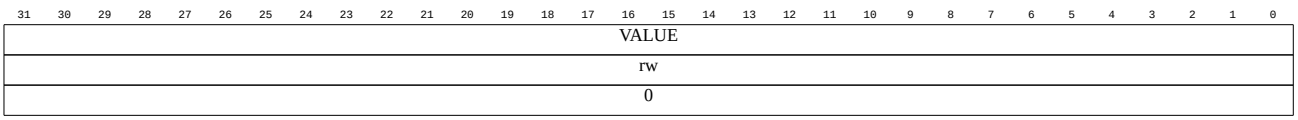
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



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Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

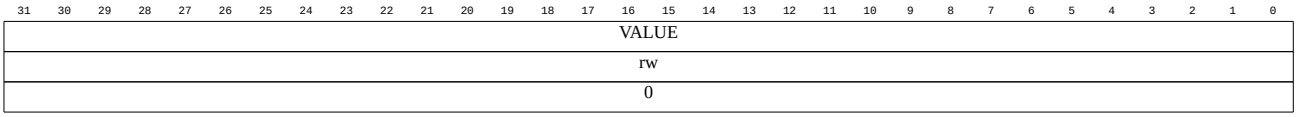
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

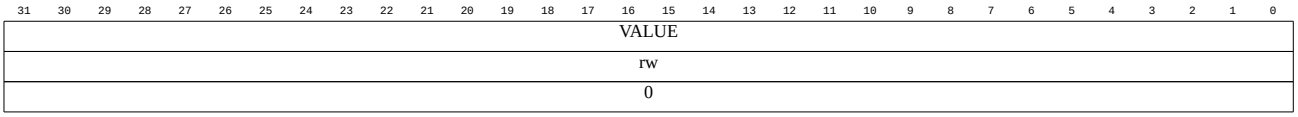
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

General purpose register

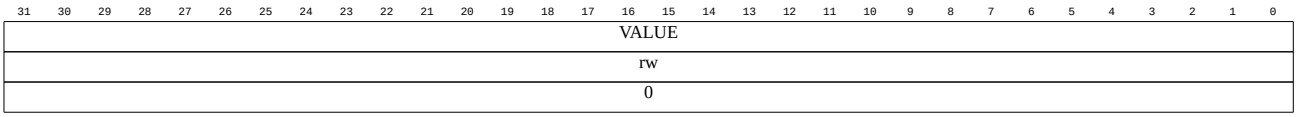
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
rw																															
0																															

Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

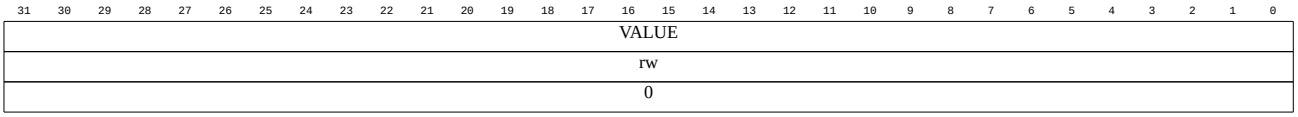
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
rw																															
0																															

Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

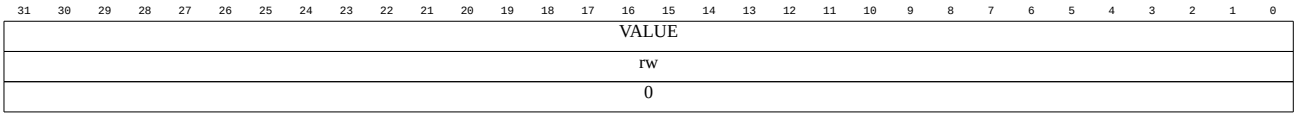
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
rw																															
0																															

Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

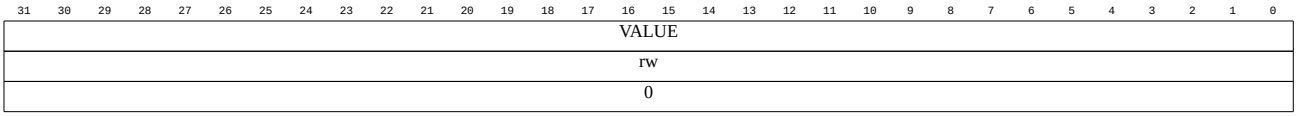
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

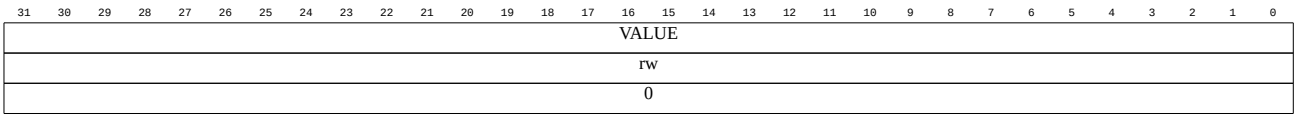
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

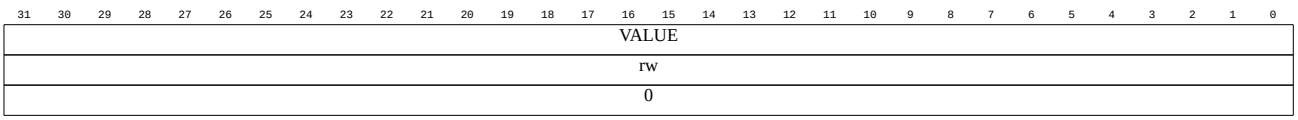
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



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Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

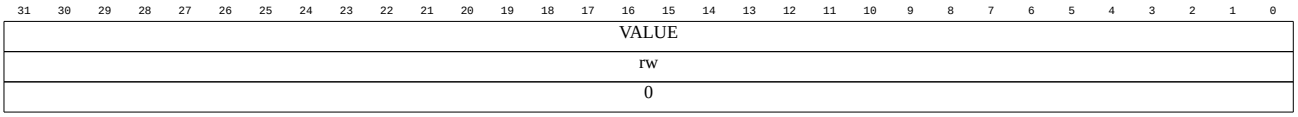
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

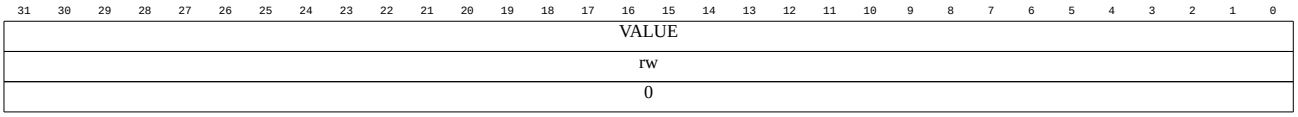
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

General purpose register

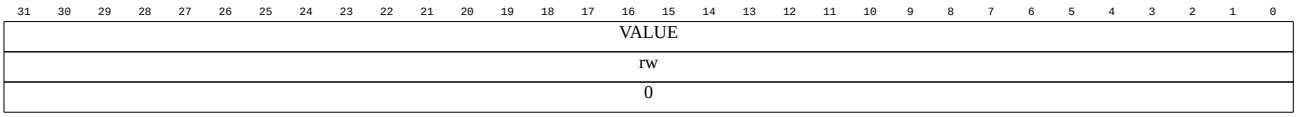
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

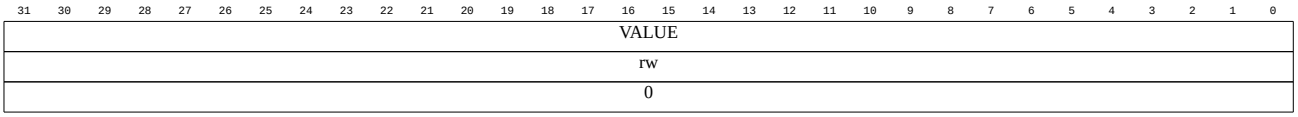
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

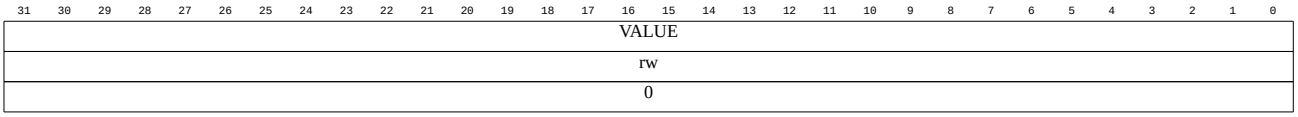
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

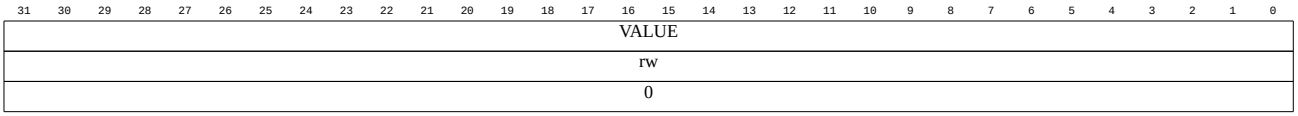
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

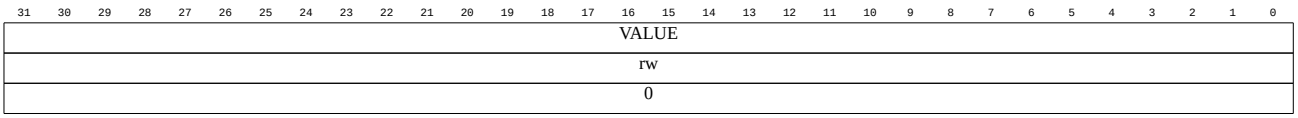
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Register GPREG

Description

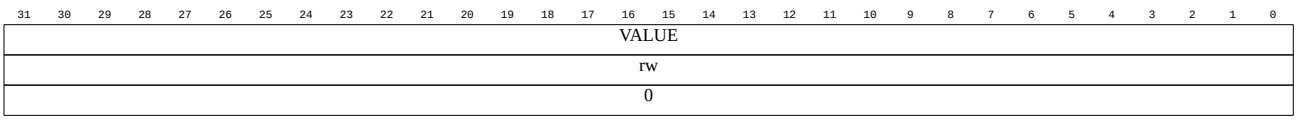
General purpose register

Reset value

0x00000000

Warm reset mask

0xffffffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
VALUE	0xffffffff	0x0	General purpose register value

Commands

Name	Description
delete	Dispose instance of GRGPRBANK

9.17.5. Limitations

9.18. GRGPREG

The GRGPREG device is part of the GRLIB IP library. It is available in `libTEMUGRGPREG.so`.

9.18.1. Loading the Plugin

```
import GRGPREG
```

9.18.2. Configuration

9.18.3. @GRGPREG Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Description
delete	Dispose instance of @GRGPREG
new	Create new instance of GRGPREG

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.18.4. GRGPREG Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
GPREG	[uint32_t; 2]	General purpose register bits 31:0
GPREG_MASK	[uint32_t; 2]	General purpose register mask
GPREG_RESET	[uint32_t; 2]	General purpose register reset value
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
config.littleEndian	uint8_t	Endianess of memory interface.
pnp.bar	uint32_t	AMBA plug and play base address register
pnp.config	uint32_t	AMBA plug and play config word

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Interfaces

Name	Type	Description
ApbIface	ApbIface	AMBA plug and play interface.
DeviceIface	DeviceIface	Device interface.
MemAccessIface	MemAccessIface	Memory access interface.
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	Reset interface.

Registers



Register support is currently experimental!

Register Bank Regs

Register GPREG

Description

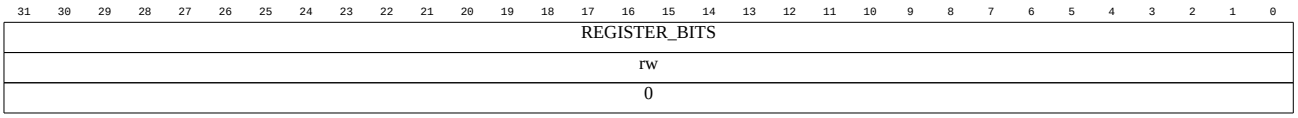
General purpose register bits 31:0

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
REGISTER_BITS	0xffffffff	0x0	General purpose register bits

Register GPREG

Description

General purpose register bits 63:32

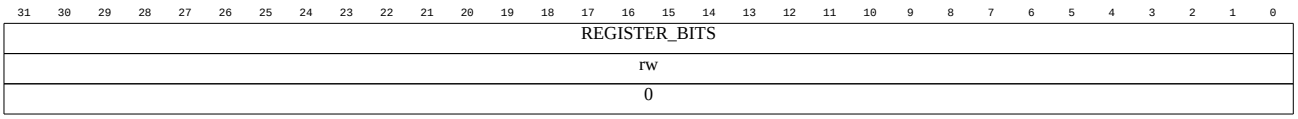
Reset value

0x00000000

Warm reset mask

0xffffffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.



Field	Mask	Reset	Description
REGISTER_BITS	0xffffffff	0x0	General purpose register bits

Commands

Name	Description
delete	Dispose instance of GRGPREG

9.18.5. Limitations

9.19. GRSPWROUTER

The GrSpwRouter device is part of the GRLIB IP library. It is available in `libTEMUGrSpwRouter.so`.

9.19.1. Loading the Plugin

```
import GrSpwRouter
```

9.19.2. Configuration

9.19.3. @GrSpwRouter Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GrSpwRouter
new	Create new instance of GrSpwRouter

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.19.4. GrSpwRouter Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
ambaPort0.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort0.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort0.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ambaPort0config.baseAddr	uint32_t	Base address
ambaPort0config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort0config.interrupt	uint8_t	Interrupt number
ambaPort0config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort0config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort0config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort0config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort0config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort0config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort0config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort0internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort0internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort0internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort0internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort0internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort0internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort0internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort0internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort0internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort0internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ambaPort0internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort0internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort0internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort0internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort0internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort0internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort0internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort0regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort0regs.destKey	uint32_t	Amba port destination key registers
ambaPort0regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort0regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort0regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort0regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort0regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort0regs.portCtrl	uint32_t	Amba ports control registers
ambaPort0regs.portStatus	uint32_t	Amba port status registers
ambaPort0regs.time	uint32_t	Amba port time registers
ambaPort1.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort1.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs

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Name	Type	Description
ambaPort1.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort10.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort10.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort10.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort10config.baseAddr	uint32_t	Base address
ambaPort10config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort10config.interrupt	uint8_t	Interrupt number
ambaPort10config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort10config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort10config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort10config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort10config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort10config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort10config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort10internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort10internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort10internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort10internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort10internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort10internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0

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Name	Type	Description
ambaPort10internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort10internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort10internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort10internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort10internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort10internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort10internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort10internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort10internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort10internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort10internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort10regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort10regs.destKey	uint32_t	Amba port destination key registers
ambaPort10regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort10regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort10regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort10regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers

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Name	Type	Description
ambaPort10regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort10regs.portCtrl	uint32_t	Amba ports control registers
ambaPort10regs.portStatus	uint32_t	Amba port status registers
ambaPort10regs.time	uint32_t	Amba port time registers
ambaPort11.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort11.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort11.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort11config.baseAddr	uint32_t	Base address
ambaPort11config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort11config.interrupt	uint8_t	Interrupt number
ambaPort11config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort11config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort11config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort11config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort11config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort11config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort11config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort11internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort11internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort11internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor

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Name	Type	Description
ambaPort11internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort11internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort11internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort11internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort11internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort11internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort11internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort11internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort11internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort11internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort11internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort11internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort11internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort11internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort11regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort11regs.destKey	uint32_t	Amba port destination key registers
ambaPort11regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort11regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers

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Name	Type	Description
ambaPort11regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort11regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort11regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort11regs.portCtrl	uint32_t	Amba ports control registers
ambaPort11regs.portStatus	uint32_t	Amba port status registers
ambaPort11regs.time	uint32_t	Amba port time registers
ambaPort12.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort12.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort12.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort12config.baseAddr	uint32_t	Base address
ambaPort12config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort12config.interrupt	uint8_t	Interrupt number
ambaPort12config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort12config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort12config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort12config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort12config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort12config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort12config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort12internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported

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Name	Type	Description
ambaPort12internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort12internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort12internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort12internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort12internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort12internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort12internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort12internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort12internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort12internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort12internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort12internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort12internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort12internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort12internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort12internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort12regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort12regs.destKey	uint32_t	Amba port destination key registers

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Name	Type	Description
ambaPort12regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort12regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort12regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort12regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort12regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort12regs.portCtrl	uint32_t	Amba ports control registers
ambaPort12regs.portStatus	uint32_t	Amba port status registers
ambaPort12regs.time	uint32_t	Amba port time registers
ambaPort13.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort13.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort13.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort13config.baseAddr	uint32_t	Base address
ambaPort13config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort13config.interrupt	uint8_t	Interrupt number
ambaPort13config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort13config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort13config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort13config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort13config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort13config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check

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Name	Type	Description
ambaPort13config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort13internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort13internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort13internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort13internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort13internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort13internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort13internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort13internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort13internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort13internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort13internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort13internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort13internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort13internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort13internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort13internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer

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Name	Type	Description
ambaPort13internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort13regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort13regs.destKey	uint32_t	Amba port destination key registers
ambaPort13regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort13regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort13regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort13regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort13regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort13regs.portCtrl	uint32_t	Amba ports control registers
ambaPort13regs.portStatus	uint32_t	Amba port status registers
ambaPort13regs.time	uint32_t	Amba port time registers
ambaPort14.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort14.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort14.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort14config.baseAddr	uint32_t	Base address
ambaPort14config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort14config.interrupt	uint8_t	Interrupt number
ambaPort14config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort14config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort14config.logTxHeader	uint8_t	Log Packet transmitted from port

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Name	Type	Description
ambaPort14config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort14config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort14config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort14config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort14internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort14internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort14internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort14internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort14internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort14internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort14internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort14internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort14internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort14internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort14internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort14internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort14internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort14internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer

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Name	Type	Description
ambaPort14internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort14internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort14internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort14regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort14regs.destKey	uint32_t	Amba port destination key registers
ambaPort14regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort14regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort14regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort14regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort14regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort14regs.portCtrl	uint32_t	Amba ports control registers
ambaPort14regs.portStatus	uint32_t	Amba port status registers
ambaPort14regs.time	uint32_t	Amba port time registers
ambaPort15.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort15.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort15.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort15config.baseAddr	uint32_t	Base address
ambaPort15config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort15config.interrupt	uint8_t	Interrupt number
ambaPort15config.logRxHeader	uint8_t	Log Packet received by the port

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Name	Type	Description
ambaPort15config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort15config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort15config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort15config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort15config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort15config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort15internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort15internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort15internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort15internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort15internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort15internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort15internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort15internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort15internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort15internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort15internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort15internal.txBusy	uint8_t	Set while a transmission is claimed by this port

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Name	Type	Description
ambaPort15internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort15internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort15internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort15internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort15internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort15regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort15regs.destKey	uint32_t	Amba port destination key registers
ambaPort15regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort15regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort15regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort15regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort15regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort15regs.portCtrl	uint32_t	Amba ports control registers
ambaPort15regs.portStatus	uint32_t	Amba port status registers
ambaPort15regs.time	uint32_t	Amba port time registers
ambaPort1config.baseAddr	uint32_t	Base address
ambaPort1config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort1config.interrupt	uint8_t	Interrupt number
ambaPort1config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort1config.logRxPkt	uint8_t	Log Packet received by the port

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Name	Type	Description
ambaPort1config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort1config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort1config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort1config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort1config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort1internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort1internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort1internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort1internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort1internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort1internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort1internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort1internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort1internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort1internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort1internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort1internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort1internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer

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Name	Type	Description
ambaPort1internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort1internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort1internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort1internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort1regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort1regs.destKey	uint32_t	Amba port destination key registers
ambaPort1regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort1regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort1regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort1regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort1regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort1regs.portCtrl	uint32_t	Amba ports control registers
ambaPort1regs.portStatus	uint32_t	Amba port status registers
ambaPort1regs.time	uint32_t	Amba port time registers
ambaPort2.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort2.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort2.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort2config.baseAddr	uint32_t	Base address
ambaPort2config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort2config.interrupt	uint8_t	Interrupt number

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Name	Type	Description
ambaPort2config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort2config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort2config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort2config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort2config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort2config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort2config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort2internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort2internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort2internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort2internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort2internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort2internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort2internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort2internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort2internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort2internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort2internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort2internal.txBusy	uint8_t	Set while a transmission is claimed by this port

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Name	Type	Description
ambaPort2internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort2internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort2internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort2internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort2internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort2regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort2regs.destKey	uint32_t	Amba port destination key registers
ambaPort2regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort2regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort2regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort2regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort2regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort2regs.portCtrl	uint32_t	Amba ports control registers
ambaPort2regs.portStatus	uint32_t	Amba port status registers
ambaPort2regs.time	uint32_t	Amba port time registers
ambaPort3.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort3.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort3.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort3config.baseAddr	uint32_t	Base address

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Name	Type	Description
ambaPort3config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort3config.interrupt	uint8_t	Interrupt number
ambaPort3config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort3config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort3config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort3config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort3config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort3config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort3config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort3internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort3internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort3internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort3internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort3internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort3internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort3internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort3internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort3internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort3internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission

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Name	Type	Description
ambaPort3internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort3internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort3internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort3internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort3internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort3internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort3internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort3regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort3regs.destKey	uint32_t	Amba port destination key registers
ambaPort3regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort3regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort3regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort3regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort3regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort3regs.portCtrl	uint32_t	Amba ports control registers
ambaPort3regs.portStatus	uint32_t	Amba port status registers
ambaPort3regs.time	uint32_t	Amba port time registers
ambaPort4.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort4.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs

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Name	Type	Description
ambaPort4.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort4config.baseAddr	uint32_t	Base address
ambaPort4config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort4config.interrupt	uint8_t	Interrupt number
ambaPort4config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort4config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort4config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort4config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort4config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort4config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort4config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort4internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort4internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort4internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort4internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort4internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort4internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort4internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort4internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort4internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3

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Name	Type	Description
ambaPort4internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort4internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort4internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort4internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort4internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort4internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort4internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort4internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort4regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort4regs.destKey	uint32_t	Amba port destination key registers
ambaPort4regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort4regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort4regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort4regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort4regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort4regs.portCtrl	uint32_t	Amba ports control registers
ambaPort4regs.portStatus	uint32_t	Amba port status registers
ambaPort4regs.time	uint32_t	Amba port time registers
ambaPort5.internal.txCurrChan	uint8_t	Channel scheduled for transmission

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Name	Type	Description
ambaPort5.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort5.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort5config.baseAddr	uint32_t	Base address
ambaPort5config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort5config.interrupt	uint8_t	Interrupt number
ambaPort5config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort5config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort5config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort5config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort5config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort5config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort5config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort5internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort5internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort5internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort5internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort5internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort5internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort5internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort5internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2

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Name	Type	Description
ambaPort5internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort5internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort5internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort5internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort5internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort5internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort5internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort5internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort5internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort5regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort5regs.destKey	uint32_t	Amba port destination key registers
ambaPort5regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort5regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort5regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort5regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort5regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort5regs.portCtrl	uint32_t	Amba ports control registers
ambaPort5regs.portStatus	uint32_t	Amba port status registers
ambaPort5regs.time	uint32_t	Amba port time registers

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Name	Type	Description
ambaPort6.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort6.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort6.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort6config.baseAddr	uint32_t	Base address
ambaPort6config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort6config.interrupt	uint8_t	Interrupt number
ambaPort6config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort6config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort6config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort6config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort6config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort6config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort6config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort6internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort6internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort6internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort6internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort6internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort6internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort6internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1

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Name	Type	Description
ambaPort6internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort6internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort6internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort6internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort6internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort6internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort6internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort6internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort6internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort6internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort6regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort6regs.destKey	uint32_t	Amba port destination key registers
ambaPort6regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort6regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort6regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort6regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort6regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort6regs.portCtrl	uint32_t	Amba ports control registers

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Name	Type	Description
ambaPort6regs.portStatus	uint32_t	Amba port status registers
ambaPort6regs.time	uint32_t	Amba port time registers
ambaPort7.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort7.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort7.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort7config.baseAddr	uint32_t	Base address
ambaPort7config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort7config.interrupt	uint8_t	Interrupt number
ambaPort7config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort7config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort7config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort7config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort7config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort7config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort7config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort7internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort7internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort7internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort7internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort7internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor

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Name	Type	Description
ambaPort7internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort7internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort7internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort7internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort7internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort7internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort7internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort7internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort7internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort7internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort7internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort7internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort7regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort7regs.destKey	uint32_t	Amba port destination key registers
ambaPort7regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort7regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort7regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort7regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers

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Name	Type	Description
ambaPort7regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort7regs.portCtrl	uint32_t	Amba ports control registers
ambaPort7regs.portStatus	uint32_t	Amba port status registers
ambaPort7regs.time	uint32_t	Amba port time registers
ambaPort8.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort8.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort8.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort8config.baseAddr	uint32_t	Base address
ambaPort8config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort8config.interrupt	uint8_t	Interrupt number
ambaPort8config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort8config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort8config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort8config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort8config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort8config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort8config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort8internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported
ambaPort8internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort8internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor

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Name	Type	Description
ambaPort8internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort8internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort8internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort8internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort8internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort8internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort8internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort8internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort8internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort8internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort8internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort8internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort8internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort8internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort8regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort8regs.destKey	uint32_t	Amba port destination key registers
ambaPort8regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort8regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers

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Name	Type	Description
ambaPort8regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort8regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort8regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort8regs.portCtrl	uint32_t	Amba ports control registers
ambaPort8regs.portStatus	uint32_t	Amba port status registers
ambaPort8regs.time	uint32_t	Amba port time registers
ambaPort9.internal.txCurrChan	uint8_t	Channel scheduled for transmission
ambaPort9.irqCtrl	temu_IfaceRef/ <unknown>	Irq controller used by the amba port to raise IRQs
ambaPort9.memAccess	temu_IfaceRef/ <unknown>	Memory used by the amba port for DMA accesses
ambaPort9config.baseAddr	uint32_t	Base address
ambaPort9config.infiniteSpeed	uint8_t	If 1, the pack will be sent immediately
ambaPort9config.interrupt	uint8_t	Interrupt number
ambaPort9config.logRxHeader	uint8_t	Log Packet received by the port
ambaPort9config.logRxPkt	uint8_t	Log Packet received by the port
ambaPort9config.logTxHeader	uint8_t	Log Packet transmitted from port
ambaPort9config.logTxPkt	uint8_t	Log Packet transmitted from port
ambaPort9config.nsPerByte	uint64_t	Ns it takes to transfer each byte
ambaPort9config.realCrcCheck	uint8_t	If 1, the real CRC value will be calculated and check
ambaPort9config.rxHoldQueueDepth	uint32_t	Packets a DMA channel holds when no-spill is set and no descriptor is available (zero always spills).
ambaPort9internal.ambiguousChanAddrWarned	uint8_t	Ambiguous channel address reported

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Name	Type	Description
ambaPort9internal.heldRxPkt0	temu::list::Buffer	Packets held for DMA channel 0 awaiting a descriptor
ambaPort9internal.heldRxPkt1	temu::list::Buffer	Packets held for DMA channel 1 awaiting a descriptor
ambaPort9internal.heldRxPkt2	temu::list::Buffer	Packets held for DMA channel 2 awaiting a descriptor
ambaPort9internal.heldRxPkt3	temu::list::Buffer	Packets held for DMA channel 3 awaiting a descriptor
ambaPort9internal.heldRxType0	temu::list::U8	Packet type of each entry in heldRxPkt0
ambaPort9internal.heldRxType1	temu::list::U8	Packet type of each entry in heldRxPkt1
ambaPort9internal.heldRxType2	temu::list::U8	Packet type of each entry in heldRxPkt2
ambaPort9internal.heldRxType3	temu::list::U8	Packet type of each entry in heldRxPkt3
ambaPort9internal.rmapOutgoingReplyPkt	temu::list::Buffer	Queue of RMAP reply packets awaiting transmission
ambaPort9internal.tcBusy	uint8_t	Set while a time code transmission is pending
ambaPort9internal.txBusy	uint8_t	Set while a transmission is claimed by this port
ambaPort9internal.txDAddr	uint32_t	Data address for the scheduled dma engine transfer
ambaPort9internal.txDLength	uint32_t	Data length for the scheduled dma engine transfer
ambaPort9internal.txFlags	uint32_t	Flags for the scheduled dma engine transfer
ambaPort9internal.txHAddr	uint32_t	Header address for the scheduled dma engine transfer
ambaPort9internal.txType	uint8_t	Scheduled transmission type (dma engine/rmap)
ambaPort9regs.defaultAddr	uint32_t	Amba port default address registers
ambaPort9regs.destKey	uint32_t	Amba port destination key registers

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Name	Type	Description
ambaPort9regs.dmaChannelAddr	[uint32_t; 4]	Amba port dma channel address registers
ambaPort9regs.dmaCtrl	[uint32_t; 4]	Amba port dma control registers
ambaPort9regs.dmaRxDescTableAddr	[uint32_t; 4]	Amba port dma receive descriptor table address registers
ambaPort9regs.dmaRxMaxLen	[uint32_t; 4]	Amba port dma receive max length registers
ambaPort9regs.dmaTxDescTableAddr	[uint32_t; 4]	Amba port dma transfer descriptor table address registers
ambaPort9regs.portCtrl	uint32_t	Amba ports control registers
ambaPort9regs.portStatus	uint32_t	Amba port status registers
ambaPort9regs.time	uint32_t	Amba port time registers
config.adaptiveRouteToReadyPort	uint8_t	Group adaptive routing picks an AMBA port that can accept the packet and rotates between them, instead of always picking the lowest numbered port
config.ahbCfgBaseAddr	uint32_t	Base address of the AHB configuration port
config.ahbCfgEnabled	uint8_t	Ahb configuration port enabled
config.ambaPortsNum	uint8_t	Number of AMBA ports
config.fifoIf0.bridgesToPort	uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw
amba	fifo)PortsNum.	config.fifoIf0.logPkts
uint8_t	Log packets transmitted or received by this port	config.fifoIf1.bridgesToPort
uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba
fifo)PortsNum.	config.fifoIf1.logPkts	uint8_t

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Name	Type	Description
Log packets transmitted or received by this port	config.fifoIf10.bridgesToPort	uint8_t
FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba	fifo)PortsNum.
config.fifoIf10.logPkts	uint8_t	Log packets transmitted or received by this port
config.fifoIf11.bridgesToPort	uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw
amba	fifo)PortsNum.	config.fifoIf11.logPkts
uint8_t	Log packets transmitted or received by this port	config.fifoIf12.bridgesToPort
uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba
fifo)PortsNum.	config.fifoIf12.logPkts	uint8_t
Log packets transmitted or received by this port	config.fifoIf13.bridgesToPort	uint8_t
FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba	fifo)PortsNum.
config.fifoIf13.logPkts	uint8_t	Log packets transmitted or received by this port
config.fifoIf14.bridgesToPort	uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw
amba	fifo)PortsNum.	config.fifoIf14.logPkts

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Name	Type	Description
uint8_t	Log packets transmitted or received by this port	config.fifoIf15.bridgesToPort
uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba
fifo)PortsNum.	config.fifoIf15.logPkts	uint8_t
Log packets transmitted or received by this port	config.fifoIf16.bridgesToPort	uint8_t
FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba	fifo)PortsNum.
config.fifoIf16.logPkts	uint8_t	Log packets transmitted or received by this port
config.fifoIf17.bridgesToPort	uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw
amba	fifo)PortsNum.	config.fifoIf17.logPkts
uint8_t	Log packets transmitted or received by this port	config.fifoIf18.bridgesToPort
uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba
fifo)PortsNum.	config.fifoIf18.logPkts	uint8_t
Log packets transmitted or received by this port	config.fifoIf19.bridgesToPort	uint8_t
FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba	fifo)PortsNum.

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Name	Type	Description
config.fifoIf19.logPkts	uint8_t	Log packets transmitted or received by this port
config.fifoIf2.bridgesToPort	uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw
amba	fifo)PortsNum.	config.fifoIf2.logPkts
uint8_t	Log packets transmitted or received by this port	config.fifoIf20.bridgesToPort
uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba
fifo)PortsNum.	config.fifoIf20.logPkts	uint8_t
Log packets transmitted or received by this port	config.fifoIf21.bridgesToPort	uint8_t
FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba	fifo)PortsNum.
config.fifoIf21.logPkts	uint8_t	Log packets transmitted or received by this port
config.fifoIf22.bridgesToPort	uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw
amba	fifo)PortsNum.	config.fifoIf22.logPkts
uint8_t	Log packets transmitted or received by this port	config.fifoIf23.bridgesToPort
uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba
fifo)PortsNum.	config.fifoIf23.logPkts	uint8_t

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Name	Type	Description
Log packets transmitted or received by this port	config.fifoIf24.bridgesToPort	uint8_t
FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba	fifo)PortsNum.
config.fifoIf24.logPkts	uint8_t	Log packets transmitted or received by this port
config.fifoIf25.bridgesToPort	uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw
amba	fifo)PortsNum.	config.fifoIf25.logPkts
uint8_t	Log packets transmitted or received by this port	config.fifoIf26.bridgesToPort
uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba
fifo)PortsNum.	config.fifoIf26.logPkts	uint8_t
Log packets transmitted or received by this port	config.fifoIf27.bridgesToPort	uint8_t
FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba	fifo)PortsNum.
config.fifoIf27.logPkts	uint8_t	Log packets transmitted or received by this port
config.fifoIf28.bridgesToPort	uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw
amba	fifo)PortsNum.	config.fifoIf28.logPkts

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Name	Type	Description
uint8_t	Log packets transmitted or received by this port	config.fifoIf29.bridgesToPort
uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba
fifo)PortsNum.	config.fifoIf29.logPkts	uint8_t
Log packets transmitted or received by this port	config.fifoIf3.bridgesToPort	uint8_t
FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba	fifo)PortsNum.
config.fifoIf3.logPkts	uint8_t	Log packets transmitted or received by this port
config.fifoIf30.bridgesToPort	uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw
amba	fifo)PortsNum.	config.fifoIf30.logPkts
uint8_t	Log packets transmitted or received by this port	config.fifoIf4.bridgesToPort
uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba
fifo)PortsNum.	config.fifoIf4.logPkts	uint8_t
Log packets transmitted or received by this port	config.fifoIf5.bridgesToPort	uint8_t
FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba	fifo)PortsNum.

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Name	Type	Description
config.fifoIf5.logPkts	uint8_t	Log packets transmitted or received by this port
config.fifoIf6.bridgesToPort	uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw
amba	fifo)PortsNum.	config.fifoIf6.logPkts
uint8_t	Log packets transmitted or received by this port	config.fifoIf7.bridgesToPort
uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba
fifo)PortsNum.	config.fifoIf7.logPkts	uint8_t
Log packets transmitted or received by this port	config.fifoIf8.bridgesToPort	uint8_t
FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw	amba	fifo)PortsNum.
config.fifoIf8.logPkts	uint8_t	Log packets transmitted or received by this port
config.fifoIf9.bridgesToPort	uint8_t	FIFO bridge mode pair port index of this port. This maps from a FIFO interface index to a port index, so the value to use depends on config.(spw
amba	fifo)PortsNum.	config.fifoIf9.logPkts
uint8_t	Log packets transmitted or received by this port	config.fifoPortsNum
uint8_t	Number of FiFo ports	config.instanceId
uint8_t	Value of Instance-ID field in Version/InstanceId register	config.logDiscards
uint8_t	Report every discarded packet, not just the first of each reason	config.majorVersion

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Name	Type	Description
uint8_t	Value of major version field in Version/InstanceId register	config.minorVersion
uint8_t	Value of minor version field in Version/InstanceId register	config.patch
uint8_t	Value of patch field in Version/InstanceId register	config.spwPortsNum
uint8_t	Number of SpaceWire ports	config.staticRountingEnabled
uint8_t	Static routing enabled (deprecated spelling)	config.staticRoutingEnabled
uint8_t	Static routing enabled	fifoEndpoints
[temu_IfaceRef; 31]/ <unknown>	FIFO ports into this device.	internal.adaptiveRouteCursor
uint8_t	Rotation cursor for group adaptive port selection	internal.ahbConfigPort.pnp.bar
[uint32_t; 4]	Pnp BAR for the AHB configuration port	internal.ahbConfigPort.pnp.ident
uint32_t	Pnp identification region word for the AHB configuration port	internal.ahbConfigPort.pnp.user
[uint32_t; 3]	Pnp user defined words for the AHB configuration port	internal.discardReported
uint32_t	Discard reasons already reported	internal.spwSpwLinkState
[int32_t; 31]	Link state of the SpaceWire port	regs.cfgWriteEnable
uint32_t	Configuration write enable register	regs.incCharCount
[uint32_t; 31]	Incoming character count register	regs.incPktCount
[uint32_t; 31]	Incoming packet count register	regs.initDiv
uint32_t	Initialization divisor register	regs.outCharCount
[uint32_t; 31]	Outgoing character count register	regs.outPktCount
[uint32_t; 31]	Outgoing packet count register	regs.portCtrl
[uint32_t; 32]	Port control registers for ports [0-31]	regs.portCtrl2
[uint32_t; 32]	Port control 2 registers for ports [0-31]	regs.portSetup

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Name	Type	Description
[uint32_t; 255]	Port setup registers for ports [1-31] and logical addresses [32-255]	regs.portStatus
[uint32_t; 32]	Port status registers for ports [0-31]	regs.routerCfgSt
uint32_t	Router configuration/status register	regs.routingTable
[uint32_t; 223]	Routing table entry registers for logical addresses [32-255]	regs.timeCode
uint32_t	Time code register	regs.timerPrescalerReload
uint32_t	Timer prescaler reload register	regs.timerReload
[uint32_t; 32]	Timer reload registers for ports [0-31]	regs.versionInstanceId
uint32_t	Version / Instance Id register	spwPort0.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort0.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort1.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort1.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort10.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort10.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort11.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort11.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort12.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort12.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort13.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort13.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort14.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort14.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort15.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort15.config.logTxPkt

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Name	Type	Description
uint8_t	Log Packet transmitted from port	spwPort16.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort16.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort17.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort17.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort18.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort18.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort19.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort19.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort2.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort2.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort20.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort20.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort21.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort21.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort22.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort22.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort23.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort23.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort24.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort24.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort25.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort25.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort26.config.logRxPkt

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Name	Type	Description
uint8_t	Log Packet received by the port	spwPort26.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort27.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort27.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort28.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort28.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort29.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort29.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort3.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort3.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort30.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort30.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort31.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort31.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort4.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort4.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort5.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort5.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort6.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort6.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort7.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort7.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwPort8.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort8.config.logTxPkt

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Name	Type	Description
uint8_t	Log Packet transmitted from port	spwPort9.config.logRxPkt
uint8_t	Log Packet received by the port	spwPort9.config.logTxPkt
uint8_t	Log Packet transmitted from port	spwUplink

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	Device interface
RegisterIface	temu::RegisterIface	Auto-generated register interface
ResetIface	ResetIface	Reset interface
SpwPortIface	SpwPortIface	SpaceWire ports interfaces
ahbConfigPortAhbIface	AhbIface	AHB configuration port AHB interface
ahbConfigPortMemAccessIf	MemAccessIface	AHB configuration port memory access interface
ambaPortApbIface	ApbIface	Apb interface
ambaPortMemAccessIface	MemAccessIface	Amba port memory access interface
fifoIfaces	SpwPortIface	FIFO ports out of this device.

Commands

Name	Description
delete	Dispose instance of GrSpwRouter

9.19.5. Limitations

9.20. L2CACHE

The GrlibL2Cache device is part of the GRLIB IP library. It is available in `libTEMUGrlibL2Cache.so`.

9.20.1. Loading the Plugin

```
import GrlibL2Cache
```

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9.20.2. Configuration

9.20.3. @GrlibL2Cache Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GrlibL2Cache
new	Create new instance of GrlibL2Cache

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.20.4. GrlibL2Cache Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component

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Name	Type	Description
L2CACCCColdResetValue	uint32_t	L2C Access control register
L2CACCCForcedBits	uint32_t	L2C Access control register
L2CACCCForcedFlippedBits	uint32_t	L2C Access control register
L2CACCCReadMask	uint32_t	L2C Access control register
L2CACCCResetMask	uint32_t	L2C Access control register
L2CACCCResetValue	uint32_t	L2C Access control register
L2CACCCWriteMask	uint32_t	L2C Access control register
L2CCBColdResetValue	uint32_t	L2C Data-Check-Bits register
L2CCBForcedBits	uint32_t	L2C Data-Check-Bits register
L2CCBForcedFlippedBits	uint32_t	L2C Data-Check-Bits register
L2CCBReadMask	uint32_t	L2C Data-Check-Bits register
L2CCBResetMask	uint32_t	L2C Data-Check-Bits register
L2CCBResetValue	uint32_t	L2C Data-Check-Bits register
L2CCBWriteMask	uint32_t	L2C Data-Check-Bits register
L2CCColdResetValue	uint32_t	L2C Control register
L2CCForcedBits	uint32_t	L2C Control register
L2CCForcedFlippedBits	uint32_t	L2C Control register
L2CCReadMask	uint32_t	L2C Control register
L2CCResetMask	uint32_t	L2C Control register
L2CCResetValue	uint32_t	L2C Control register
L2CCWriteMask	uint32_t	L2C Control register
L2CEINJCFGColdResetValue	uint32_t	L2C injection configuration register
L2CEINJCFGForcedBits	uint32_t	L2C injection configuration register
L2CEINJCFGForcedFlippedBits	uint32_t	L2C injection configuration register
L2CEINJCFGReadMask	uint32_t	L2C injection configuration register
L2CEINJCFGResetMask	uint32_t	L2C injection configuration register
L2CEINJCFGResetValue	uint32_t	L2C injection configuration register

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Name	Type	Description
L2CEINJCFGWriteMask	uint32_t	L2C injection configuration register
L2CEINJColdResetValue	uint32_t	L2C Error injection register
L2CEINJForcedBits	uint32_t	L2C Error injection register
L2CEINJForcedFlippedBits	uint32_t	L2C Error injection register
L2CEINJReadMask	uint32_t	L2C Error injection register
L2CEINJResetMask	uint32_t	L2C Error injection register
L2CEINJResetValue	uint32_t	L2C Error injection register
L2CEINJWriteMask	uint32_t	L2C Error injection register
L2CERRAColdResetValue	uint32_t	L2C Error address register
L2CERRAForcedBits	uint32_t	L2C Error address register
L2CERRAForcedFlippedBits	uint32_t	L2C Error address register
L2CERRAReadMask	uint32_t	L2C Error address register
L2CERRAResetMask	uint32_t	L2C Error address register
L2CERRAResetValue	uint32_t	L2C Error address register
L2CERRAWriteMask	uint32_t	L2C Error address register
L2CERRColdResetValue	uint32_t	L2C Error status/control register
L2CERRForcedBits	uint32_t	L2C Error status/control register
L2CERRForcedFlippedBits	uint32_t	L2C Error status/control register
L2CERRReadMask	uint32_t	L2C Error status/control register
L2CERRResetMask	uint32_t	L2C Error status/control register
L2CERRResetValue	uint32_t	L2C Error status/control register
L2CERRWriteMask	uint32_t	L2C Error status/control register
L2CFMAColdResetValue	uint32_t	L2C Flush memory address register
L2CFMAForcedBits	uint32_t	L2C Flush memory address register

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Name	Type	Description
L2CFMAForcedFlippedBits	uint32_t	L2C Flush memory address register
L2CFMAReadMask	uint32_t	L2C Flush memory address register
L2CFMAResetMask	uint32_t	L2C Flush memory address register
L2CFMAResetValue	uint32_t	L2C Flush memory address register
L2CFMAWriteMask	uint32_t	L2C Flush memory address register
L2CFSIColdResetValue	uint32_t	L2C Flush set/index register
L2CFSIForcedBits	uint32_t	L2C Flush set/index register
L2CFSIForcedFlippedBits	uint32_t	L2C Flush set/index register
L2CFSIReadMask	uint32_t	L2C Flush set/index register
L2CFSIResetMask	uint32_t	L2C Flush set/index register
L2CFSIResetValue	uint32_t	L2C Flush set/index register
L2CFSIWriteMask	uint32_t	L2C Flush set/index register
L2CSCRUBColdResetValue	uint32_t	L2C Scrub control/status register
L2CSCRUBForcedBits	uint32_t	L2C Scrub control/status register
L2CSCRUBForcedFlippedBits	uint32_t	L2C Scrub control/status register
L2CSCRUBReadMask	uint32_t	L2C Scrub control/status register
L2CSCRUBResetMask	uint32_t	L2C Scrub control/status register
L2CSCRUBResetValue	uint32_t	L2C Scrub control/status register
L2CSCRUBWriteMask	uint32_t	L2C Scrub control/status register
L2CSColdResetValue	uint32_t	L2C Status register
L2CSDELColdResetValue	uint32_t	L2C Scrub delay register
L2CSDELForcedBits	uint32_t	L2C Scrub delay register
L2CSDELForcedFlippedBits	uint32_t	L2C Scrub delay register

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Name	Type	Description
L2CSDELReadMask	uint32_t	L2C Scrub delay register
L2CSDELResetMask	uint32_t	L2C Scrub delay register
L2CSDELResetValue	uint32_t	L2C Scrub delay register
L2CSDELWriteMask	uint32_t	L2C Scrub delay register
L2CSForcedBits	uint32_t	L2C Status register
L2CSForcedFlippedBits	uint32_t	L2C Status register
L2CSReadMask	uint32_t	L2C Status register
L2CSResetMask	uint32_t	L2C Status register
L2CSResetValue	uint32_t	L2C Status register
L2CSWriteMask	uint32_t	L2C Status register
L2CTCBColdResetValue	uint32_t	L2C TAG-Check-Bits register
L2CTCBForcedBits	uint32_t	L2C TAG-Check-Bits register
L2CTCBForcedFlippedBits	uint32_t	L2C TAG-Check-Bits register
L2CTCBReadMask	uint32_t	L2C TAG-Check-Bits register
L2CTCBResetMask	uint32_t	L2C TAG-Check-Bits register
L2CTCBResetValue	uint32_t	L2C TAG-Check-Bits register
L2CTCBWriteMask	uint32_t	L2C TAG-Check-Bits register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
accessControl	uint32_t	L2C Access control register
config.littleEndian	uint8_t	Endianess of memory interface.
control	uint32_t	L2C Control register
dataCheckBits	uint32_t	L2C Data-Check-Bits register
errorAddress	uint32_t	L2C Error address register

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Name	Type	Description
errorHandlingAndInjectionConfig	uint32_t	L2C injection configuration register
errorInjection	uint32_t	L2C Error injection register
errorStatusCtrl	uint32_t	L2C Error status/control register
flushMem	uint32_t	L2C Flush memory address register
flushSet	uint32_t	L2C Flush set/index register
mtrr	[uint32_t; 32]	L2C Memory type range register
pnp.bar	uint32_t	
scrubControlStatus	uint32_t	L2C Scrub control/status register
scrubDelay	uint32_t	L2C Scrub delay register
status	uint32_t	L2C Status register
tagCheckBits	uint32_t	L2C TAG-Check-Bits register

Interfaces

Name	Type	Description
AhbIface	AhbIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Registers



Register support is currently experimental!

Register Bank Regs

Register L2CC

Description

L2C Control register

Reset value

0x00040000

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Warm reset mask

0xf007ff3f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	EDAC	REPL		-									BBS			INDEX_WAY				LOCK				-		HPRHB	HPB	UC	HC	WP	HP
rw	rw	rw		-									rw			rw				rw				-		rw	rw	rw	rw	rw	rw
0	0	0		-									4			0				0				-		0	0	0	0	0	0

Field	Mask	Reset	Description
EN	0x80000000	0x0	Cache enable
EDAC	0x40000000	0x0	EDAC enable
REPL	0x30000000	0x0	Replacement policy
BBS	0x00070000	0x4	Backend bus size configuration
INDEX_WAY	0x0000f000	0x0	Master-index replacement
LOCK	0x00000f00	0x0	Locked ways
HPRHB	0x00000020	0x0	HPROT read hit bypass
HPB	0x00000010	0x0	HPROT bufferable
UC	0x00000008	0x0	Bus usage status mode
HC	0x00000004	0x0	Hit rate status mode
WP	0x00000002	0x0	Write policy
HP	0x00000001	0x0	HPROT enable

Register L2CS

Description

L2C Status register

Reset value

0x00502003

Warm reset mask

0x01ffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-							LS	AT	MP	MTRR						BBUS_W			WAY_SIZE											WAY	
-							ro	ro	ro	ro						ro			ro											ro	
-							0	0	1	16						1			0											3	

Field	Mask	Reset	Description
LS	0x01000000	0x0	Cache line size
AT	0x00800000	0x0	Access time
MP	0x00400000	0x1	Memory protection
MTRR	0x003f0000	0x10	Number of MTRR registers implemented

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Field	Mask	Reset	Description
BBUS_W	0x0000e000	0x1	Backend bus width
WAY_SIZE	0x00001ffc	0x0	Cache way size
WAY	0x00000003	0x3	Multi-way configuration

Register L2CFMA

Description

L2C Flush memory address register

Reset value

0x00000000

Warm reset mask

0x00000007

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																											-	DI	FMODE		
rw																											-	wo	rw		
-																											-	-	0		

Field	Mask	Reset	Description
ADDR	0xfffffe0	-	Memory address
DI	0x00000008	-	Cache disable
FMODE	0x00000007	0x0	Flush mode

Register L2CFSI

Description

L2C Flush set/index register

Reset value

0x00000000

Warm reset mask

0x000003b7

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INDEX_TAG																-						FL	VB	DB	-	WAY		DI	WF	FMODE	
rw																-						rw	rw	rw	-	rw		wo	rw	rw	
-																-						0	0	0	-	0		-	0	0	

Field	Mask	Reset	Description
INDEX_TAG	0xffff0000	-	Cache line index or tag
FL	0x00000200	0x0	Fetch line
VB	0x00000100	0x0	Valid bit

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Field	Mask	Reset	Description
DB	0x00000080	0x0	Dirty bit
WAY	0x00000030	0x0	Cache way
DI	0x00000008	-	Cache disable
WF	0x00000004	0x0	Way flush
FMODE	0x00000003	0x0	Flush mode

Register L2CERR

Description

L2C Error status/control register

Reset value

0x00000000

Warm reset mask

0x00000ffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASTER				SCRUB	TYPE			TAGDATA	UNCORRECTABLE	MULTI	VALID	DISERESP	CORRECTABLE_COUNT			IRQ_PENDING				IRQ_MASK				CB				TCB		XOR	RCB	COMPRST	
ro				ro	ro			ro	ro	ro	ro	rw	ro			ro				rw				rw				rw		rw	rw	wo	
-				-	-			-	-	-	-	-	-			-				0				0				0		0	0	-	

Field	Mask	Reset	Description
MASTER	0xf0000000	-	AHB master that generated the access
SCRUB	0x08000000	-	Scrub error
TYPE	0x07000000	-	Access/error type
TAGDATA	0x00800000	-	Tag or data error
UNCORRECTABLE	0x00400000	-	Correctable or uncorrectable error
MULTI	0x00200000	-	Multiple error
VALID	0x00100000	-	Error status valid
DISERESP	0x00080000	-	Disable error responses for uncorrectable EDAC error
CORRECTABLE_COUNT	0x00070000	-	Correctable error counter
IRQ_PENDING	0x0000f000	-	Interrupt pending
IRQ_MASK	0x00000f00	0x0	Interrupt mask
CB	0x000000c0	0x0	Select data check-bits for diagnostic data write
TCB	0x00000030	0x0	Select tag check-bits for diagnostic tag write
XOR	0x00000008	0x0	Xor check-bits
RCB	0x00000004	0x0	Read check-bits

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Field	Mask	Reset	Description
COMP	0x00000002	0x0	Compare error status
RST	0x00000001	-	Reset error status

Register L2CERRA

Description

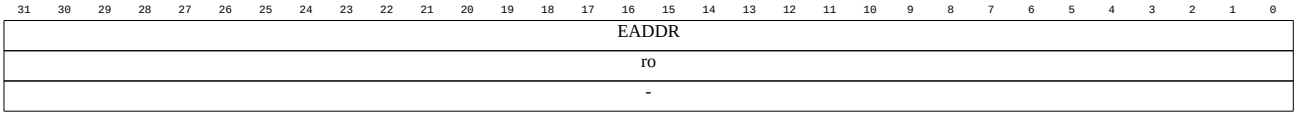
L2C Error address register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
EADDR	0xffffffff	-	Error address

Register L2CTCB

Description

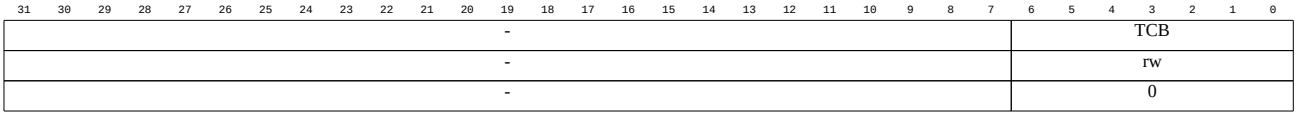
L2C TAG-Check-Bits register

Reset value

0x00000000

Warm reset mask

0x0000007f



Field	Mask	Reset	Description
TCB	0x0000007f	0x0	TAG check-bits

Register L2CCB

Description

L2C Data-Check-Bits register

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Reset value

0x00000000

Warm reset mask

0x0fffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-				CB																											
-				rw																											
-				0																											

Field	Mask	Reset	Description
CB	0x0fffffff	0x0	Data check-bits

Register L2CSCRUB

Description

L2C Scrub control/status register

Reset value

0x00000000

Warm reset mask

0xffff000f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INDEX																-												WAY		PEN	EN
rw																-												rw		rw	rw
0																-												0		0	0

Field	Mask	Reset	Description
INDEX	0xffff0000	0x0	Scrub index
WAY	0x0000000c	0x0	Scrub way
PEN	0x00000002	0x0	Scrub pending
EN	0x00000001	0x0	Scrub enable

Register L2CSDEL

Description

L2C Scrub delay register

Reset value

0x00000000

Warm reset mask

0x0000ffff

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																DEL															
-																rw															
-																0															

Field	Mask	Reset	Description
DEL	0x0000ffff	0x0	Scrub delay

Register L2CEINJ

Description

L2C Error injection register

Reset value

0x00000000

Warm reset mask

0xfffffffd

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																														-	INJ
rw																														-	rw
0																														-	0

Field	Mask	Reset	Description
ADDR	0xfffffffc	0x0	Error inject address
INJ	0x00000001	0x0	Inject error

Register L2CACCC

Description

L2C Access control register

Reset value

0x00000000

Warm reset mask

0x000067f6

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																	DSC	SH	-		SPLITQ	HM	BERR	DAPM	LINE	DBPI	28W	F	-	DBPW	SPLIT	-
-																	rw	rw	-		rw	rw	rw	rw	rw	rw	rw	-	-	rw	rw	-
-																	0	0	-		0	0	0	0	0	0	0	-	-	0	0	-

Field	Mask	Reset	Description
DSC	0x00004000	0x0	Disable cancellation and reissue of scrubber operation
SH	0x00002000	0x0	Scrubber hold
SPLITQ	0x00000400	0x0	SPLIT queue write order

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Field	Mask	Reset	Description
NHM	0x00000200	0x0	No hit for cache misses
BERR	0x00000100	0x0	Bit error status
OAPM	0x00000080	0x0	One access per master
FLINE	0x00000040	0x0	Fetch line replacement
DBPF	0x00000020	0x0	Disable bypass prefetching
128WF	0x00000010	0x0	128-bit write line fetch
DBPWS	0x00000004	0x0	Disable wait-states for discarded bypass data
SPLIT	0x00000002	0x0	Enable SPLIT response

Register L2CEINJCFG

Description

L2C injection configuration register

Reset value

0x00000000

Warm reset mask

0x00000700

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																					EDI	TER	IMD	-							
-																					rw	rw	rw	-							
-																					0	0	0	-							

Field	Mask	Reset	Description
EDI	0x00000400	0x0	Enable invalidation of cache line with uncorrectable data error
TER	0x00000200	0x0	Disable error response on uncorrectable TAG error detection
IMD	0x00000100	0x0	Disable index match only after uncorrectable TAG error

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

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31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

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31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
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Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

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31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

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31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

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31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

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31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
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L2C Memory type range register

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Warm reset mask

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31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
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0	0	0	0	0

Field	Mask	Reset	Description
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ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

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L2C Memory type range register

Reset value

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Warm reset mask

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rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
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ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
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ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

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31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
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Description

L2C Memory type range register

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Warm reset mask

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ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
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L2C Memory type range register

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Warm reset mask

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31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

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Warm reset mask

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ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

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L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

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L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Register L2CMTRR

Description

L2C Memory type range register

Reset value

0x00000000

Warm reset mask

0xffffffff

31 30 29 28 27 26 25 24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1	0
ADDR	ACC	MASK	WP	AC
rw	rw	rw	rw	rw
0	0	0	0	0

Field	Mask	Reset	Description
ADDR	0xfffc0000	0x0	Address field
ACC	0x00030000	0x0	Access field
MASK	0x0000fffc	0x0	Address mask
WP	0x00000002	0x0	Write protection
AC	0x00000001	0x0	Access control field

Commands

Name	Description
delete	Dispose instance of GrlibL2Cache

9.20.5. Limitations

9.21. MCTRL

The MCtrl device is part of the GRLIB IP library. It is available in `libTEMUMCtrl.so`.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

9.21.1. Loading the Plugin

```
import MCtrl
```

9.21.2. Configuration

9.21.3. @MCtrl Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @MCtrl
new	Create new instance of MCtrl

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.21.4. MCtrl Reference

Properties

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
MCFG1ColdResetValue	uint32_t	Memory configuration register 1
MCFG1ForcedBits	uint32_t	Memory configuration register 1
MCFG1ForcedFlippedBits	uint32_t	Memory configuration register 1
MCFG1ReadMask	uint32_t	Memory configuration register 1
MCFG1ResetMask	uint32_t	Memory configuration register 1
MCFG1ResetValue	uint32_t	Memory configuration register 1
MCFG1WriteMask	uint32_t	Memory configuration register 1
MCFG2ColdResetValue	uint32_t	Memory configuration register 2
MCFG2ForcedBits	uint32_t	Memory configuration register 2
MCFG2ForcedFlippedBits	uint32_t	Memory configuration register 2
MCFG2ReadMask	uint32_t	Memory configuration register 2
MCFG2ResetMask	uint32_t	Memory configuration register 2
MCFG2ResetValue	uint32_t	Memory configuration register 2
MCFG2WriteMask	uint32_t	Memory configuration register 2

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
MCFG3ColdResetValue	uint32_t	Memory configuration register 3
MCFG3ForcedBits	uint32_t	Memory configuration register 3
MCFG3ForcedFlippedBits	uint32_t	Memory configuration register 3
MCFG3ReadMask	uint32_t	Memory configuration register 3
MCFG3ResetMask	uint32_t	Memory configuration register 3
MCFG3ResetValue	uint32_t	Memory configuration register 3
MCFG3WriteMask	uint32_t	Memory configuration register 3
MCFG4ColdResetValue	uint32_t	Power-saving configuration register
MCFG4ForcedBits	uint32_t	Power-saving configuration register
MCFG4ForcedFlippedBits	uint32_t	Power-saving configuration register
MCFG4ReadMask	uint32_t	Power-saving configuration register
MCFG4ResetMask	uint32_t	Power-saving configuration register
MCFG4ResetValue	uint32_t	Power-saving configuration register
MCFG4WriteMask	uint32_t	Power-saving configuration register
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
ahb.pnp.bar	[uint32_t; 4]	
ahb.pnp.identReg	uint32_t	
ahb.pnp.userDef	[uint32_t; 3]	

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
apb.pnp.bar	uint32_t	
apb.pnp.config	uint32_t	
config.littleEndian	uint8_t	Endianess of memory interface.
mcfg1	uint32_t	Memory configuration register 1
mcfg2	uint32_t	Memory configuration register 2
mcfg3	uint32_t	Memory configuration register 3
mcfg4	uint32_t	Power-saving configuration register

Interfaces

Name	Type	Description
AhbIface	AhbIface	
ApbIface	ApbIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Commands

Name	Description
delete	Dispose instance of MCtrl

9.21.5. Limitations

9.22. GR740THSENS

The GR740THSENS device is part of the GRLIB IP library. It is available in `libTEMUGR740THSENS.so`.

9.22.1. Loading the Plugin

```
import GR740THSENS
```

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

9.22.2. Configuration

9.22.3. @GR740THSENS Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GR740THSENS
new	Create new instance of GR740THSENS

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.22.4. GR740THSENS Reference

Properties

Name	Type	Description
CTRLColdResetValue	uint32_t	Control Register
CTRLForcedBits	uint32_t	Control Register
CTRLForcedFlippedBits	uint32_t	Control Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
CTRLReadMask	uint32_t	Control Register
CTRLResetMask	uint32_t	Control Register
CTRLResetValue	uint32_t	Control Register
CTRLWriteMask	uint32_t	Control Register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
ControlReg	uint32_t	Control Register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
STATUSColdResetValue	uint32_t	Status register
STATUSForcedBits	uint32_t	Status register
STATUSForcedFlippedBits	uint32_t	Status register
STATUSReadMask	uint32_t	Status register
STATUSResetMask	uint32_t	Status register
STATUSResetValue	uint32_t	Status register
STATUSWriteMask	uint32_t	Status register
StatusReg	uint32_t	Status register
THRESColdResetValue	uint32_t	Threshold register
THRESForcedBits	uint32_t	Threshold register
THRESForcedFlippedBits	uint32_t	Threshold register
THRESReadMask	uint32_t	Threshold register
THRESResetMask	uint32_t	Threshold register
THRESResetValue	uint32_t	Threshold register
THRESWriteMask	uint32_t	Threshold register
ThresholdReg	uint32_t	Threshold register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
TimeSource	*void	Time source object
apb.pnp.bar	uint32_t	
apb.pnp.config	uint32_t	
config.littleEndian	uint8_t	Endianess of memory interface.

Interfaces

Name	Type	Description
ApbIface	ApbIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Registers



Register support is currently experimental!

Register Bank Regs

Register CTRL

Description

Control Register

Reset value

0x00000000

Warm reset mask

0x03ff01ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-						div										-							alen	pdn	dcorrect					srstn	clken	
-						rw										-							rw	rw	rw					rw	rw	
-						0										-							0	0	0					0	0	

Field	Mask	Reset	Description
div	0x03ff0000	0x0	Temp sensor clock divider
alen	0x00000100	0x0	Alarm enabled
pdn	0x00000080	0x0	Power down
dcorrect	0x0000007c	0x0	Offset correction

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
srstn	0x00000002	0x0	Sensor reset
clken	0x00000001	0x0	Clock enabled

Register STATUS

Description

Status register

Reset value

0x007f0000

Warm reset mask

0x7f7f867f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	max							-	min							sclk	-				we	upd	alact	-	data						
-	rw							-	rw							ro	-				rw	ro	rw	-	ro						
-	0							-	127							0	-				0	0	-	-	0						

Field	Mask	Reset	Description
max	0x7f000000	0x0	Maximum value (W only if WE=1)
min	0x007f0000	0x7f	Minimum value (W only if WE=1)
sclk	0x00008000	0x0	Sensor clock
we	0x00000400	0x0	Write enable
upd	0x00000200	0x0	Update
alact	0x00000100	-	Alarm active
data	0x0000007f	0x0	Data value

Register THRES

Description

Threshold register

Reset value

0x00000000

Warm reset mask

0x0000007f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																									thres						
-																									rw						
-																									0						

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
thres	0x0000007f	0x0	Threshold

Commands

Name	Description
delete	Dispose instance of GR740THSENS

9.22.5. Limitations

The GR740THSENSE does not interact with the environment.

The device is non-functional, in that it only provides registers for reading and writing.

9.23. L4STAT

The L4STAT device is part of the GRLIB IP library. It is available in `libTEMUL4STAT.so`.

9.23.1. Loading the Plugin

```
import L4STAT
```

9.23.2. Configuration

9.23.3. @L4STAT Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @L4STAT
new	Create new instance of L4STAT

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.23.4. L4STAT Reference

Properties

Name	Type	Description
CCTRL	[uint32_t; 16]	Counter control register
CSVAL	[uint32_t; 16]	Counter max/latch register
CVAL	[uint32_t; 16]	Counter value register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TSTAMP	uint32_t	Timestamp register
TSTAMPColdResetValue	uint32_t	Timestamp register
TSTAMPForcedBits	uint32_t	Timestamp register

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Name	Type	Description
TSTAMPForcedFlippedBits	uint32_t	Timestamp register
TSTAMPReadMask	uint32_t	Timestamp register
TSTAMPResetMask	uint32_t	Timestamp register
TSTAMPResetValue	uint32_t	Timestamp register
TSTAMPWriteMask	uint32_t	Timestamp register
TimeSource	*void	Time source object
apb.pnp.bar	uint32_t	
apb.pnp.config	uint32_t	
config.littleEndian	uint8_t	Endianess of memory interface.

Interfaces

Name	Type	Description
ApbIface	ApbIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Registers



Register support is currently experimental!

Register Bank Regs

Register TSTAMP

Description

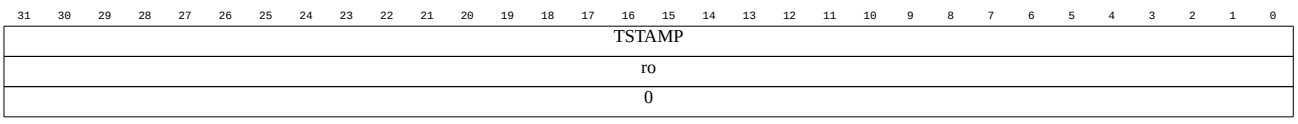
Timestamp register

Reset value

0x00000000

Warm reset mask

0xffffffff



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Field	Mask	Reset	Description
TSTAMP	0xffffffff	0x0	Timestamp

Register CVAL

Description

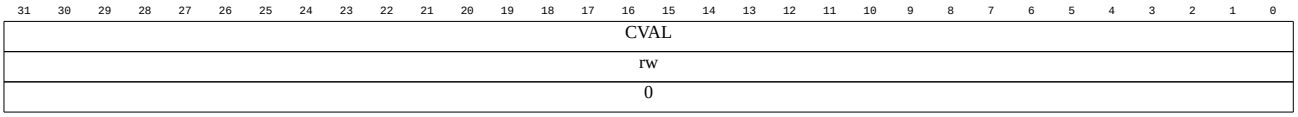
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

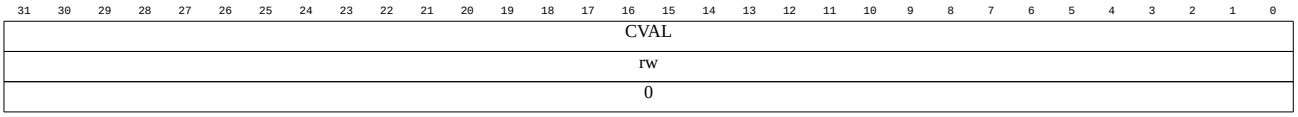
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

Counter value register

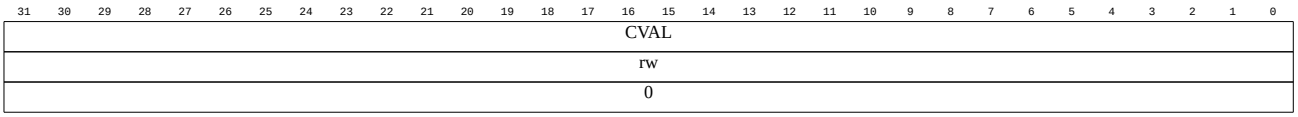
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

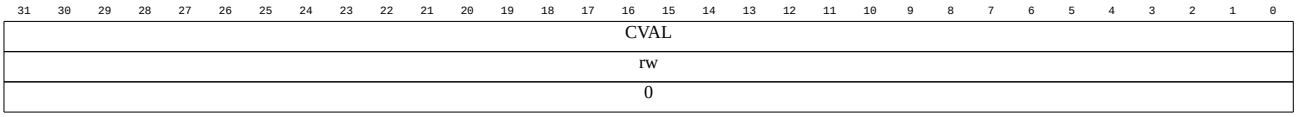
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

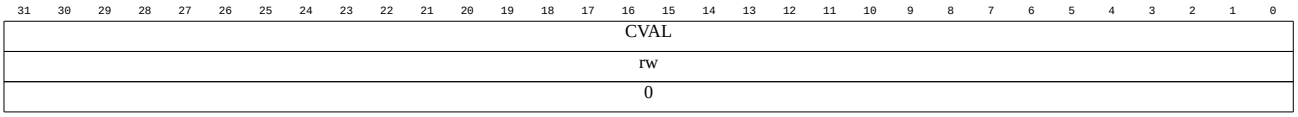
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

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Description

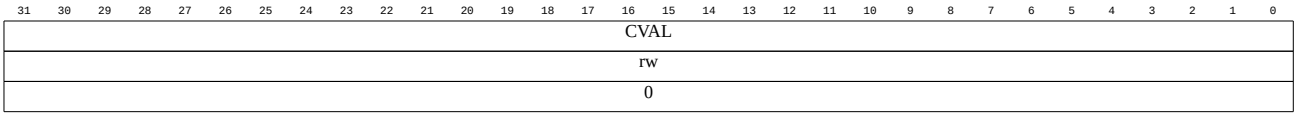
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

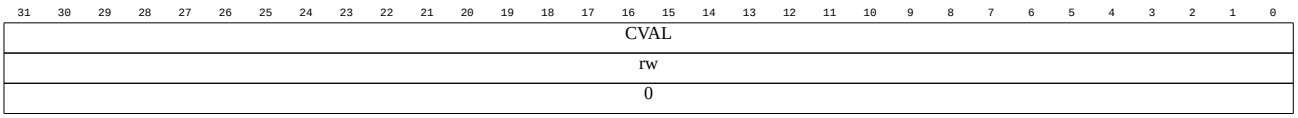
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

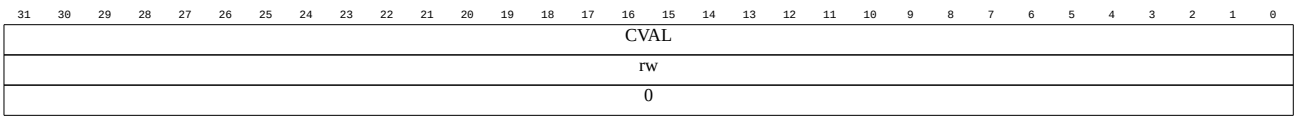
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



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Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

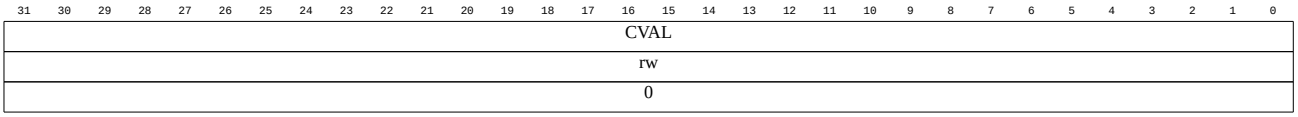
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

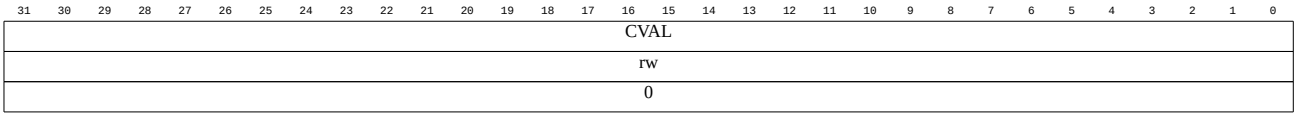
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

Counter value register

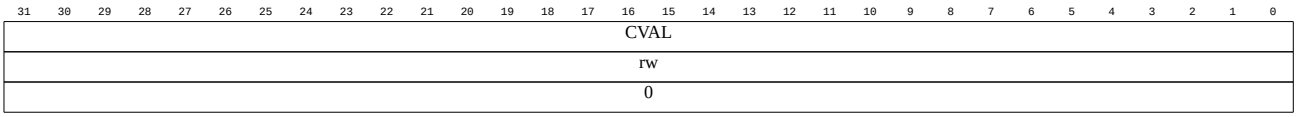
Reset value

0x00000000

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Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

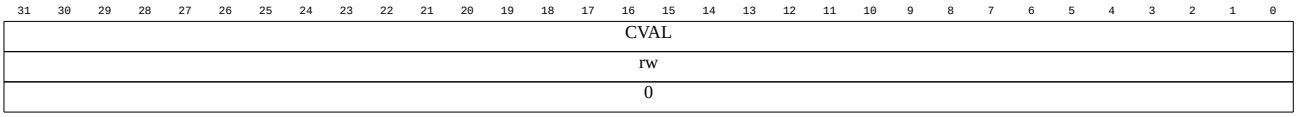
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

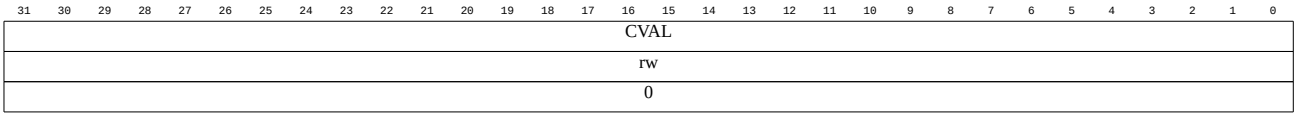
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

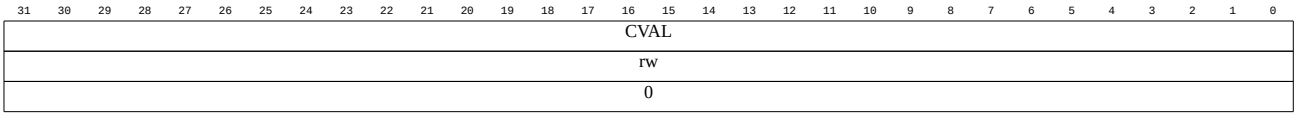
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

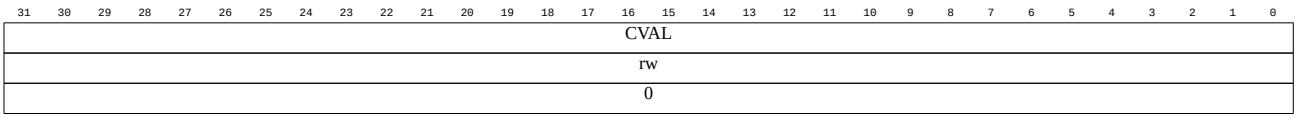
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CVAL

Description

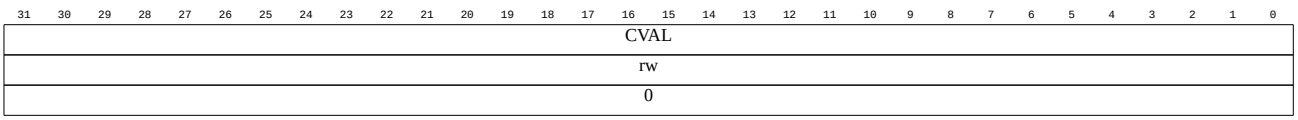
Counter value register

Reset value

0x00000000

Warm reset mask

0xffffffff



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Field	Mask	Reset	Description
CVAL	0xffffffff	0x0	Counter value

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCPU				NCNT					MC	IA	DS	EE	AE	EL	CD	SU		CL	EN	EVENT								CPU_AHBM			
ro				ro					ro	ro	ro	ro	ro	rw	rw	rw		rw	rw	rw								rw			
3				15					1	1	1	1	1	0	0	0		0	0	0								0			

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

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Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCPU				NCNT					MC	IA	DS	EE	AE	EL	CD	SU		CL	EN	EVENT								CPU_AHBM			
ro				ro					ro	ro	ro	ro	ro	rw	rw	rw		rw	rw	rw								rw			
3				15					1	1	1	1	1	0	0	0		0	0	0								0			

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCPU				NCNT					MC	IA	DS	EE	AE	EL	CD	SU		CL	EN	EVENT								CPU_AHBM			
ro				ro					ro	ro	ro	ro	ro	rw	rw	rw		rw	rw	rw								rw			
3				15					1	1	1	1	1	0	0	0		0	0	0								0			

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one

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Field	Mask	Reset	Description
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4	3 2 1 0
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level

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Field	Mask	Reset	Description
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4	3 2 1 0
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

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Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4	3 2 1 0
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

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31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4	3 2 1 0
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4	3 2 1 0
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support

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Field	Mask	Reset	Description
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4 3 2 1 0	
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter

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Field	Mask	Reset	Description
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4	3 2 1 0
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4	3 2 1 0
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4	3 2 1 0
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4	3 2 1 0
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4 3 2 1 0
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4	3 2 1 0
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CCTRL

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Description

Counter control register

Reset value

0x37fc0000

Warm reset mask

0xffffffff

31 30 29 28	27 26 25 24 23	22	21	20	19	18	17	16	15 14	13	12	11 10 9 8 7 6 5 4	3 2 1 0
NCPU	NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT	CPU_AHBM
ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw
3	15	1	1	1	1	1	0	0	0	0	0	0	0

Field	Mask	Reset	Description
NCPU	0xf0000000	0x3	Number of supported processors minus one
NCNT	0x0f800000	0xf	Number of implemented counters minus one
MC	0x00400000	0x1	Maximum count support
IA	0x00200000	0x1	Internal AHB count support
DS	0x00100000	0x1	DSU support
EE	0x00080000	0x1	External event support
AE	0x00040000	0x1	AHBTRACE event support
EL	0x00020000	0x0	Event level
CD	0x00010000	0x0	Count maximum duration
SU	0x0000c000	0x0	Supervisor/User mode filter
CL	0x00002000	0x0	Clear counter on read
EN	0x00001000	0x0	Enable counter
EVENT	0x00000ff0	0x0	Event ID to be counted
CPU_AHBM	0x0000000f	0x0	CPU or AHB master to monitor

Register CSVAL

Description

Counter max/latch register

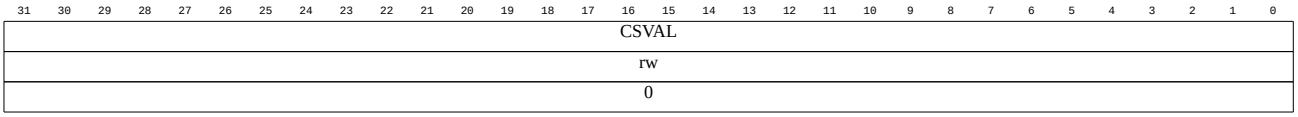
Reset value

0x00000000

Warm reset mask

0xffffffff

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

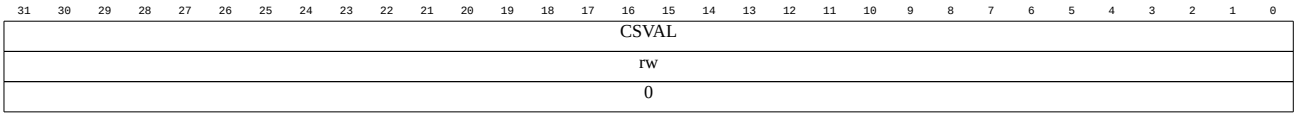
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

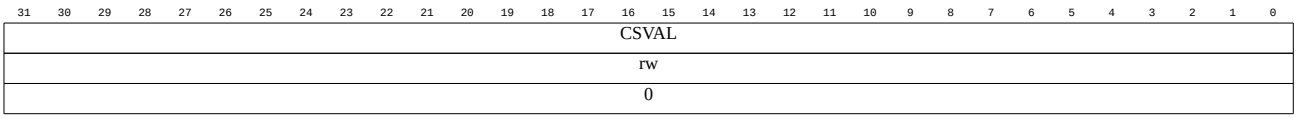
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

Counter max/latch register

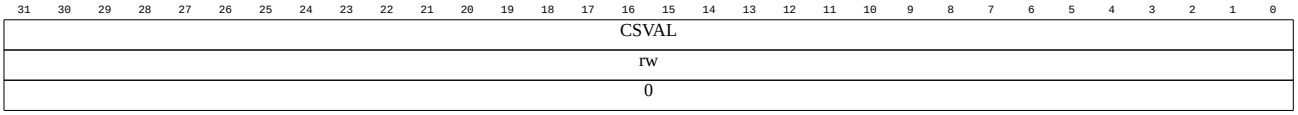
The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

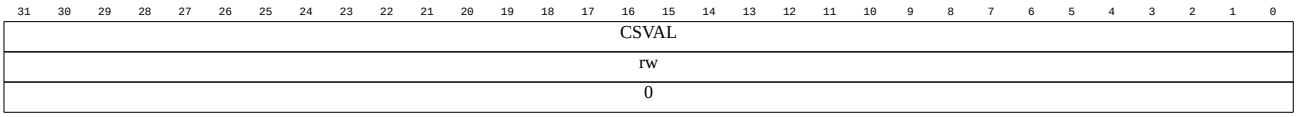
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

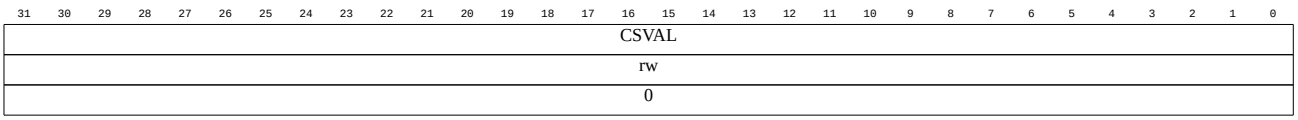
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

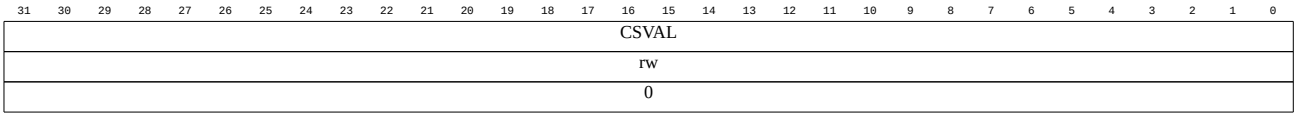
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

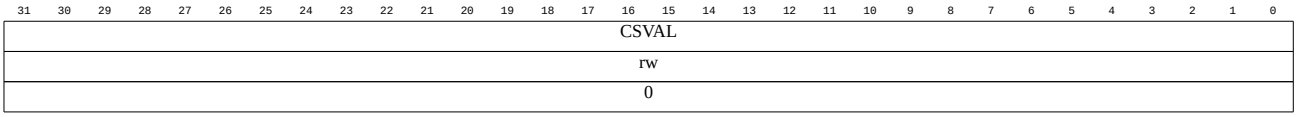
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

Counter max/latch register

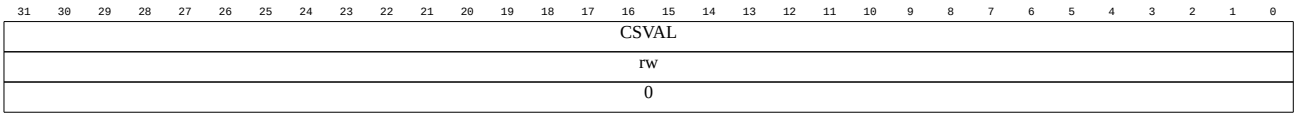
Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

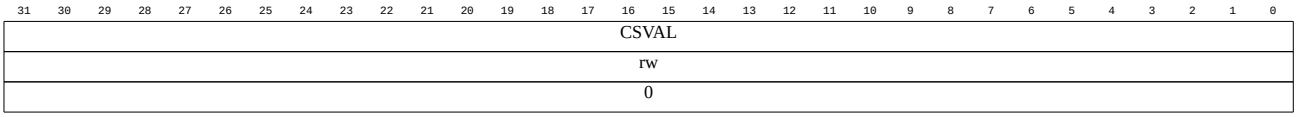
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

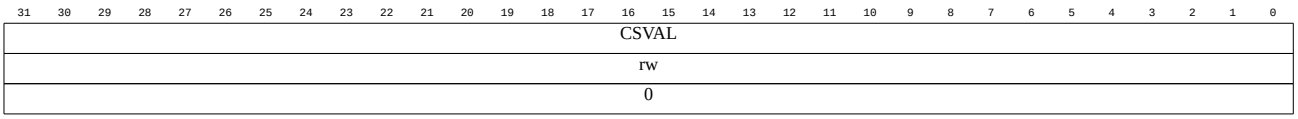
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

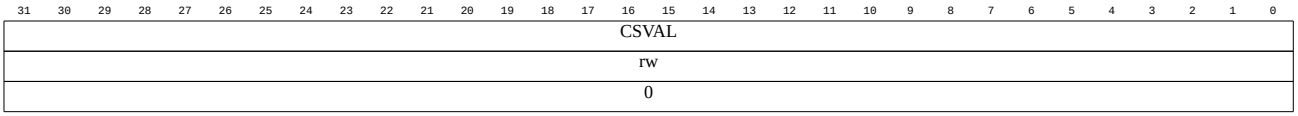
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

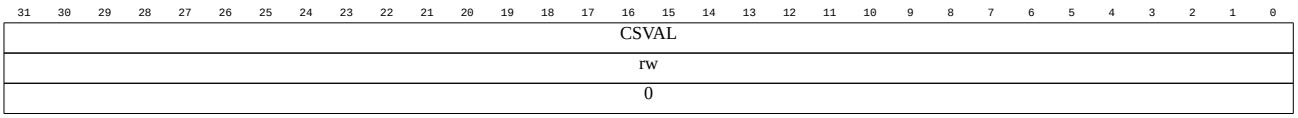
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

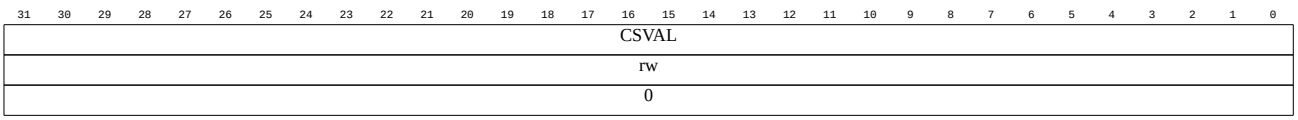
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

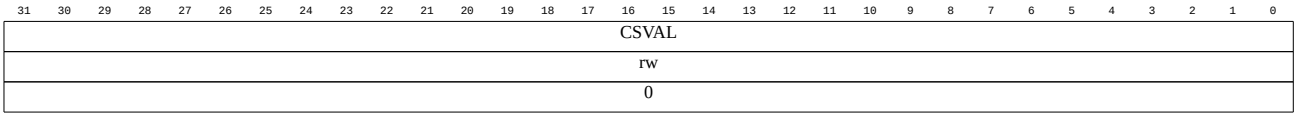
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Register CSVAL

Description

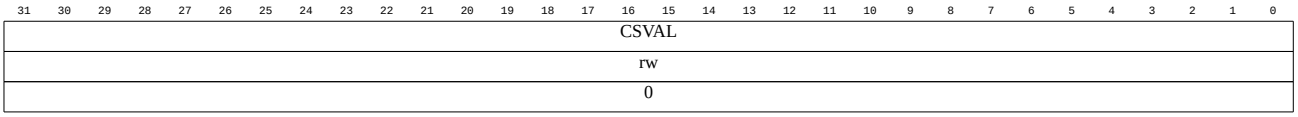
Counter max/latch register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CSVAL	0xffffffff	0x0	Counter max/latch value

Commands

Name	Description
delete	Dispose instance of L4STAT

9.23.5. Limitations

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

The L4STAT device is non-functional, providing only registers and PNP data. Statistics is thus not collected by the device.

The end user is expected to write to registers manually, in order to inject statistics data.

9.24. MEMSCRUB

The MEMSCRUB device is part of the GRLIB IP library. It is available in `libTEMUMEMSCRUB.so`.

9.24.1. Loading the Plugin

```
import MEMSCRUB
```

9.24.2. Configuration

9.24.3. @MEMSCRUB Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @MEMSCRUB
new	Create new instance of MEMSCRUB

Command new Arguments

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Required	Description
name	string	yes	Name of object to create

9.24.4. MEMSCRUB Reference

Properties

Name	Type	Description
AHBERC	uint32_t	AHB Error configuration register
AHBERCColdResetValue	uint32_t	AHB Error configuration register
AHBERCForcedBits	uint32_t	AHB Error configuration register
AHBERCForcedFlippedBits	uint32_t	AHB Error configuration register
AHBERCReadMask	uint32_t	AHB Error configuration register
AHBERCResetMask	uint32_t	AHB Error configuration register
AHBERCResetValue	uint32_t	AHB Error configuration register
AHBERCWriteMask	uint32_t	AHB Error configuration register
AHBFAR	uint32_t	AHB Failing Address Register
AHBFARColdResetValue	uint32_t	AHB Failing Address Register
AHBFARForcedBits	uint32_t	AHB Failing Address Register
AHBFARForcedFlippedBits	uint32_t	AHB Failing Address Register
AHBFARReadMask	uint32_t	AHB Failing Address Register
AHBFARResetMask	uint32_t	AHB Failing Address Register
AHBFARResetValue	uint32_t	AHB Failing Address Register
AHBFARWriteMask	uint32_t	AHB Failing Address Register
AHBS	uint32_t	AHB Status register
AHBSColdResetValue	uint32_t	AHB Status register
AHBSForcedBits	uint32_t	AHB Status register
AHBSForcedFlippedBits	uint32_t	AHB Status register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
AHBSReadMask	uint32_t	AHB Status register
AHBSResetMask	uint32_t	AHB Status register
AHBSResetValue	uint32_t	AHB Status register
AHBSWriteMask	uint32_t	AHB Status register
CONFIG	uint32_t	Configuration register
CONFIGColdResetValue	uint32_t	Configuration register
CONFIGForcedBits	uint32_t	Configuration register
CONFIGForcedFlippedBits	uint32_t	Configuration register
CONFIGReadMask	uint32_t	Configuration register
CONFIGResetMask	uint32_t	Configuration register
CONFIGResetValue	uint32_t	Configuration register
CONFIGWriteMask	uint32_t	Configuration register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
ETHRES	uint32_t	Error threshold register
ETHRESColdResetValue	uint32_t	Error threshold register
ETHRESForcedBits	uint32_t	Error threshold register
ETHRESForcedFlippedBits	uint32_t	Error threshold register
ETHRESReadMask	uint32_t	Error threshold register
ETHRESResetMask	uint32_t	Error threshold register
ETHRESResetValue	uint32_t	Error threshold register
ETHRESWriteMask	uint32_t	Error threshold register
INIT	uint32_t	Initialisation data register
INITColdResetValue	uint32_t	Initialisation data register
INITForcedBits	uint32_t	Initialisation data register
INITForcedFlippedBits	uint32_t	Initialisation data register
INITReadMask	uint32_t	Initialisation data register
INITResetMask	uint32_t	Initialisation data register
INITResetValue	uint32_t	Initialisation data register
INITWriteMask	uint32_t	Initialisation data register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
POS	uint32_t	Position register
POSColdResetValue	uint32_t	Position register
POSForcedBits	uint32_t	Position register
POSForcedFlippedBits	uint32_t	Position register
POSReadMask	uint32_t	Position register
POSResetMask	uint32_t	Position register
POSResetValue	uint32_t	Position register
POSWriteMask	uint32_t	Position register
RANGEH	uint32_t	Range high address register
RANGEH2	uint32_t	Second range high address register
RANGEH2ColdResetValue	uint32_t	Second range high address register
RANGEH2ForcedBits	uint32_t	Second range high address register
RANGEH2ForcedFlippedBits	uint32_t	Second range high address register
RANGEH2ReadMask	uint32_t	Second range high address register
RANGEH2ResetMask	uint32_t	Second range high address register
RANGEH2ResetValue	uint32_t	Second range high address register
RANGEH2WriteMask	uint32_t	Second range high address register
RANGEHColdResetValue	uint32_t	Range high address register
RANGEHForcedBits	uint32_t	Range high address register
RANGEHForcedFlippedBits	uint32_t	Range high address register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
RANGEHReadMask	uint32_t	Range high address register
RANGEHResetMask	uint32_t	Range high address register
RANGEHResetValue	uint32_t	Range high address register
RANGEHWriteMask	uint32_t	Range high address register
RANGEL	uint32_t	Range low address register
RANGEL2	uint32_t	Second range low address register
RANGEL2ColdResetValue	uint32_t	Second range low address register
RANGEL2ForcedBits	uint32_t	Second range low address register
RANGEL2ForcedFlippedBits	uint32_t	Second range low address register
RANGEL2ReadMask	uint32_t	Second range low address register
RANGEL2ResetMask	uint32_t	Second range low address register
RANGEL2ResetValue	uint32_t	Second range low address register
RANGEL2WriteMask	uint32_t	Second range low address register
RANGELColdResetValue	uint32_t	Range low address register
RANGELForcedBits	uint32_t	Range low address register
RANGELForcedFlippedBits	uint32_t	Range low address register
RANGELReadMask	uint32_t	Range low address register
RANGELResetMask	uint32_t	Range low address register
RANGELResetValue	uint32_t	Range low address register
RANGELWriteMask	uint32_t	Range low address register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
STAT	uint32_t	Status register
STATColdResetValue	uint32_t	Status register
STATForcedBits	uint32_t	Status register
STATForcedFlippedBits	uint32_t	Status register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
STATReadMask	uint32_t	Status register
STATResetMask	uint32_t	Status register
STATResetValue	uint32_t	Status register
STATWriteMask	uint32_t	Status register
TimeSource	*void	Time source object
ahb.pnp.bar	[uint32_t; 4]	AMBA plug and play base address register
ahb.pnp.identReg	uint32_t	AMBA plug and play config word
ahb.pnp.userDef	[uint32_t; 3]	AMBA plug and play user words
config.littleEndian	uint8_t	Endianess of memory interface.

Interfaces

Name	Type	Description
AhbIface	AhbIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Registers



Register support is currently experimental!

Register Bank Regs

Register AHBS

Description

AHB Status register

Reset value

0x00000000

Warm reset mask

0xffffef00

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31 30 29 28 27 26 25 24 23 22	21 20 19 18 17 16 15 14	13	12	11	10	9	8	7	6 5 4	3 2 1 0
CECNT	UECNT	DONE	-	SEC	SBC	CE	NE	HWRITE	HMASTER	HSIZE
rw	rw	ro	-	rw	rw	rw	rw	ro	ro	ro
0	0	0	-	0	0	0	0	-	-	-

Field	Mask	Reset	Description
CECNT	0xffc00000	0x0	Global correctable error count
UECNT	0x003fc000	0x0	Global uncorrectable error count
DONE	0x00002000	0x0	Task completed
SEC	0x00000800	0x0	Scrubber error counter threshold exceeded
SBC	0x00000400	0x0	Scrubber block error counter threshold exceeded
CE	0x00000200	0x0	Correctable error
NE	0x00000100	0x0	New error
HWRITE	0x00000080	-	AMBA write signal
HMASTER	0x00000078	-	AMBA master signal
HSIZE	0x00000007	-	AMBA size signal

Register AHBFAR

Description

AHB Failing Address Register

Reset value

0x00000000

Warm reset mask

0x00000000

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
AHB_FAILING_ADDRESS
ro
-

Field	Mask	Reset	Description
AHB_FAILING_ADDRESS	0xffffffff	-	AHB failing address

Register AHBERC

Description

AHB Error configuration register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffc003

31 30 29 28 27 26 25 24 23 22	21 20 19 18 17 16 15 14	13 12 11 10 9 8 7 6 5 4 3 2	1	0
CECNTT	UECNTT	-	CECTE	UECTE
rw	rw	-	rw	rw
0	0	-	0	0

Field	Mask	Reset	Description
CECNTT	0xffc00000	0x0	Interrupt threshold value for global correctable error count
UECNTT	0x003fc000	0x0	Interrupt threshold value for global uncorrectable error count
CECTE	0x00000002	0x0	Correctable error count threshold enable
UECTE	0x00000001	0x0	Uncorrectable error count threshold enable

Register STAT

Description

Status register

Reset value

0x00000002

Warm reset mask

0xffffc01f

31 30 29 28 27 26 25 24 23 22	21 20 19 18 17 16 15 14	13	12 11 10 9 8 7 6 5	4 3 2 1	0
RUNCOUNT	BLKCOUNT	DONE	-	BURSTLEN	ACTIV
ro	ro	rw	-	ro	ro
0	0	-	-	1	0

Field	Mask	Reset	Description
RUNCOUNT	0xffc00000	0x0	Number of correctable errors in current scrub run
BLKCOUNT	0x003fc000	0x0	Number of correctable errors in current block
DONE	0x00002000	-	Task completed
BURSTLEN	0x0000001e	0x1	2-log of AHB bus cycles
ACTIVE	0x00000001	0x0	Current state

Register CONFIG

Description

Configuration register

Reset value

0x00000000

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0x0000ffbf

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																DELAY								IRQD	-	SERA	LOOP	MODE		ES	SCEN
-																rw								rw	-	rw	rw	rw		rw	rw
-																0								0	-	0	0	0		0	0

Field	Mask	Reset	Description
DELAY	0x0000ff00	0x0	Delay time between processed blocks
IRQD	0x00000080	0x0	Interrupt when task has completed
SERA	0x00000020	0x0	Second memory range enable
LOOP	0x00000010	0x0	Loop mode
MODE	0x0000000c	0x0	Operation mode
ES	0x00000002	0x0	External start enable
SCEN	0x00000001	0x0	Scrubber enable

Register RANGEL

Description

Range low address register

Reset value

0x00000000

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RLADDR																												ALIGN			
rw																												ro			
0																												0			

Field	Mask	Reset	Description
RLADDR	0xffffffe0	0x0	Scrubber range low address
ALIGN	0x0000001f	0x0	Burst size alignment bits

Register RANGEH

Description

Range high address register

Reset value

0x0000001f

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RHADDR																														ALIGN	
rw																														ro	
0																														31	

Field	Mask	Reset	Description
RHADDR	0xfffffffe0	0x0	Scrubber range high address
ALIGN	0x0000001f	0x1f	Burst size alignment bits

Register POS

Description

Position register

Reset value

0x00000000

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POSITION																														ALIGN	
rw																														ro	
0																														0	

Field	Mask	Reset	Description
POSITION	0xfffffffe0	0x0	Scrubber position
ALIGN	0x0000001f	0x0	Burst size alignment bits

Register ETHRES

Description

Error threshold register

Reset value

0x00000000

Warm reset mask

0xffffc003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RECT										BECT								-												RECT	RECT
rw										rw								-												rw	rw
0										0								-												0	0

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
RECT	0xffc00000	0x0	Interrupt threshold value for current scrub run correctable error count
BECT	0x003fc000	0x0	Interrupt threshold value for current scrub block correctable error count
RECTE	0x00000002	0x0	Scrub run correctable error count threshold enable
BECTE	0x00000001	0x0	Scrub block correctable error count threshold enable

Register INIT

Description

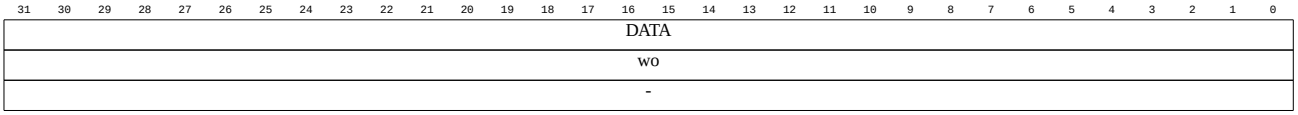
Initialisation data register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
DATA	0xffffffff	-	Initialisation data

Register RANGEL2

Description

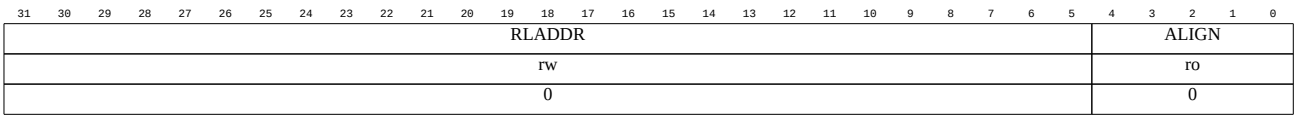
Second range low address register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
RLADDR	0xffffffe0	0x0	Scrubber range low address
ALIGN	0x0000001f	0x0	Burst size alignment bits

Register RANGEH2

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Second range high address register

Reset value

0x0000001f

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RHADDR																											ALIGN			
rw																											ro			
0																											31			

Field	Mask	Reset	Description
RHADDR	`0xffffffe0`	`0x0`	Scrubber range high address
ALIGN	`0x0000001f`	`0x1f`	Burst size alignment bits

Commands

Name	Description
delete	Dispose instance of MEMSCRUB

9.24.5. Limitations

The device is non-functional, in that it only provides registers for reading and writing.

To inject scrubbing errors, set the registers with a fault injection model, and raise any corresponding interrupt manually.

9.25. MMCTRL

The MMCTRL device is part of the GRLIB IP library. It is available in `libTEMUMMCTRL.so`.

9.25.1. Loading the Plugin

```
import MMCTRL
```

9.25.2. Configuration

9.25.3. @MMCTRL Reference

Properties

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @MMCTRL
new	Create new instance of MMCTRL

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.25.4. MMCTRL Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
FTBND	uint32_t	FT boundary address register
FTBNDColdResetValue	uint32_t	FT boundary address register
FTBNDForcedBits	uint32_t	FT boundary address register
FTBNDForcedFlippedBits	uint32_t	FT boundary address register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
FTBNDReadMask	uint32_t	FT boundary address register
FTBNDResetMask	uint32_t	FT boundary address register
FTBNDResetValue	uint32_t	FT boundary address register
FTBNDWriteMask	uint32_t	FT boundary address register
FTDA	uint32_t	FT diagnostic address register
FTDAColdResetValue	uint32_t	FT diagnostic address register
FTDAForcedBits	uint32_t	FT diagnostic address register
FTDAForcedFlippedBits	uint32_t	FT diagnostic address register
FTDAReadMask	uint32_t	FT diagnostic address register
FTDAResetMask	uint32_t	FT diagnostic address register
FTDAResetValue	uint32_t	FT diagnostic address register
FTDAWriteMask	uint32_t	FT diagnostic address register
FTDC	uint32_t	FT diagnostic checkbits register
FTDCColdResetValue	uint32_t	FT diagnostic checkbits register
FTDCForcedBits	uint32_t	FT diagnostic checkbits register
FTDCForcedFlippedBits	uint32_t	FT diagnostic checkbits register
FTDCReadMask	uint32_t	FT diagnostic checkbits register
FTDCResetMask	uint32_t	FT diagnostic checkbits register
FTDCResetValue	uint32_t	FT diagnostic checkbits register
FTDCWriteMask	uint32_t	FT diagnostic checkbits register
FTDD	uint32_t	FT diagnostic data register
FTDDColdResetValue	uint32_t	FT diagnostic data register
FTDDForcedBits	uint32_t	FT diagnostic data register
FTDDForcedFlippedBits	uint32_t	FT diagnostic data register
FTDDReadMask	uint32_t	FT diagnostic data register
FTDDResetMask	uint32_t	FT diagnostic data register
FTDDResetValue	uint32_t	FT diagnostic data register
FTDDWriteMask	uint32_t	FT diagnostic data register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LoggingFlags	uint64_t	Flags for logging info
MUXCFG	uint32_t	Mux configuration register
MUXCFGColdResetValue	uint32_t	Mux configuration register
MUXCFGForcedBits	uint32_t	Mux configuration register
MUXCFGForcedFlippedBits	uint32_t	Mux configuration register
MUXCFGReadMask	uint32_t	Mux configuration register
MUXCFGResetMask	uint32_t	Mux configuration register
MUXCFGResetValue	uint32_t	Mux configuration register
MUXCFGWriteMask	uint32_t	Mux configuration register
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
SDCFG	[uint32_t; 2]	SDRAM configuration register
TimeSource	*void	Time source object
ahb.pnp.bar	[uint32_t; 4]	AMBA plug and play base address register
ahb.pnp.identReg	uint32_t	AMBA plug and play config word
ahb.pnp.userDef	[uint32_t; 3]	AMBA plug and play user words
config.littleEndian	uint8_t	Endianess of memory interface.

Interfaces

Name	Type	Description
AhbIface	AhbIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Registers



Register support is currently experimental!

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register Bank Regs

Register MUXCFG

Description

Mux configuration register

Reset value

0x00001000

Warm reset mask

0xfffff0ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERRLOC												DERR	DWIDTH			BEID				-				DATAMUX			CEM	BAUPD	BAEN	CODE	EDEN	
ro												ro	ro			ro				-				rw			rw	rw	rw	rw	rw	
0												0	0			1				-				0			0	0	0	0	0	

Field	Mask	Reset	Description
ERRLOC	0xfff00000	0x0	Diagnostic data read error location
DERR	0x00080000	0x0	Last diagnostic data read contained an uncorrectable error
DWIDTH	0x00070000	0x0	Data width
BEID	0x0000f000	0x1	Back-end identifier
DATAMUX	0x000000e0	0x0	Data mux control
CEM	0x00000010	0x0	Correctable error masking
BAUPD	0x00000008	0x0	Enable automatic boundary shifting on write
BAEN	0x00000004	0x0	Enable the code boundary
CODE	0x00000002	0x0	Code selection
EDEN	0x00000001	0x0	EDAC enable

Register FTDA

Description

FT diagnostic address register

Reset value

0x00000000

Warm reset mask

0xfffffffc

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FTDA																														-	
rw																														-	
0																														-	

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
FTDA	0xfffffffc	0x0	Address to memory location for checkbit read/write

Register FTDC

Description

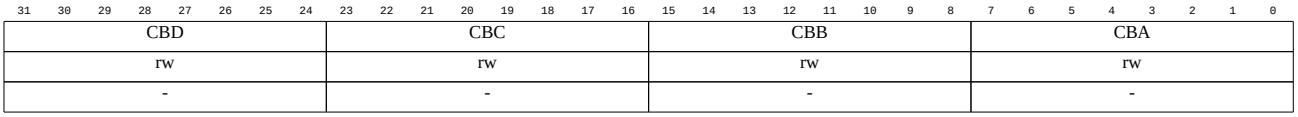
FT diagnostic checkbits register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
CBD	0xff000000	-	Checkbits for part D of 64-bit data word
CBC	0x00ff0000	-	Checkbits for part C of 64-bit data word
CBB	0x0000ff00	-	Checkbits for part B of 64-bit data word
CBA	0x000000ff	-	Checkbits for part A of 64-bit data word

Register FTDD

Description

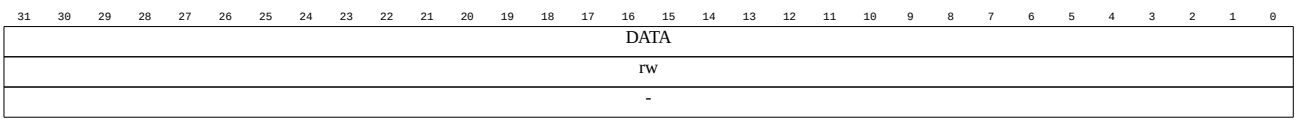
FT diagnostic data register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
DATA	0xffffffff	-	Uncorrected data

Register FTBND

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

FT boundary address register

Reset value

0x00000000

Warm reset mask

0xfffffff8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FTBND																													-		
rw																													-		
0																													-		

Field	Mask	Reset	Description
FTBND	0xfffffff8	0x0	Code boundary address

Register SDCFG1

Description

SDRAM configuration register

Reset value

0x7c400000

Warm reset mask

0xfffdfffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RF	tRP	tRFC			tC	BANKSZ			COLSZ		COMMAND			-	MS	64	RFLOAD															
rw	rw	rw			rw	rw			rw		rw			-	ro	ro	rw														
0	1	7			1	0			2		0			-	0	0	0														

Field	Mask	Reset	Description
RF	0x80000000	0x0	SDRAM refresh
tRP	0x40000000	0x1	SDRAM tRP timing
tRFC	0x38000000	0x7	SDRAM tRFC timing
tC	0x04000000	0x1	SDRAM CAS delay
BANKSZ	0x03800000	0x0	SDRAM banks size
COLSZ	0x00600000	0x2	SDRAM column size
COMMAND	0x001c0000	0x0	SDRAM command
MS	0x00010000	0x0	Mobile SDRAM support
64	0x00008000	0x0	64-bit data bus
RFLOAD	0x00007fff	0x0	Refresh counter reload value

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Register SDCFG2

Description

SDRAM configuration register 2

Reset value

0x40000000

Warm reset mask

0x4000e000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	CE	-														EN2T	DCS	BPARK	-												
-	rw	-														rw	rw	rw	-												
-	1	-														0	0	0	-												

Field	Mask	Reset	Description
CE	0x40000000	0x1	Clock enable
EN2T	0x00008000	0x0	Enable 2T signaling
DCS	0x00004000	0x0	Double chip select mode
BPARK	0x00002000	0x0	Bus parking enable

Commands

Name	Description
delete	Dispose instance of MMCTRL

9.25.5. Limitations

The MMCTRL device is non-functional, providing only registers and PNP data. To raise memory controller errors, the users is expected to implement a fault injection model, which sets the registers and raises relevant interrupts.

9.26. GRCANFD

The GRCANFD model is available in the GRCANFD plugin.

9.26.1. Loading the Plugin

```
import GRCANFD
```

9.26.2. Configuration

9.26.3. @GRCANFD Reference

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GRCANFD
new	Create new instance of GRCANFD

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.26.4. GRCANFD Reference

Properties

Name	Type	Description
CAP	uint32_t	Capability Register
CAPColdResetValue	uint32_t	Capability Register
CAPForcedBits	uint32_t	Capability Register
CAPForcedFlippedBits	uint32_t	Capability Register
CAPReadMask	uint32_t	Capability Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
CAPResetMask	uint32_t	Capability Register
CAPResetValue	uint32_t	Capability Register
CAPWriteMask	uint32_t	Capability Register
COCTRL	uint32_t	CANOpen Control Register
COCTRLColdResetValue	uint32_t	CANOpen Control Register
COCTRLForcedBits	uint32_t	CANOpen Control Register
COCTRLForcedFlippedBits	uint32_t	CANOpen Control Register
COCTRLReadMask	uint32_t	CANOpen Control Register
COCTRLResetMask	uint32_t	CANOpen Control Register
COCTRLResetValue	uint32_t	CANOpen Control Register
COCTRLWriteMask	uint32_t	CANOpen Control Register
COHBCT	uint32_t	CANOpen Heartbeat Count Register
COHBCTColdResetValue	uint32_t	CANOpen Heartbeat Count Register
COHBCTForcedBits	uint32_t	CANOpen Heartbeat Count Register
COHBCTForcedFlippedBits	uint32_t	CANOpen Heartbeat Count Register
COHBCTReadMask	uint32_t	CANOpen Heartbeat Count Register
COHBCTResetMask	uint32_t	CANOpen Heartbeat Count Register
COHBCTResetValue	uint32_t	CANOpen Heartbeat Count Register
COHBCTWriteMask	uint32_t	CANOpen Heartbeat Count Register
COHBTO	uint32_t	CANOpen Heartbeat Timeout Register
COHBTOColdResetValue	uint32_t	CANOpen Heartbeat Timeout Register
COHBTOForcedBits	uint32_t	CANOpen Heartbeat Timeout Register
COHBTOForcedFlippedBits	uint32_t	CANOpen Heartbeat Timeout Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
COHBTOReadMask	uint32_t	CANOpen Heartbeat Timeout Register
COHBTOResetMask	uint32_t	CANOpen Heartbeat Timeout Register
COHBTOResetValue	uint32_t	CANOpen Heartbeat Timeout Register
COHBTOWriteMask	uint32_t	CANOpen Heartbeat Timeout Register
CONF	uint32_t	Configuration Register
CONFColdResetValue	uint32_t	Configuration Register
CONFForcedBits	uint32_t	Configuration Register
CONFForcedFlippedBits	uint32_t	Configuration Register
CONFReadMask	uint32_t	Configuration Register
CONFResetMask	uint32_t	Configuration Register
CONFResetValue	uint32_t	Configuration Register
CONFWriteMask	uint32_t	Configuration Register
COSTS	uint32_t	CANOpen Status Register
COSTSColdResetValue	uint32_t	CANOpen Status Register
COSTSForcedBits	uint32_t	CANOpen Status Register
COSTSForcedFlippedBits	uint32_t	CANOpen Status Register
COSTSReadMask	uint32_t	CANOpen Status Register
COSTSResetMask	uint32_t	CANOpen Status Register
COSTSResetValue	uint32_t	CANOpen Status Register
COSTSWriteMask	uint32_t	CANOpen Status Register
CTRL	uint32_t	Control Register
CTRLColdResetValue	uint32_t	Control Register
CTRLForcedBits	uint32_t	Control Register
CTRLForcedFlippedBits	uint32_t	Control Register
CTRLReadMask	uint32_t	Control Register
CTRLResetMask	uint32_t	Control Register
CTRLResetValue	uint32_t	Control Register
CTRLWriteMask	uint32_t	Control Register
Class	*void	Class object

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Name	Type	Description
Component	*void	Pointer to component object if part of component
DATABR	uint32_t	Data Bit-Rate Configuration Register
DATABRColdResetValue	uint32_t	Data Bit-Rate Configuration Register
DATABRForcedBits	uint32_t	Data Bit-Rate Configuration Register
DATABRForcedFlippedBits	uint32_t	Data Bit-Rate Configuration Register
DATABRReadMask	uint32_t	Data Bit-Rate Configuration Register
DATABRResetMask	uint32_t	Data Bit-Rate Configuration Register
DATABRResetValue	uint32_t	Data Bit-Rate Configuration Register
DATABRWriteMask	uint32_t	Data Bit-Rate Configuration Register
DELCOMP	uint32_t	Transmitter Delay Compensation Register
DELCOMPColdResetValue	uint32_t	Transmitter Delay Compensation Register
DELCOMPForcedBits	uint32_t	Transmitter Delay Compensation Register
DELCOMPForcedFlippedBits	uint32_t	Transmitter Delay Compensation Register
DELCOMPReadMask	uint32_t	Transmitter Delay Compensation Register
DELCOMPResetMask	uint32_t	Transmitter Delay Compensation Register
DELCOMPResetValue	uint32_t	Transmitter Delay Compensation Register
DELCOMPWriteMask	uint32_t	Transmitter Delay Compensation Register

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Name	Type	Description
DescriptorBuffer	temu_Buff	Internal: Descriptors already received but not fitting inside the memory-mapped RX circular buffer
IM	uint32_t	Interrupt Mask Register
IMColdResetValue	uint32_t	Interrupt Mask Register
IMForcedBits	uint32_t	Interrupt Mask Register
IMForcedFlippedBits	uint32_t	Interrupt Mask Register
IMReadMask	uint32_t	Interrupt Mask Register
IMResetMask	uint32_t	Interrupt Mask Register
IMResetValue	uint32_t	Interrupt Mask Register
IMWriteMask	uint32_t	Interrupt Mask Register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
NOMBR	uint32_t	Nominal Bit-Rate Configuration Register
NOMBRColdResetValue	uint32_t	Nominal Bit-Rate Configuration Register
NOMBRForcedBits	uint32_t	Nominal Bit-Rate Configuration Register
NOMBRForcedFlippedBits	uint32_t	Nominal Bit-Rate Configuration Register
NOMBRReadMask	uint32_t	Nominal Bit-Rate Configuration Register
NOMBRResetMask	uint32_t	Nominal Bit-Rate Configuration Register
NOMBRResetValue	uint32_t	Nominal Bit-Rate Configuration Register
NOMBRWriteMask	uint32_t	Nominal Bit-Rate Configuration Register
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
PI	uint32_t	Pending Interrupt Register

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Name	Type	Description
PIColdResetValue	uint32_t	Pending Interrupt Register
PIForcedBits	uint32_t	Pending Interrupt Register
PIForcedFlippedBits	uint32_t	Pending Interrupt Register
PIReadMask	uint32_t	Pending Interrupt Register
PIResetMask	uint32_t	Pending Interrupt Register
PIResetValue	uint32_t	Pending Interrupt Register
PIWriteMask	uint32_t	Pending Interrupt Register
PendingCANOpenResponses	temu_Buff	Internal: Pending CANOpen Read PDO responses
RXADDR	uint32_t	Receive Channel Address Register
RXADDRColdResetValue	uint32_t	Receive Channel Address Register
RXADDRForcedBits	uint32_t	Receive Channel Address Register
RXADDRForcedFlippedBits	uint32_t	Receive Channel Address Register
RXADDRReadMask	uint32_t	Receive Channel Address Register
RXADDRResetMask	uint32_t	Receive Channel Address Register
RXADDRResetValue	uint32_t	Receive Channel Address Register
RXADDRWriteMask	uint32_t	Receive Channel Address Register
RXCODE	uint32_t	Receive Channel Acceptance Code Register
RXCODEColdResetValue	uint32_t	Receive Channel Acceptance Code Register
RXCODEForcedBits	uint32_t	Receive Channel Acceptance Code Register
RXCODEForcedFlippedBits	uint32_t	Receive Channel Acceptance Code Register
RXCODEReadMask	uint32_t	Receive Channel Acceptance Code Register

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Name	Type	Description
RXCODEResetMask	uint32_t	Receive Channel Acceptance Code Register
RXCODEResetValue	uint32_t	Receive Channel Acceptance Code Register
RXCODEWriteMask	uint32_t	Receive Channel Acceptance Code Register
RXCTRL	uint32_t	Receive Channel Control Register
RXCTRLColdResetValue	uint32_t	Receive Channel Control Register
RXCTRLForcedBits	uint32_t	Receive Channel Control Register
RXCTRLForcedFlippedBits	uint32_t	Receive Channel Control Register
RXCTRLReadMask	uint32_t	Receive Channel Control Register
RXCTRLResetMask	uint32_t	Receive Channel Control Register
RXCTRLResetValue	uint32_t	Receive Channel Control Register
RXCTRLWriteMask	uint32_t	Receive Channel Control Register
RXIRQ	uint32_t	Receive Channel Interrupt Register
RXIRQColdResetValue	uint32_t	Receive Channel Interrupt Register
RXIRQForcedBits	uint32_t	Receive Channel Interrupt Register
RXIRQForcedFlippedBits	uint32_t	Receive Channel Interrupt Register
RXIRQReadMask	uint32_t	Receive Channel Interrupt Register
RXIRQResetMask	uint32_t	Receive Channel Interrupt Register
RXIRQResetValue	uint32_t	Receive Channel Interrupt Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
RXIRQWriteMask	uint32_t	Receive Channel Interrupt Register
RXMASK	uint32_t	Receive Channel Acceptance Mask Register
RXMASKColdResetValue	uint32_t	Receive Channel Acceptance Mask Register
RXMASKForcedBits	uint32_t	Receive Channel Acceptance Mask Register
RXMASKForcedFlippedBits	uint32_t	Receive Channel Acceptance Mask Register
RXMASKReadMask	uint32_t	Receive Channel Acceptance Mask Register
RXMASKResetMask	uint32_t	Receive Channel Acceptance Mask Register
RXMASKResetValue	uint32_t	Receive Channel Acceptance Mask Register
RXMASKWriteMask	uint32_t	Receive Channel Acceptance Mask Register
RXRD	uint32_t	Receive Channel Read Register
RXRDColdResetValue	uint32_t	Receive Channel Read Register
RXRDForcedBits	uint32_t	Receive Channel Read Register
RXRDForcedFlippedBits	uint32_t	Receive Channel Read Register
RXRDReadMask	uint32_t	Receive Channel Read Register
RXRDResetMask	uint32_t	Receive Channel Read Register
RXRDResetValue	uint32_t	Receive Channel Read Register
RXRDWriteMask	uint32_t	Receive Channel Read Register
RXSIZE	uint32_t	Receive Channel Size Register
RXSIZEColdResetValue	uint32_t	Receive Channel Size Register
RXSIZEForcedBits	uint32_t	Receive Channel Size Register
RXSIZEForcedFlippedBits	uint32_t	Receive Channel Size Register
RXSIZEReadMask	uint32_t	Receive Channel Size Register
RXSIZEResetMask	uint32_t	Receive Channel Size Register
RXSIZEResetValue	uint32_t	Receive Channel Size Register
RXSIZEWriteMask	uint32_t	Receive Channel Size Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
RXWR	uint32_t	Receive Channel Write Register
RXWRColdResetValue	uint32_t	Receive Channel Write Register
RXWRForcedBits	uint32_t	Receive Channel Write Register
RXWRForcedFlippedBits	uint32_t	Receive Channel Write Register
RXWRReadMask	uint32_t	Receive Channel Write Register
RXWRResetMask	uint32_t	Receive Channel Write Register
RXWRResetValue	uint32_t	Receive Channel Write Register
RXWRWriteMask	uint32_t	Receive Channel Write Register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
STAT	uint32_t	Status Register
STATColdResetValue	uint32_t	Status Register
STATForcedBits	uint32_t	Status Register
STATForcedFlippedBits	uint32_t	Status Register
STATReadMask	uint32_t	Status Register
STATResetMask	uint32_t	Status Register
STATResetValue	uint32_t	Status Register
STATWriteMask	uint32_t	Status Register
SYNCCODE	uint32_t	SYNC Code Filter Register
SYNCCODEColdResetValue	uint32_t	SYNC Code Filter Register
SYNCCODEForcedBits	uint32_t	SYNC Code Filter Register
SYNCCODEForcedFlippedBits	uint32_t	SYNC Code Filter Register
SYNCCODEReadMask	uint32_t	SYNC Code Filter Register
SYNCCODEResetMask	uint32_t	SYNC Code Filter Register
SYNCCODEResetValue	uint32_t	SYNC Code Filter Register
SYNCCODEWriteMask	uint32_t	SYNC Code Filter Register
SYNCMASK	uint32_t	SYNC Mask Filter Register
SYNCMASKColdResetValue	uint32_t	SYNC Mask Filter Register
SYNCMASKForcedBits	uint32_t	SYNC Mask Filter Register
SYNCMASKForcedFlippedBits	uint32_t	SYNC Mask Filter Register
SYNCMASKReadMask	uint32_t	SYNC Mask Filter Register
SYNCMASKResetMask	uint32_t	SYNC Mask Filter Register

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Name	Type	Description
SYNCMASKResetValue	uint32_t	SYNC Mask Filter Register
SYNCMASKWriteMask	uint32_t	SYNC Mask Filter Register
TXADDR	uint32_t	Transmit Channel Address Register
TXADDRColdResetValue	uint32_t	Transmit Channel Address Register
TXADDRForcedBits	uint32_t	Transmit Channel Address Register
TXADDRForcedFlippedBits	uint32_t	Transmit Channel Address Register
TXADDRReadMask	uint32_t	Transmit Channel Address Register
TXADDRResetMask	uint32_t	Transmit Channel Address Register
TXADDRResetValue	uint32_t	Transmit Channel Address Register
TXADDRWriteMask	uint32_t	Transmit Channel Address Register
TXCTRL	uint32_t	Transmit Channel Control Register
TXCTRLColdResetValue	uint32_t	Transmit Channel Control Register
TXCTRLForcedBits	uint32_t	Transmit Channel Control Register
TXCTRLForcedFlippedBits	uint32_t	Transmit Channel Control Register
TXCTRLReadMask	uint32_t	Transmit Channel Control Register
TXCTRLResetMask	uint32_t	Transmit Channel Control Register
TXCTRLResetValue	uint32_t	Transmit Channel Control Register
TXCTRLWriteMask	uint32_t	Transmit Channel Control Register
TXIRQ	uint32_t	Transmit Channel Interrupt Register

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Name	Type	Description
TXIRQColdResetValue	uint32_t	Transmit Channel Interrupt Register
TXIRQForcedBits	uint32_t	Transmit Channel Interrupt Register
TXIRQForcedFlippedBits	uint32_t	Transmit Channel Interrupt Register
TXIRQReadMask	uint32_t	Transmit Channel Interrupt Register
TXIRQResetMask	uint32_t	Transmit Channel Interrupt Register
TXIRQResetValue	uint32_t	Transmit Channel Interrupt Register
TXIRQWriteMask	uint32_t	Transmit Channel Interrupt Register
TXRD	uint32_t	Transmit Channel Read Register
TXRDColdResetValue	uint32_t	Transmit Channel Read Register
TXRDForcedBits	uint32_t	Transmit Channel Read Register
TXRDForcedFlippedBits	uint32_t	Transmit Channel Read Register
TXRDReadMask	uint32_t	Transmit Channel Read Register
TXRDResetMask	uint32_t	Transmit Channel Read Register
TXRDResetValue	uint32_t	Transmit Channel Read Register
TXRDWriteMask	uint32_t	Transmit Channel Read Register
TXSIZE	uint32_t	Transmit Channel Size Register
TXSIZEColdResetValue	uint32_t	Transmit Channel Size Register
TXSIZEForcedBits	uint32_t	Transmit Channel Size Register
TXSIZEForcedFlippedBits	uint32_t	Transmit Channel Size Register
TXSIZEReadMask	uint32_t	Transmit Channel Size Register
TXSIZEResetMask	uint32_t	Transmit Channel Size Register
TXSIZEResetValue	uint32_t	Transmit Channel Size Register
TXSIZEWriteMask	uint32_t	Transmit Channel Size Register
TXWR	uint32_t	Transmit Channel Write Register
TXWRColdResetValue	uint32_t	Transmit Channel Write Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
TXWRForcedBits	uint32_t	Transmit Channel Write Register
TXWRForcedFlippedBits	uint32_t	Transmit Channel Write Register
TXWRReadMask	uint32_t	Transmit Channel Write Register
TXWRResetMask	uint32_t	Transmit Channel Write Register
TXWRResetValue	uint32_t	Transmit Channel Write Register
TXWRWriteMask	uint32_t	Transmit Channel Write Register
TimeSource	*void	Time source object
bus	temu_IfaceRef/ <unknown>	CAN (FD) bus.
config.infiniteBusSpeed	uint8_t	Send next CAN-FD frame without delay.
config.irq	uint8_t	Interrupt number
config.littleEndian	uint8_t	Endianess of memory interface.
config.singleIrq	uint8_t	Single interrupt
irqCtrl	temu_IfaceRef/ <unknown>	IRQ controller.
memAccess	temu_IfaceRef/ <unknown>	Memory Interface for DMA containing underlying buffers.
pnp.bar	uint32_t	AMBA plug and play base address register
pnp.config	uint32_t	AMBA plug and play config word

Interfaces

Name	Type	Description
ApbIface	ApbIface	APB P&P interface.
CanDevIface	CanDevIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.

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Registers



Register support is currently experimental!

Register Bank Regs

Register CONF

Description

Configuration Register

Reset value

0x00000000

Warm reset mask

0x000000df

31 … 8	7	6	5	4	3	2	1	0
-	LBS	LB	-	SILENT	SELECT	ENABLE1	ENABLE0	ABORT
-	rw	rw	-	rw	rw	rw	rw	rw
-	0	0	-	0	0	0	0	0

Field	Mask	Reset	Description
LBS	0x00000080	0x0	Loopback single-shot
LB	0x00000040	0x0	Loopback
SILENT	0x00000010	0x0	Silent mode
SELECT	0x00000008	0x0	Bus select
ENABLE1	0x00000004	0x0	Enable bus 1
ENABLE0	0x00000002	0x0	Enable bus 0
ABORT	0x00000001	0x0	Abort ongoing transfer

Register STAT

Description

Status Register

Reset value

0x00000000

Warm reset mask

0x00ffff3f

31 … 24	23 … 16	15 … 8	7 … 6	5	4	3	2	1	0
-	TxErrCntr	RxErrCntr	-	MDA	ACTIVE	EMErr	OR	BusOff	ErrPas
-	ro	ro	-	ro	ro	ro	ro	ro	ro
-	0	0	-	0	0	0	0	0	0

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Field	Mask	Reset	Description
TxErrCntr	0x00ff0000	0x0	Transmit error counter
RxErrCntr	0x0000ff00	0x0	Receive error counter
MD	0x00000020	0x0	Multiple descriptors
ACTIVE	0x00000010	0x0	Active
BMErr	0x00000008	0x0	Bus master error
OR	0x00000004	0x0	Overrun
BusOff	0x00000002	0x0	Bus off
ErrPass	0x00000001	0x0	Error passive

Register CTRL

Description

Control Register

Reset value

0x00000000

Warm reset mask

0x00000001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																														RESET	ENABL
-																														wo	rw
-																														-	0

Field	Mask	Reset	Description
RESET	0x00000002	-	Reset
ENABLE	0x00000001	0x0	Enable

Register CAP

Description

Capability Register

Reset value

0xc0000112

Warm reset mask

0xc0000777

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rev1	Rev2	-																			TxBufSize			-	RxBufSize			-	SepBus	SOpSm	SingIR
ro	ro	-																			ro			-	ro			-	ro	ro	ro
1	1	-																			1			-	1			-	0	1	0

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Field	Mask	Reset	Description
Rev1	0x80000000	0x1	Revision bit 1
Rev2	0x40000000	0x1	Revision bit 2
TxBufSize	0x00000700	0x1	Transmit buffer size
RxBufSize	0x00000070	0x1	Receive buffer size
SepBus	0x00000004	0x0	Separate CAN buses
COpen	0x00000002	0x1	CANOpen support
SingIRQ	0x00000001	0x0	Single IRQ support

Register SYNCMASK

Description

SYNC Mask Filter Register

Reset value

0x1fffffff

Warm reset mask

0x1fffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	MASK																														
-	rw																														
-	536870911																														

Field	Mask	Reset	Description
MASK	0x1fffffff	0x1fffffff	SYNC mask

Register SYNCCODE

Description

SYNC Code Filter Register

Reset value

0x00000000

Warm reset mask

0x1fffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	CODE																														
-	rw																														
-	0																														

Field	Mask	Reset	Description
CODE	0x1fffffff	0x0	SYNC code

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Register NOMBR

Description

Nominal Bit-Rate Configuration Register

Reset value

0x00000000

Warm reset mask

0x00ffffff

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8 7 6 5 4	3 2 1 0
-	SCALER	PS1	PS2	SJW
-	rw	rw	rw	rw
-	0	0	0	0

Field	Mask	Reset	Description
SCALER	0x00ff0000	0x0	Prescaler
PS1	0x0000fc00	0x0	Phase segment 1
PS2	0x000003f0	0x0	Phase segment 2
SJW	0x0000000f	0x0	Synchronization jump width

Register DATABR

Description

Data Bit-Rate Configuration Register

Reset value

0x00000000

Warm reset mask

0x00ff3def

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12 11 10	9	8 7 6 5	4	3 2 1 0
-	SCALER	-	PS1	-	PS2	-	SJW
-	rw	-	rw	-	rw	-	rw
-	0	-	0	-	0	-	0

Field	Mask	Reset	Description
SCALER	0x00ff0000	0x0	Prescaler
PS1	0x00003c00	0x0	Phase segment 1
PS2	0x000001e0	0x0	Phase segment 2
SJW	0x0000000f	0x0	Synchronization jump width

Register DELCOMP

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Transmitter Delay Compensation Register

Reset value

0x00000000

Warm reset mask

0x0000003f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																												TxCompVal			
-																												rw			
-																												0			

Field	Mask	Reset	Description
TxCompVal	0x0000003f	0x0	Transmitter delay compensation value

Register COCTRL

Description

CANOpen Control Register

Reset value

0x000007f0

Warm reset mask

0x000007f7

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																					ID							-	RC	SS	EN
-																					rw							-	rw	rw	rw
-																					127							-	0	0	0

Field	Mask	Reset	Description
ID	0x000007f0	0x7f	CANOpen node ID
RC	0x00000004	0x0	Remote command
SS	0x00000002	0x0	SYNC single-shot
EN	0x00000001	0x0	CANOpen enable

Register COHBTO

Description

CANOpen Heartbeat Timeout Register

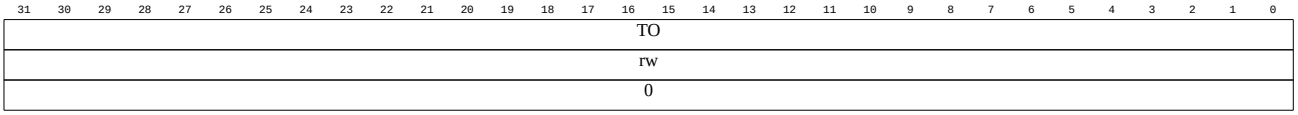
Reset value

0x00000000

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Warm reset mask

0xffffffff



Field	Mask	Reset	Description
TO	0xffffffff	0x0	Heartbeat timeout

Register COHBCT

Description

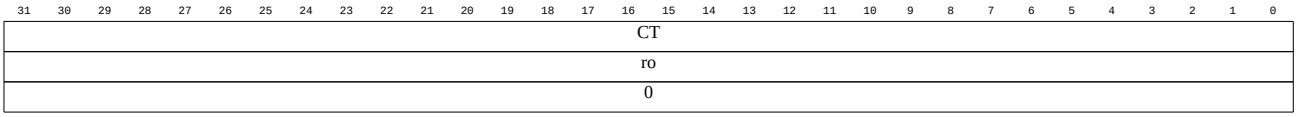
CANOpen Heartbeat Count Register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
CT	0xffffffff	0x0	Heartbeat count

Register COSTS

Description

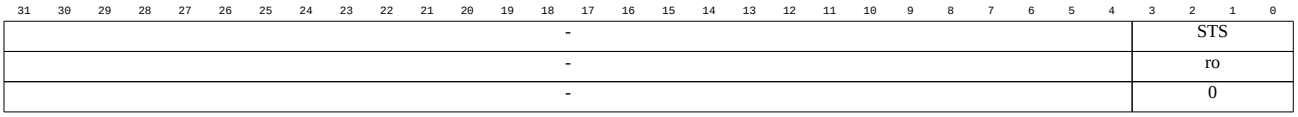
CANOpen Status Register

Reset value

0x00000000

Warm reset mask

0x0000000f



Field	Mask	Reset	Description
STS	0x0000000f	0x0	CANOpen status

Register PIMS

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Pending Interrupt Masked Status Register

Reset value

0x00000000

Warm reset mask

0x001fffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-											COHbErr	COSync	COWrCmd	CORdCmd	TxLoss	RxMiss	TxErrCntr	RxErrCntr	TxSync	RxSync	Tx	Rx	TxEmpty	RxFull	TxIRQ	RxIRQ	BmRdErr	BmWrErr	OR	Off	Pass
-											ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro
-											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
COHbErr	0x00100000	0x0	CANOpen heartbeat error
COSync	0x00080000	0x0	CANOpen SYNC message
COWrCmd	0x00040000	0x0	CANOpen write command
CORdCmd	0x00020000	0x0	CANOpen read command
TxLoss	0x00010000	0x0	Transmit loss
RxMiss	0x00008000	0x0	Receive miss
TxErrCntr	0x00004000	0x0	Transmit error counter threshold
RxErrCntr	0x00002000	0x0	Receive error counter threshold
TxSync	0x00001000	0x0	Transmit synchronization
RxSync	0x00000800	0x0	Receive synchronization
Tx	0x00000400	0x0	Transmit complete
Rx	0x00000200	0x0	Receive complete
TxEmpty	0x00000100	0x0	Transmit channel empty
RxFull	0x00000080	0x0	Receive channel full
TxIRQ	0x00000040	0x0	Transmit channel interrupt
RxIRQ	0x00000020	0x0	Receive channel interrupt
BmRdErr	0x00000010	0x0	Bus master read error
BmWrErr	0x00000008	0x0	Bus master write error
OR	0x00000004	0x0	Overrun
Off	0x00000002	0x0	Bus off
Pass	0x00000001	0x0	Error passive

Register PIM

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Pending Interrupt Masked Register

Reset value

0x00000000

Warm reset mask

0x001fffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-											COHbErr	COSync	COWrCmd	CORdCmd	TxLoss	RxMiss	TxErrCntr	RxErrCntr	TxSync	RxSync	Tx	Rx	TxEmpty	RxFull	TxIRQ	RxIRQ	BmRdErr	BmWrErr	OR	Off	Pass
-											ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro
-											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
COHbErr	0x00100000	0x0	CANOpen heartbeat error
COSync	0x00080000	0x0	CANOpen SYNC message
COWrCmd	0x00040000	0x0	CANOpen write command
CORdCmd	0x00020000	0x0	CANOpen read command
TxLoss	0x00010000	0x0	Transmit loss
RxMiss	0x00008000	0x0	Receive miss
TxErrCntr	0x00004000	0x0	Transmit error counter threshold
RxErrCntr	0x00002000	0x0	Receive error counter threshold
TxSync	0x00001000	0x0	Transmit synchronization
RxSync	0x00000800	0x0	Receive synchronization
Tx	0x00000400	0x0	Transmit complete
Rx	0x00000200	0x0	Receive complete
TxEmpty	0x00000100	0x0	Transmit channel empty
RxFull	0x00000080	0x0	Receive channel full
TxIRQ	0x00000040	0x0	Transmit channel interrupt
RxIRQ	0x00000020	0x0	Receive channel interrupt
BmRdErr	0x00000010	0x0	Bus master read error
BmWrErr	0x00000008	0x0	Bus master write error
OR	0x00000004	0x0	Overrun
Off	0x00000002	0x0	Bus off
Pass	0x00000001	0x0	Error passive

Register PIS

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Pending Interrupt Status Register

Reset value

0x00000000

Warm reset mask

0x001fffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-											COHbErr	COSync	COWrCmd	CORdCmd	TxLoss	RxMiss	TxErrCntr	RxErrCntr	TxSync	RxSync	Tx	Rx	TxEmpty	RxFull	TxIRQ	RxIRQ	BmRdErr	BmWrErr	OR	Off	Pass
-											ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro
-											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
COHbErr	0x00100000	0x0	CANOpen heartbeat error
COSync	0x00080000	0x0	CANOpen SYNC message
COWrCmd	0x00040000	0x0	CANOpen write command
CORdCmd	0x00020000	0x0	CANOpen read command
TxLoss	0x00010000	0x0	Transmit loss
RxMiss	0x00008000	0x0	Receive miss
TxErrCntr	0x00004000	0x0	Transmit error counter threshold
RxErrCntr	0x00002000	0x0	Receive error counter threshold
TxSync	0x00001000	0x0	Transmit synchronization
RxSync	0x00000800	0x0	Receive synchronization
Tx	0x00000400	0x0	Transmit complete
Rx	0x00000200	0x0	Receive complete
TxEmpty	0x00000100	0x0	Transmit channel empty
RxFull	0x00000080	0x0	Receive channel full
TxIRQ	0x00000040	0x0	Transmit channel interrupt
RxIRQ	0x00000020	0x0	Receive channel interrupt
BmRdErr	0x00000010	0x0	Bus master read error
BmWrErr	0x00000008	0x0	Bus master write error
OR	0x00000004	0x0	Overrun
Off	0x00000002	0x0	Bus off
Pass	0x00000001	0x0	Error passive

Register PI

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Pending Interrupt Register

Reset value

0x00000000

Warm reset mask

0x001fffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-											COHbErr	COSync	COWrCmd	CORdCmd	TxLoss	RxMiss	TxErrCntr	RxErrCntr	TxSync	RxSync	Tx	Rx	TxEmpty	RxFull	TxIRQ	RxIRQ	BmRdErr	BmWrErr	OR	Off	Pass
-											rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
COHbErr	0x00100000	0x0	CANOpen heartbeat error
COSync	0x00080000	0x0	CANOpen SYNC message
COWrCmd	0x00040000	0x0	CANOpen write command
CORdCmd	0x00020000	0x0	CANOpen read command
TxLoss	0x00010000	0x0	Transmit loss
RxMiss	0x00008000	0x0	Receive miss
TxErrCntr	0x00004000	0x0	Transmit error counter threshold
RxErrCntr	0x00002000	0x0	Receive error counter threshold
TxSync	0x00001000	0x0	Transmit synchronization
RxSync	0x00000800	0x0	Receive synchronization
Tx	0x00000400	0x0	Transmit complete
Rx	0x00000200	0x0	Receive complete
TxEmpty	0x00000100	0x0	Transmit channel empty
RxFull	0x00000080	0x0	Receive channel full
TxIRQ	0x00000040	0x0	Transmit channel interrupt
RxIRQ	0x00000020	0x0	Receive channel interrupt
BmRdErr	0x00000010	0x0	Bus master read error
BmWrErr	0x00000008	0x0	Bus master write error
OR	0x00000004	0x0	Overrun
Off	0x00000002	0x0	Bus off
Pass	0x00000001	0x0	Error passive

Register IM

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Interrupt Mask Register

Reset value

0x00000000

Warm reset mask

0x001fffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-											COHbErr	COSync	COWrCmd	CORdCmd	TxLoss	RxMiss	TxErrCntr	RxErrCntr	TxSync	RxSync	Tx	Rx	TxEmpty	RxFull	TxIRQ	RxIRQ	BmRdErr	BmWrErr	OR	Off	Pass
-											rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Mask	Reset	Description
COHbErr	0x00100000	0x0	CANOpen heartbeat error
COSync	0x00080000	0x0	CANOpen SYNC message
COWrCmd	0x00040000	0x0	CANOpen write command
CORdCmd	0x00020000	0x0	CANOpen read command
TxLoss	0x00010000	0x0	Transmit loss
RxMiss	0x00008000	0x0	Receive miss
TxErrCntr	0x00004000	0x0	Transmit error counter threshold
RxErrCntr	0x00002000	0x0	Receive error counter threshold
TxSync	0x00001000	0x0	Transmit synchronization
RxSync	0x00000800	0x0	Receive synchronization
Tx	0x00000400	0x0	Transmit complete
Rx	0x00000200	0x0	Receive complete
TxEmpty	0x00000100	0x0	Transmit channel empty
RxFull	0x00000080	0x0	Receive channel full
TxIRQ	0x00000040	0x0	Transmit channel interrupt
RxIRQ	0x00000020	0x0	Receive channel interrupt
BmRdErr	0x00000010	0x0	Bus master read error
BmWrErr	0x00000008	0x0	Bus master write error
OR	0x00000004	0x0	Overrun
Off	0x00000002	0x0	Bus off
Pass	0x00000001	0x0	Error passive

Register PIC

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Pending Interrupt Clear Register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-											COHbErr	COSync	COWrCmd	CORdCmd	TxLoss	RxMiss	TxErrCntr	RxErrCntr	TxSync	RxSync	Tx	Rx	TxEmpty	RxFull	TxIRQ	RxIRQ	BmRdErr	BmWrErr	OR	Off	Pass
-											wo	wo	wo	wo	wo	wo	wo	wo	wo	wo	wo	wo	wo	wo	wo	wo	wo	wo	wo	wo	wo
-											-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Field	Mask	Reset	Description
COHbErr	0x00100000	-	CANOpen heartbeat error
COSync	0x00080000	-	CANOpen SYNC message
COWrCmd	0x00040000	-	CANOpen write command
CORdCmd	0x00020000	-	CANOpen read command
TxLoss	0x00010000	-	Transmit loss
RxMiss	0x00008000	-	Receive miss
TxErrCntr	0x00004000	-	Transmit error counter threshold
RxErrCntr	0x00002000	-	Receive error counter threshold
TxSync	0x00001000	-	Transmit synchronization
RxSync	0x00000800	-	Receive synchronization
Tx	0x00000400	-	Transmit complete
Rx	0x00000200	-	Receive complete
TxEmpty	0x00000100	-	Transmit channel empty
RxFull	0x00000080	-	Receive channel full
TxIRQ	0x00000040	-	Transmit channel interrupt
RxIRQ	0x00000020	-	Receive channel interrupt
BmRdErr	0x00000010	-	Bus master read error
BmWrErr	0x00000008	-	Bus master write error
OR	0x00000004	-	Overrun
Off	0x00000002	-	Bus off
Pass	0x00000001	-	Error passive

Register RXMASK

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Receive Channel Acceptance Mask Register

Reset value

0x1fffffff

Warm reset mask

0x1fffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	AM
-	rw
-	536870911

Field	Mask	Reset	Description
AM	0x1fffffff	0x1fffffff	Acceptance mask

Register RXCODE

Description

Receive Channel Acceptance Code Register

Reset value

0x00000000

Warm reset mask

0x1fffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	AC
-	rw
-	0

Field	Mask	Reset	Description
AC	0x1fffffff	0x0	Acceptance code

Register TXCTRL

Description

Transmit Channel Control Register

Reset value

0x00000000

Warm reset mask

0x0000000f

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																												DisAck	Single	Ongoing	Enable
-																												ro	rw	ro	rw
-																												0	0	0	0

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
DisAck	0x00000008	0x0	Disable acknowledge
Single	0x00000004	0x0	Single descriptor
Ongoing	0x00000002	0x0	Transfer ongoing
Enable	0x00000001	0x0	Channel enable

Register TXADDR

Description

Transmit Channel Address Register

Reset value

0x00000000

Warm reset mask

0xfffffc00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																						-									
rw																						-									
0																						-									

Field	Mask	Reset	Description
ADDR	0xfffffc00	0x0	Descriptor table address

Register TXSIZE

Description

Transmit Channel Size Register

Reset value

0x00000000

Warm reset mask

0x001fffc0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-											SIZE															-						
-											rw															-						
-											0															-						

Field	Mask	Reset	Description
SIZE	0x001fffc0	0x0	Descriptor table size

Register TXWR

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Transmit Channel Write Register

Reset value

0x00000000

Warm reset mask

0x000ffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-												WR																-			
-												rw																-			
-												0																-			

Field	Mask	Reset	Description
WR	0x000ffff0	0x0	Write pointer

Register TXRD

Description

Transmit Channel Read Register

Reset value

0x00000000

Warm reset mask

0x000ffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-												RD																-			
-												rw																-			
-												0																-			

Field	Mask	Reset	Description
RD	0x000ffff0	0x0	Read pointer

Register TXIRQ

Description

Transmit Channel Interrupt Register

Reset value

0x00000000

Warm reset mask

0x000ffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-												IRQ																-			
-												rw																-			
-												0																-			

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
IRQ	0x000ffff0	0x0	Interrupt pointer

Register RXCTRL

Description

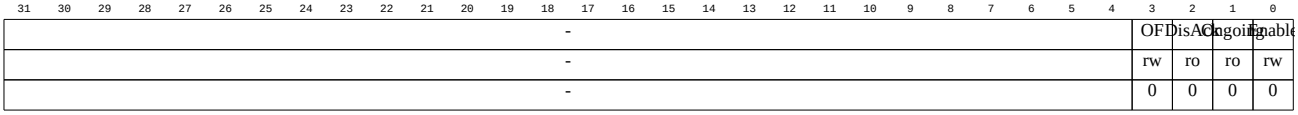
Receive Channel Control Register

Reset value

0x00000000

Warm reset mask

0x0000000f



Field	Mask	Reset	Description
OF	0x00000008	0x0	Overflow
DisAck	0x00000004	0x0	Disable acknowledge
Ongoing	0x00000002	0x0	Transfer ongoing
Enable	0x00000001	0x0	Channel enable

Register RXADDR

Description

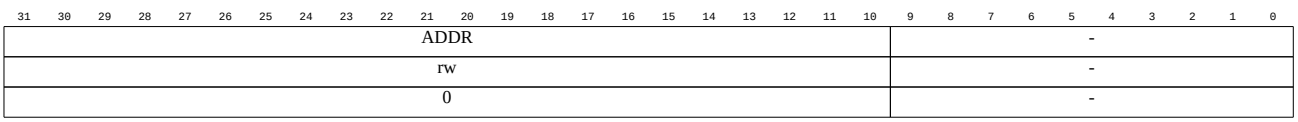
Receive Channel Address Register

Reset value

0x00000000

Warm reset mask

0xfffffc00



Field	Mask	Reset	Description
ADDR	0xfffffc00	0x0	Descriptor table address

Register RXSIZE

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

Receive Channel Size Register

Reset value

0x00000000

Warm reset mask

0x001fffc0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-											SIZE																	-			
-											rw																	-			
-											0																	-			

Field	Mask	Reset	Description
SIZE	0x001fffc0	0x0	Descriptor table size

Register RXWR

Description

Receive Channel Write Register

Reset value

0x00000000

Warm reset mask

0x000ffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-												WR																-			
-												rw																-			
-												0																-			

Field	Mask	Reset	Description
WR	0x000ffff0	0x0	Write pointer

Register RXRD

Description

Receive Channel Read Register

Reset value

0x00000000

Warm reset mask

0x000ffff0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-												RD																-			
-												rw																-			
-												0																-			

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
RD	0x000ffff0	0x0	Read pointer

Register RXIRQ

Description

Receive Channel Interrupt Register

Reset value

0x00000000

Warm reset mask

0x000ffff0

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
-	IRQ	-
-	rw	-
-	0	-

Field	Mask	Reset	Description
IRQ	0x000ffff0	0x0	Interrupt pointer

Commands

Name	Description
delete	Dispose instance of GRCANFD

9.26.5. Limitations

- There is no arbitration of messages in the message passing simulated world and buses are not synchronized.
- The model does at present not register filters with the CAN bus model.
- The CANOpen Heartbeat mechanism is unimplemented. Anything written to or read from CANOpen Heartbeat related registers will be ignored. CANOpen PDOs with a heartbeat function code are acknowleged but do not reset any counters.
- The model would report a overrun if a frame is received without a RX descriptor beeing available sooner than the hardware if the `rxbufsize` IP configuration option is higher than one.

9.27. I2CMST

The I2CMST model is available in the I2CMST plugin.

9.27.1. Loading the Plugin

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

```
import I2CMST
```

9.27.2. Configuration

9.27.3. @I2CMST Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @I2CMST
new	Create new instance of I2CMST

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.27.4. I2CMST Reference

Properties

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
CMD	uint32_t	I2C-master command register
CMDColdResetValue	uint32_t	I2C-master command register
CMDForcedBits	uint32_t	I2C-master command register
CMDForcedFlippedBits	uint32_t	I2C-master command register
CMDReadMask	uint32_t	I2C-master command register
CMDResetMask	uint32_t	I2C-master command register
CMDResetValue	uint32_t	I2C-master command register
CMDWriteMask	uint32_t	I2C-master command register
CTRL	uint32_t	I2C-master control register
CTRLColdResetValue	uint32_t	I2C-master control register
CTRLForcedBits	uint32_t	I2C-master control register
CTRLForcedFlippedBits	uint32_t	I2C-master control register
CTRLReadMask	uint32_t	I2C-master control register
CTRLResetMask	uint32_t	I2C-master control register
CTRLResetValue	uint32_t	I2C-master control register
CTRLWriteMask	uint32_t	I2C-master control register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
FILT	uint32_t	I2C-master dynamic filter register
FILTColdResetValue	uint32_t	I2C-master dynamic filter register
FILTForcedBits	uint32_t	I2C-master dynamic filter register
FILTForcedFlippedBits	uint32_t	I2C-master dynamic filter register
FILTReadMask	uint32_t	I2C-master dynamic filter register
FILTResetMask	uint32_t	I2C-master dynamic filter register
FILTResetValue	uint32_t	I2C-master dynamic filter register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
FILTWriteMask	uint32_t	I2C-master dynamic filter register
LatestBusState	int32_t	Internal: Bus state reported between transfer events
LatestResponseByte	uint8_t	Internal: Bus state response between transfer events
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
PRESCALE	uint32_t	I2C-master Clock prescale register
PRESCALEColdResetValue	uint32_t	I2C-master Clock prescale register
PRESCALEForcedBits	uint32_t	I2C-master Clock prescale register
PRESCALEForcedFlippedBits	uint32_t	I2C-master Clock prescale register
PRESCALEReadMask	uint32_t	I2C-master Clock prescale register
PRESCALEResetMask	uint32_t	I2C-master Clock prescale register
PRESCALEResetValue	uint32_t	I2C-master Clock prescale register
PRESCALEWriteMask	uint32_t	I2C-master Clock prescale register
RX	uint32_t	I2C-master receive register
RXColdResetValue	uint32_t	I2C-master receive register
RXForcedBits	uint32_t	I2C-master receive register
RXForcedFlippedBits	uint32_t	I2C-master receive register
RXReadMask	uint32_t	I2C-master receive register
RXResetMask	uint32_t	I2C-master receive register
RXResetValue	uint32_t	I2C-master receive register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
RXWriteMask	uint32_t	I2C-master receive register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
STAT	uint32_t	I2C-master status register
STATColdResetValue	uint32_t	I2C-master status register
STATForcedBits	uint32_t	I2C-master status register
STATForcedFlippedBits	uint32_t	I2C-master status register
STATReadMask	uint32_t	I2C-master status register
STATResetMask	uint32_t	I2C-master status register
STATResetValue	uint32_t	I2C-master status register
STATWriteMask	uint32_t	I2C-master status register
TX	uint32_t	I2C-master transmit register
TXColdResetValue	uint32_t	I2C-master transmit register
TXForcedBits	uint32_t	I2C-master transmit register
TXForcedFlippedBits	uint32_t	I2C-master transmit register
TXReadMask	uint32_t	I2C-master transmit register
TXResetMask	uint32_t	I2C-master transmit register
TXResetValue	uint32_t	I2C-master transmit register
TXWriteMask	uint32_t	I2C-master transmit register
TimeSource	*void	Time source object
bus	temu_IfaceRef/ <unknown>	I2C bus.
config.I2CBusTimeoutInNS	uint64_t	Time after which to reset this I2C bus even if no STOP condition was seen.
config.infiniteBusSpeed	uint64_t	Handle transfer-done events without delay
config.irq	uint8_t	Interrupt number
config.transferTimeInNS	uint64_t	Number of nanoseconds spent in 'Transport In Progress' mode.
irqCtrl	temu_IfaceRef/ <unknown>	IRQ controller.
lastCounterValOnBus	uint64_t	
lastDevAddrOnBus	uint16_t	
memAccess	temu_IfaceRef/ <unknown>	Memory Interface for DMA containing underlying buffers.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Interfaces

Name	Type	Description
ApbIface	ApbIface	APB P&P interface.
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.

Registers



Register support is currently experimental!

Register Bank Regs

Register PRESCALE

Description

I2C-master Clock prescale register

Reset value

0x0000ffff

Warm reset mask

0x0000ffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																ClockPrescale															
-																rw															
-																65535															

Field	Mask	Reset	Description
ClockPrescale	`0x0000ffff`	`0xffff`	Value used to prescale the SCL clock line

Register CTRL

Description

I2C-master control register

Reset value

0x00000000

Warm reset mask

0x000000c0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								EN	IEN	-					
-																								rw	rw	-					
-																								0	0	-					

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
EN	0x00000080	0x0	Enable I2C core
IEN	0x00000040	0x0	Interrupt enable

Register RX

Description

I2C-master receive register

Reset value

0x00000000

Warm reset mask

0x000000ff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								RDATA							
-																								ro							
-																								0							

Field	Mask	Reset	Description
RDATA	0x000000ff	0x0	Receive data

Register TX

Description

I2C-master transmit register

Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								TDATA							RW
-																								wo							wo
-																								-							-

Field	Mask	Reset	Description
TDATA	0x000000fe	-	Transmit data
RW	0x00000001	-	Read/write bit

Register CMD

Description

I2C-master command register

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Reset value

0x00000000

Warm reset mask

0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								STA	STO	RD	WR	ACK	-	IACK	
-																								wo	wo	wo	wo	wo	-	wo	
-																								-	-	-	-	-	-	-	

Field	Mask	Reset	Description
STA	0x00000080	-	Generate START condition
STO	0x00000040	-	Generate STOP condition
RD	0x00000020	-	Read from slave
WR	0x00000010	-	Write to slave
ACK	0x00000008	-	Acknowledge control
IACK	0x00000001	-	Interrupt acknowledge

Register STAT

Description

I2C-master status register

Reset value

0x00000000

Warm reset mask

0x000000e2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																								RxACK	BUSY	AL	-			TIP	IF
-																								ro	ro	ro	-			ro	rw
-																								0	0	0	-			0	-

Field	Mask	Reset	Description
RxACK	0x00000080	0x0	Receive acknowledge
BUSY	0x00000040	0x0	I2C-bus busy
AL	0x00000020	0x0	Arbitration lost
TIP	0x00000002	0x0	Transfer in progress
IF	0x00000001	-	Interrupt flag

Register FILT

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Description

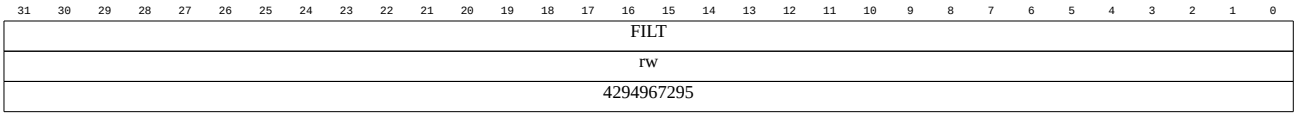
I2C-master dynamic filter register

Reset value

0xffffffff

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
FILT	0xffffffff	0xffffffff	Dynamic filter reload value

Commands

Name	Description
delete	Dispose instance of I2CMST

9.27.5. Limitations

- It is possible for a device to lock up the bus. On hardware, there is a timeout mechanism between the last start condition and when a controller is alowed to send a new start condition without having seen a stop condition on the bus. This timeout mechanism is currently not implemented.

9.28. GRSPFI

The GRSPFI device is part of the GRLIB IP library. It is available in `libTEMUGRSPFI.so`.

9.28.1. Loading the Plugin

```
import GRSPFI
```

9.28.2. Configuration

9.28.3. @GRSPFI Reference

Properties

Name	Type	Description
Class	*void	Class object

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GRSPFI
new	Create new instance of GRSPFI

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.28.4. GRSPFI Reference

Properties

Name	Type	Description
BCCONF	uint32_t	Broadcast Channel Configuration Register
BCCONFColdResetValue	uint32_t	Broadcast Channel Configuration Register
BCCONFForcedBits	uint32_t	Broadcast Channel Configuration Register
BCCONFForcedFlippedBits	uint32_t	Broadcast Channel Configuration Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BCCONFReadMask	uint32_t	Broadcast Channel Configuration Register
BCCONFResetMask	uint32_t	Broadcast Channel Configuration Register
BCCONFResetValue	uint32_t	Broadcast Channel Configuration Register
BCCONFWriteMask	uint32_t	Broadcast Channel Configuration Register
BCMAP	uint32_t	Broadcast Channel Mapping Register
BCMAPColdResetValue	uint32_t	Broadcast Channel Mapping Register
BCMAPForcedBits	uint32_t	Broadcast Channel Mapping Register
BCMAPForcedFlippedBits	uint32_t	Broadcast Channel Mapping Register
BCMAPReadMask	uint32_t	Broadcast Channel Mapping Register
BCMAPResetMask	uint32_t	Broadcast Channel Mapping Register
BCMAPResetValue	uint32_t	Broadcast Channel Mapping Register
BCMAPWriteMask	uint32_t	Broadcast Channel Mapping Register
BCRXADDR	uint32_t	Broadcast Channel RX Address Register
BCRXADDRColdResetValue	uint32_t	Broadcast Channel RX Address Register
BCRXADDRForcedBits	uint32_t	Broadcast Channel RX Address Register
BCRXADDRForcedFlippedBits	uint32_t	Broadcast Channel RX Address Register
BCRXADDRReadMask	uint32_t	Broadcast Channel RX Address Register
BCRXADDRResetMask	uint32_t	Broadcast Channel RX Address Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BCRXADDRResetValue	uint32_t	Broadcast Channel RX Address Register
BCRXADDRWriteMask	uint32_t	Broadcast Channel RX Address Register
BCRXRPTR	uint32_t	Broadcast Channel RX Read Pointer Register
BCRXRPTRColdResetValue	uint32_t	Broadcast Channel RX Read Pointer Register
BCRXRPTRForcedBits	uint32_t	Broadcast Channel RX Read Pointer Register
BCRXRPTRForcedFlippedBits	uint32_t	Broadcast Channel RX Read Pointer Register
BCRXRPTRReadMask	uint32_t	Broadcast Channel RX Read Pointer Register
BCRXRPTRResetMask	uint32_t	Broadcast Channel RX Read Pointer Register
BCRXRPTRResetValue	uint32_t	Broadcast Channel RX Read Pointer Register
BCRXRPTRWriteMask	uint32_t	Broadcast Channel RX Read Pointer Register
BCRXSIZE	uint32_t	Broadcast Channel RX Size Register
BCRXSIZEColdResetValue	uint32_t	Broadcast Channel RX Size Register
BCRXSIZEForcedBits	uint32_t	Broadcast Channel RX Size Register
BCRXSIZEForcedFlippedBits	uint32_t	Broadcast Channel RX Size Register
BCRXSIZEReadMask	uint32_t	Broadcast Channel RX Size Register
BCRXSIZEResetMask	uint32_t	Broadcast Channel RX Size Register
BCRXSIZEResetValue	uint32_t	Broadcast Channel RX Size Register
BCRXSIZEWriteMask	uint32_t	Broadcast Channel RX Size Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BCRXWPTR	uint32_t	Broadcast Channel RX Write Pointer Register
BCRXWPTRColdResetValue	uint32_t	Broadcast Channel RX Write Pointer Register
BCRXWPTRForcedBits	uint32_t	Broadcast Channel RX Write Pointer Register
BCRXWPTRForcedFlippedBits	uint32_t	Broadcast Channel RX Write Pointer Register
BCRXWPTRReadMask	uint32_t	Broadcast Channel RX Write Pointer Register
BCRXWPTRResetMask	uint32_t	Broadcast Channel RX Write Pointer Register
BCRXWPTRResetValue	uint32_t	Broadcast Channel RX Write Pointer Register
BCRXWPTRWriteMask	uint32_t	Broadcast Channel RX Write Pointer Register
BCTXADDR	uint32_t	Broadcast Channel TX Address Register
BCTXADDRColdResetValue	uint32_t	Broadcast Channel TX Address Register
BCTXADDRForcedBits	uint32_t	Broadcast Channel TX Address Register
BCTXADDRForcedFlippedBits	uint32_t	Broadcast Channel TX Address Register
BCTXADDRReadMask	uint32_t	Broadcast Channel TX Address Register
BCTXADDRResetMask	uint32_t	Broadcast Channel TX Address Register
BCTXADDRResetValue	uint32_t	Broadcast Channel TX Address Register
BCTXADDRWriteMask	uint32_t	Broadcast Channel TX Address Register
BCTXRPTR	uint32_t	Broadcast Channel TX Read Pointer Register
BCTXRPTRColdResetValue	uint32_t	Broadcast Channel TX Read Pointer Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BCTXRPTRForcedBits	uint32_t	Broadcast Channel TX Read Pointer Register
BCTXRPTRForcedFlippedBits	uint32_t	Broadcast Channel TX Read Pointer Register
BCTXRPTRReadMask	uint32_t	Broadcast Channel TX Read Pointer Register
BCTXRPTRResetMask	uint32_t	Broadcast Channel TX Read Pointer Register
BCTXRPTRResetValue	uint32_t	Broadcast Channel TX Read Pointer Register
BCTXRPTRWriteMask	uint32_t	Broadcast Channel TX Read Pointer Register
BCTXSIZE	uint32_t	Broadcast Channel TX Size Register
BCTXSIZEColdResetValue	uint32_t	Broadcast Channel TX Size Register
BCTXSIZEForcedBits	uint32_t	Broadcast Channel TX Size Register
BCTXSIZEForcedFlippedBits	uint32_t	Broadcast Channel TX Size Register
BCTXSIZEReadMask	uint32_t	Broadcast Channel TX Size Register
BCTXSIZEResetMask	uint32_t	Broadcast Channel TX Size Register
BCTXSIZEResetValue	uint32_t	Broadcast Channel TX Size Register
BCTXSIZEWriteMask	uint32_t	Broadcast Channel TX Size Register
BCTXWPTR	uint32_t	Broadcast Channel TX Write Pointer Register
BCTXWPTRColdResetValue	uint32_t	Broadcast Channel TX Write Pointer Register
BCTXWPTRForcedBits	uint32_t	Broadcast Channel TX Write Pointer Register
BCTXWPTRForcedFlippedBits	uint32_t	Broadcast Channel TX Write Pointer Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
BCTXWPTRReadMask	uint32_t	Broadcast Channel TX Write Pointer Register
BCTXWPTRResetMask	uint32_t	Broadcast Channel TX Write Pointer Register
BCTXWPTRResetValue	uint32_t	Broadcast Channel TX Write Pointer Register
BCTXWPTRWriteMask	uint32_t	Broadcast Channel TX Write Pointer Register
BUFCAP	uint32_t	Codec Buffers Capabilities Register
BUFCAPColdResetValue	uint32_t	Codec Buffers Capabilities Register
BUFCAPForcedBits	uint32_t	Codec Buffers Capabilities Register
BUFCAPForcedFlippedBits	uint32_t	Codec Buffers Capabilities Register
BUFCAPReadMask	uint32_t	Codec Buffers Capabilities Register
BUFCAPResetMask	uint32_t	Codec Buffers Capabilities Register
BUFCAPResetValue	uint32_t	Codec Buffers Capabilities Register
BUFCAPWriteMask	uint32_t	Codec Buffers Capabilities Register
CCTRL	uint32_t	Codec Control Register
CCTRLColdResetValue	uint32_t	Codec Control Register
CCTRLForcedBits	uint32_t	Codec Control Register
CCTRLForcedFlippedBits	uint32_t	Codec Control Register
CCTRLReadMask	uint32_t	Codec Control Register
CCTRLResetMask	uint32_t	Codec Control Register
CCTRLResetValue	uint32_t	Codec Control Register
CCTRLWriteMask	uint32_t	Codec Control Register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
DCCTRL_0	uint32_t	DMA Channel Control Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DCCTRL_0ColdResetValue	uint32_t	DMA Channel Control Register
DCCTRL_0ForcedBits	uint32_t	DMA Channel Control Register
DCCTRL_0ForcedFlippedBits	uint32_t	DMA Channel Control Register
DCCTRL_0ReadMask	uint32_t	DMA Channel Control Register
DCCTRL_0ResetMask	uint32_t	DMA Channel Control Register
DCCTRL_0ResetValue	uint32_t	DMA Channel Control Register
DCCTRL_0WriteMask	uint32_t	DMA Channel Control Register
DCCTRL_1	uint32_t	DMA Channel Control Register
DCCTRL_1ColdResetValue	uint32_t	DMA Channel Control Register
DCCTRL_1ForcedBits	uint32_t	DMA Channel Control Register
DCCTRL_1ForcedFlippedBits	uint32_t	DMA Channel Control Register
DCCTRL_1ReadMask	uint32_t	DMA Channel Control Register
DCCTRL_1ResetMask	uint32_t	DMA Channel Control Register
DCCTRL_1ResetValue	uint32_t	DMA Channel Control Register
DCCTRL_1WriteMask	uint32_t	DMA Channel Control Register
DCCTRL_2	uint32_t	DMA Channel Control Register
DCCTRL_2ColdResetValue	uint32_t	DMA Channel Control Register
DCCTRL_2ForcedBits	uint32_t	DMA Channel Control Register
DCCTRL_2ForcedFlippedBits	uint32_t	DMA Channel Control Register
DCCTRL_2ReadMask	uint32_t	DMA Channel Control Register
DCCTRL_2ResetMask	uint32_t	DMA Channel Control Register
DCCTRL_2ResetValue	uint32_t	DMA Channel Control Register
DCCTRL_2WriteMask	uint32_t	DMA Channel Control Register
DCCTRL_3	uint32_t	DMA Channel Control Register
DCCTRL_3ColdResetValue	uint32_t	DMA Channel Control Register
DCCTRL_3ForcedBits	uint32_t	DMA Channel Control Register
DCCTRL_3ForcedFlippedBits	uint32_t	DMA Channel Control Register
DCCTRL_3ReadMask	uint32_t	DMA Channel Control Register
DCCTRL_3ResetMask	uint32_t	DMA Channel Control Register
DCCTRL_3ResetValue	uint32_t	DMA Channel Control Register
DCCTRL_3WriteMask	uint32_t	DMA Channel Control Register
DCCTRL_4	uint32_t	DMA Channel Control Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DCCTRL_4ColdResetValue	uint32_t	DMA Channel Control Register
DCCTRL_4ForcedBits	uint32_t	DMA Channel Control Register
DCCTRL_4ForcedFlippedBits	uint32_t	DMA Channel Control Register
DCCTRL_4ReadMask	uint32_t	DMA Channel Control Register
DCCTRL_4ResetMask	uint32_t	DMA Channel Control Register
DCCTRL_4ResetValue	uint32_t	DMA Channel Control Register
DCCTRL_4WriteMask	uint32_t	DMA Channel Control Register
DCCTRL_5	uint32_t	DMA Channel Control Register
DCCTRL_5ColdResetValue	uint32_t	DMA Channel Control Register
DCCTRL_5ForcedBits	uint32_t	DMA Channel Control Register
DCCTRL_5ForcedFlippedBits	uint32_t	DMA Channel Control Register
DCCTRL_5ReadMask	uint32_t	DMA Channel Control Register
DCCTRL_5ResetMask	uint32_t	DMA Channel Control Register
DCCTRL_5ResetValue	uint32_t	DMA Channel Control Register
DCCTRL_5WriteMask	uint32_t	DMA Channel Control Register
DCCTRL_6	uint32_t	DMA Channel Control Register
DCCTRL_6ColdResetValue	uint32_t	DMA Channel Control Register
DCCTRL_6ForcedBits	uint32_t	DMA Channel Control Register
DCCTRL_6ForcedFlippedBits	uint32_t	DMA Channel Control Register
DCCTRL_6ReadMask	uint32_t	DMA Channel Control Register
DCCTRL_6ResetMask	uint32_t	DMA Channel Control Register
DCCTRL_6ResetValue	uint32_t	DMA Channel Control Register
DCCTRL_6WriteMask	uint32_t	DMA Channel Control Register
DCCTRL_7	uint32_t	DMA Channel Control Register
DCCTRL_7ColdResetValue	uint32_t	DMA Channel Control Register
DCCTRL_7ForcedBits	uint32_t	DMA Channel Control Register
DCCTRL_7ForcedFlippedBits	uint32_t	DMA Channel Control Register
DCCTRL_7ReadMask	uint32_t	DMA Channel Control Register
DCCTRL_7ResetMask	uint32_t	DMA Channel Control Register
DCCTRL_7ResetValue	uint32_t	DMA Channel Control Register
DCCTRL_7WriteMask	uint32_t	DMA Channel Control Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DCICTRL_0	uint32_t	DMA Channel IRQ Control Register
DCICTRL_0ColdResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_0ForcedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_0ForcedFlippedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_0ReadMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_0ResetMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_0ResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_0WriteMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_1	uint32_t	DMA Channel IRQ Control Register
DCICTRL_1ColdResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_1ForcedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_1ForcedFlippedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_1ReadMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_1ResetMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_1ResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_1WriteMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_2	uint32_t	DMA Channel IRQ Control Register
DCICTRL_2ColdResetValue	uint32_t	DMA Channel IRQ Control Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DCICTRL_2ForcedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_2ForcedFlippedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_2ReadMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_2ResetMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_2ResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_2WriteMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_3	uint32_t	DMA Channel IRQ Control Register
DCICTRL_3ColdResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_3ForcedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_3ForcedFlippedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_3ReadMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_3ResetMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_3ResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_3WriteMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_4	uint32_t	DMA Channel IRQ Control Register
DCICTRL_4ColdResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_4ForcedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_4ForcedFlippedBits	uint32_t	DMA Channel IRQ Control Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DCICTRL_4ReadMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_4ResetMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_4ResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_4WriteMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_5	uint32_t	DMA Channel IRQ Control Register
DCICTRL_5ColdResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_5ForcedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_5ForcedFlippedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_5ReadMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_5ResetMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_5ResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_5WriteMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_6	uint32_t	DMA Channel IRQ Control Register
DCICTRL_6ColdResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_6ForcedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_6ForcedFlippedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_6ReadMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_6ResetMask	uint32_t	DMA Channel IRQ Control Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DCICTRL_6ResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_6WriteMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_7	uint32_t	DMA Channel IRQ Control Register
DCICTRL_7ColdResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_7ForcedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_7ForcedFlippedBits	uint32_t	DMA Channel IRQ Control Register
DCICTRL_7ReadMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_7ResetMask	uint32_t	DMA Channel IRQ Control Register
DCICTRL_7ResetValue	uint32_t	DMA Channel IRQ Control Register
DCICTRL_7WriteMask	uint32_t	DMA Channel IRQ Control Register
DCMAP_0	uint32_t	DMA Channel VC Mapping Register
DCMAP_0ColdResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_0ForcedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_0ForcedFlippedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_0ReadMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_0ResetMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_0ResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_0WriteMask	uint32_t	DMA Channel VC Mapping Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DCMAP_1	uint32_t	DMA Channel VC Mapping Register
DCMAP_1ColdResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_1ForcedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_1ForcedFlippedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_1ReadMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_1ResetMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_1ResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_1WriteMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_2	uint32_t	DMA Channel VC Mapping Register
DCMAP_2ColdResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_2ForcedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_2ForcedFlippedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_2ReadMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_2ResetMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_2ResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_2WriteMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_3	uint32_t	DMA Channel VC Mapping Register
DCMAP_3ColdResetValue	uint32_t	DMA Channel VC Mapping Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DCMAP_3ForcedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_3ForcedFlippedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_3ReadMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_3ResetMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_3ResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_3WriteMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_4	uint32_t	DMA Channel VC Mapping Register
DCMAP_4ColdResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_4ForcedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_4ForcedFlippedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_4ReadMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_4ResetMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_4ResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_4WriteMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_5	uint32_t	DMA Channel VC Mapping Register
DCMAP_5ColdResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_5ForcedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_5ForcedFlippedBits	uint32_t	DMA Channel VC Mapping Register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DCMAP_5ReadMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_5ResetMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_5ResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_5WriteMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_6	uint32_t	DMA Channel VC Mapping Register
DCMAP_6ColdResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_6ForcedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_6ForcedFlippedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_6ReadMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_6ResetMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_6ResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_6WriteMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_7	uint32_t	DMA Channel VC Mapping Register
DCMAP_7ColdResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_7ForcedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_7ForcedFlippedBits	uint32_t	DMA Channel VC Mapping Register
DCMAP_7ReadMask	uint32_t	DMA Channel VC Mapping Register
DCMAP_7ResetMask	uint32_t	DMA Channel VC Mapping Register

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Name	Type	Description
DCMAP_7ResetValue	uint32_t	DMA Channel VC Mapping Register
DCMAP_7WriteMask	uint32_t	DMA Channel VC Mapping Register
DCSTAT2_0	uint32_t	DMA Channel Extended Status Register
DCSTAT2_0ColdResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_0ForcedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_0ForcedFlippedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_0ReadMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_0ResetMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_0ResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_0WriteMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_1	uint32_t	DMA Channel Extended Status Register
DCSTAT2_1ColdResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_1ForcedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_1ForcedFlippedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_1ReadMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_1ResetMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_1ResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_1WriteMask	uint32_t	DMA Channel Extended Status Register

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Name	Type	Description
DCSTAT2_2	uint32_t	DMA Channel Extended Status Register
DCSTAT2_2ColdResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_2ForcedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_2ForcedFlippedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_2ReadMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_2ResetMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_2ResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_2WriteMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_3	uint32_t	DMA Channel Extended Status Register
DCSTAT2_3ColdResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_3ForcedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_3ForcedFlippedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_3ReadMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_3ResetMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_3ResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_3WriteMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_4	uint32_t	DMA Channel Extended Status Register
DCSTAT2_4ColdResetValue	uint32_t	DMA Channel Extended Status Register

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Name	Type	Description
DCSTAT2_4ForcedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_4ForcedFlippedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_4ReadMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_4ResetMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_4ResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_4WriteMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_5	uint32_t	DMA Channel Extended Status Register
DCSTAT2_5ColdResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_5ForcedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_5ForcedFlippedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_5ReadMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_5ResetMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_5ResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_5WriteMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_6	uint32_t	DMA Channel Extended Status Register
DCSTAT2_6ColdResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_6ForcedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_6ForcedFlippedBits	uint32_t	DMA Channel Extended Status Register

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Name	Type	Description
DCSTAT2_6ReadMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_6ResetMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_6ResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_6WriteMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_7	uint32_t	DMA Channel Extended Status Register
DCSTAT2_7ColdResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_7ForcedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_7ForcedFlippedBits	uint32_t	DMA Channel Extended Status Register
DCSTAT2_7ReadMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_7ResetMask	uint32_t	DMA Channel Extended Status Register
DCSTAT2_7ResetValue	uint32_t	DMA Channel Extended Status Register
DCSTAT2_7WriteMask	uint32_t	DMA Channel Extended Status Register
DCSTAT_0	uint32_t	DMA Channel Status Register
DCSTAT_0ColdResetValue	uint32_t	DMA Channel Status Register
DCSTAT_0ForcedBits	uint32_t	DMA Channel Status Register
DCSTAT_0ForcedFlippedBits	uint32_t	DMA Channel Status Register
DCSTAT_0ReadMask	uint32_t	DMA Channel Status Register
DCSTAT_0ResetMask	uint32_t	DMA Channel Status Register
DCSTAT_0ResetValue	uint32_t	DMA Channel Status Register
DCSTAT_0WriteMask	uint32_t	DMA Channel Status Register
DCSTAT_1	uint32_t	DMA Channel Status Register
DCSTAT_1ColdResetValue	uint32_t	DMA Channel Status Register
DCSTAT_1ForcedBits	uint32_t	DMA Channel Status Register

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Name	Type	Description
DCSTAT_1ForcedFlippedBits	uint32_t	DMA Channel Status Register
DCSTAT_1ReadMask	uint32_t	DMA Channel Status Register
DCSTAT_1ResetMask	uint32_t	DMA Channel Status Register
DCSTAT_1ResetValue	uint32_t	DMA Channel Status Register
DCSTAT_1WriteMask	uint32_t	DMA Channel Status Register
DCSTAT_2	uint32_t	DMA Channel Status Register
DCSTAT_2ColdResetValue	uint32_t	DMA Channel Status Register
DCSTAT_2ForcedBits	uint32_t	DMA Channel Status Register
DCSTAT_2ForcedFlippedBits	uint32_t	DMA Channel Status Register
DCSTAT_2ReadMask	uint32_t	DMA Channel Status Register
DCSTAT_2ResetMask	uint32_t	DMA Channel Status Register
DCSTAT_2ResetValue	uint32_t	DMA Channel Status Register
DCSTAT_2WriteMask	uint32_t	DMA Channel Status Register
DCSTAT_3	uint32_t	DMA Channel Status Register
DCSTAT_3ColdResetValue	uint32_t	DMA Channel Status Register
DCSTAT_3ForcedBits	uint32_t	DMA Channel Status Register
DCSTAT_3ForcedFlippedBits	uint32_t	DMA Channel Status Register
DCSTAT_3ReadMask	uint32_t	DMA Channel Status Register
DCSTAT_3ResetMask	uint32_t	DMA Channel Status Register
DCSTAT_3ResetValue	uint32_t	DMA Channel Status Register
DCSTAT_3WriteMask	uint32_t	DMA Channel Status Register
DCSTAT_4	uint32_t	DMA Channel Status Register
DCSTAT_4ColdResetValue	uint32_t	DMA Channel Status Register
DCSTAT_4ForcedBits	uint32_t	DMA Channel Status Register
DCSTAT_4ForcedFlippedBits	uint32_t	DMA Channel Status Register
DCSTAT_4ReadMask	uint32_t	DMA Channel Status Register
DCSTAT_4ResetMask	uint32_t	DMA Channel Status Register
DCSTAT_4ResetValue	uint32_t	DMA Channel Status Register
DCSTAT_4WriteMask	uint32_t	DMA Channel Status Register
DCSTAT_5	uint32_t	DMA Channel Status Register
DCSTAT_5ColdResetValue	uint32_t	DMA Channel Status Register
DCSTAT_5ForcedBits	uint32_t	DMA Channel Status Register

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Name	Type	Description
DCSTAT_5ForcedFlippedBits	uint32_t	DMA Channel Status Register
DCSTAT_5ReadMask	uint32_t	DMA Channel Status Register
DCSTAT_5ResetMask	uint32_t	DMA Channel Status Register
DCSTAT_5ResetValue	uint32_t	DMA Channel Status Register
DCSTAT_5WriteMask	uint32_t	DMA Channel Status Register
DCSTAT_6	uint32_t	DMA Channel Status Register
DCSTAT_6ColdResetValue	uint32_t	DMA Channel Status Register
DCSTAT_6ForcedBits	uint32_t	DMA Channel Status Register
DCSTAT_6ForcedFlippedBits	uint32_t	DMA Channel Status Register
DCSTAT_6ReadMask	uint32_t	DMA Channel Status Register
DCSTAT_6ResetMask	uint32_t	DMA Channel Status Register
DCSTAT_6ResetValue	uint32_t	DMA Channel Status Register
DCSTAT_6WriteMask	uint32_t	DMA Channel Status Register
DCSTAT_7	uint32_t	DMA Channel Status Register
DCSTAT_7ColdResetValue	uint32_t	DMA Channel Status Register
DCSTAT_7ForcedBits	uint32_t	DMA Channel Status Register
DCSTAT_7ForcedFlippedBits	uint32_t	DMA Channel Status Register
DCSTAT_7ReadMask	uint32_t	DMA Channel Status Register
DCSTAT_7ResetMask	uint32_t	DMA Channel Status Register
DCSTAT_7ResetValue	uint32_t	DMA Channel Status Register
DCSTAT_7WriteMask	uint32_t	DMA Channel Status Register
DEFADDR	uint32_t	Default Address Register
DEFADDRColdResetValue	uint32_t	Default Address Register
DEFADDRForcedBits	uint32_t	Default Address Register
DEFADDRForcedFlippedBits	uint32_t	Default Address Register
DEFADDRReadMask	uint32_t	Default Address Register
DEFADDRResetMask	uint32_t	Default Address Register
DEFADDRResetValue	uint32_t	Default Address Register
DEFADDRWriteMask	uint32_t	Default Address Register
DLCAP	uint32_t	DMA Layer Capabilities Register
DLCAPColdResetValue	uint32_t	DMA Layer Capabilities Register
DLCAPForcedBits	uint32_t	DMA Layer Capabilities Register

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Name	Type	Description
DLCAPForcedFlippedBits	uint32_t	DMA Layer Capabilities Register
DLCAPReadMask	uint32_t	DMA Layer Capabilities Register
DLCAPResetMask	uint32_t	DMA Layer Capabilities Register
DLCAPResetValue	uint32_t	DMA Layer Capabilities Register
DLCAPWriteMask	uint32_t	DMA Layer Capabilities Register
DLCTRL	uint32_t	DMA Layer Control Register
DLCTRLColdResetValue	uint32_t	DMA Layer Control Register
DLCTRLForcedBits	uint32_t	DMA Layer Control Register
DLCTRLForcedFlippedBits	uint32_t	DMA Layer Control Register
DLCTRLReadMask	uint32_t	DMA Layer Control Register
DLCTRLResetMask	uint32_t	DMA Layer Control Register
DLCTRLResetValue	uint32_t	DMA Layer Control Register
DLCTRLWriteMask	uint32_t	DMA Layer Control Register
DLSTAT	uint32_t	DMA Layer Status Register
DLSTATColdResetValue	uint32_t	DMA Layer Status Register
DLSTATForcedBits	uint32_t	DMA Layer Status Register
DLSTATForcedFlippedBits	uint32_t	DMA Layer Status Register
DLSTATReadMask	uint32_t	DMA Layer Status Register
DLSTATResetMask	uint32_t	DMA Layer Status Register
DLSTATResetValue	uint32_t	DMA Layer Status Register
DLSTATWriteMask	uint32_t	DMA Layer Status Register
DMAChannels	[temu_IfaceRef; 8]/ <unknown>	DMA Channel Interfaces
GENCAP	uint32_t	Codec General Capabilities Register
GENCAPColdResetValue	uint32_t	Codec General Capabilities Register
GENCAPForcedBits	uint32_t	Codec General Capabilities Register
GENCAPForcedFlippedBits	uint32_t	Codec General Capabilities Register
GENCAPReadMask	uint32_t	Codec General Capabilities Register
GENCAPResetMask	uint32_t	Codec General Capabilities Register

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Name	Type	Description
GENCAPResetValue	uint32_t	Codec General Capabilities Register
GENCAPWriteMask	uint32_t	Codec General Capabilities Register
LLSTAT	uint32_t	Lane Layer Status Register
LLSTATColdResetValue	uint32_t	Lane Layer Status Register
LLSTATForcedBits	uint32_t	Lane Layer Status Register
LLSTATForcedFlippedBits	uint32_t	Lane Layer Status Register
LLSTATReadMask	uint32_t	Lane Layer Status Register
LLSTATResetMask	uint32_t	Lane Layer Status Register
LLSTATResetValue	uint32_t	Lane Layer Status Register
LLSTATWriteMask	uint32_t	Lane Layer Status Register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
RLSTAT	uint32_t	Retry Layer Status Register
RLSTATColdResetValue	uint32_t	Retry Layer Status Register
RLSTATForcedBits	uint32_t	Retry Layer Status Register
RLSTATForcedFlippedBits	uint32_t	Retry Layer Status Register
RLSTATReadMask	uint32_t	Retry Layer Status Register
RLSTATResetMask	uint32_t	Retry Layer Status Register
RLSTATResetValue	uint32_t	Retry Layer Status Register
RLSTATWriteMask	uint32_t	Retry Layer Status Register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
SPFIEN	uint32_t	SpaceFibre Enable Register
SPFIENColdResetValue	uint32_t	SpaceFibre Enable Register
SPFIENForcedBits	uint32_t	SpaceFibre Enable Register
SPFIENForcedFlippedBits	uint32_t	SpaceFibre Enable Register

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Name	Type	Description
SPFIENReadMask	uint32_t	SpaceFibre Enable Register
SPFIENResetMask	uint32_t	SpaceFibre Enable Register
SPFIENResetValue	uint32_t	SpaceFibre Enable Register
SPFIENWriteMask	uint32_t	SpaceFibre Enable Register
SpfiPort	temu_IfaceRef/ <unknown>	SpaceFibre port to the other side of the link.
TS	uint32_t	Time-slot Register
TSCTRL	uint32_t	Time-slot Control Register
TSCTRLColdResetValue	uint32_t	Time-slot Control Register
TSCTRLForcedBits	uint32_t	Time-slot Control Register
TSCTRLForcedFlippedBits	uint32_t	Time-slot Control Register
TSCTRLReadMask	uint32_t	Time-slot Control Register
TSCTRLResetMask	uint32_t	Time-slot Control Register
TSCTRLResetValue	uint32_t	Time-slot Control Register
TSCTRLWriteMask	uint32_t	Time-slot Control Register
TSColdResetValue	uint32_t	Time-slot Register
TSForcedBits	uint32_t	Time-slot Register
TSForcedFlippedBits	uint32_t	Time-slot Register
TSLEN	uint32_t	Time-slot Length Register
TSLENColdResetValue	uint32_t	Time-slot Length Register
TSLENForcedBits	uint32_t	Time-slot Length Register
TSLENForcedFlippedBits	uint32_t	Time-slot Length Register
TSLENReadMask	uint32_t	Time-slot Length Register
TSLENResetMask	uint32_t	Time-slot Length Register
TSLENResetValue	uint32_t	Time-slot Length Register
TSLENWriteMask	uint32_t	Time-slot Length Register
TSReadMask	uint32_t	Time-slot Register
TSResetMask	uint32_t	Time-slot Register
TSResetValue	uint32_t	Time-slot Register
TSWriteMask	uint32_t	Time-slot Register
TimeSource	*void	Time source object

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Name	Type	Description
VCADDR_0	uint32_t	Virtual Channel Address Register
VCADDR_0ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_0ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_0ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_0ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_0ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_0ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_0WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_1	uint32_t	Virtual Channel Address Register
VCADDR_10	uint32_t	Virtual Channel Address Register
VCADDR_10ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_10ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_10ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_10ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_10ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_10ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_10WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_11	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_11ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_11ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_11ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_11ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_11ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_11ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_11WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_12	uint32_t	Virtual Channel Address Register
VCADDR_12ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_12ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_12ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_12ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_12ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_12ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_12WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_13	uint32_t	Virtual Channel Address Register
VCADDR_13ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_13ForcedBits	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_13ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_13ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_13ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_13ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_13WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_14	uint32_t	Virtual Channel Address Register
VCADDR_14ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_14ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_14ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_14ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_14ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_14ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_14WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_15	uint32_t	Virtual Channel Address Register
VCADDR_15ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_15ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_15ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_15ReadMask	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_15ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_15ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_15WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_16	uint32_t	Virtual Channel Address Register
VCADDR_16ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_16ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_16ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_16ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_16ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_16ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_16WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_17	uint32_t	Virtual Channel Address Register
VCADDR_17ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_17ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_17ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_17ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_17ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_17ResetValue	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_17WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_18	uint32_t	Virtual Channel Address Register
VCADDR_18ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_18ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_18ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_18ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_18ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_18ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_18WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_19	uint32_t	Virtual Channel Address Register
VCADDR_19ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_19ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_19ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_19ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_19ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_19ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_19WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_1ColdResetValue	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_1ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_1ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_1ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_1ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_1ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_1WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_2	uint32_t	Virtual Channel Address Register
VCADDR_20	uint32_t	Virtual Channel Address Register
VCADDR_20ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_20ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_20ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_20ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_20ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_20ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_20WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_21	uint32_t	Virtual Channel Address Register
VCADDR_21ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_21ForcedBits	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_21ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_21ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_21ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_21ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_21WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_22	uint32_t	Virtual Channel Address Register
VCADDR_22ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_22ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_22ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_22ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_22ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_22ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_22WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_23	uint32_t	Virtual Channel Address Register
VCADDR_23ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_23ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_23ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_23ReadMask	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_23ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_23ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_23WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_24	uint32_t	Virtual Channel Address Register
VCADDR_24ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_24ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_24ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_24ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_24ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_24ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_24WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_25	uint32_t	Virtual Channel Address Register
VCADDR_25ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_25ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_25ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_25ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_25ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_25ResetValue	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_25WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_26	uint32_t	Virtual Channel Address Register
VCADDR_26ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_26ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_26ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_26ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_26ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_26ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_26WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_27	uint32_t	Virtual Channel Address Register
VCADDR_27ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_27ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_27ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_27ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_27ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_27ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_27WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_28	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_28ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_28ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_28ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_28ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_28ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_28ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_28WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_29	uint32_t	Virtual Channel Address Register
VCADDR_29ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_29ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_29ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_29ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_29ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_29ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_29WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_2ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_2ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_2ForcedFlippedBits	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_2ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_2ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_2ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_2WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_3	uint32_t	Virtual Channel Address Register
VCADDR_30	uint32_t	Virtual Channel Address Register
VCADDR_30ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_30ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_30ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_30ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_30ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_30ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_30WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_31	uint32_t	Virtual Channel Address Register
VCADDR_31ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_31ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_31ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_31ReadMask	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_31ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_31ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_31WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_3ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_3ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_3ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_3ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_3ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_3ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_3WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_4	uint32_t	Virtual Channel Address Register
VCADDR_4ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_4ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_4ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_4ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_4ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_4ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_4WriteMask	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_5	uint32_t	Virtual Channel Address Register
VCADDR_5ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_5ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_5ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_5ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_5ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_5ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_5WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_6	uint32_t	Virtual Channel Address Register
VCADDR_6ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_6ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_6ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_6ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_6ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_6ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_6WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_7	uint32_t	Virtual Channel Address Register
VCADDR_7ColdResetValue	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_7ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_7ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_7ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_7ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_7ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_7WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_8	uint32_t	Virtual Channel Address Register
VCADDR_8ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_8ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_8ForcedFlippedBits	uint32_t	Virtual Channel Address Register
VCADDR_8ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_8ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_8ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_8WriteMask	uint32_t	Virtual Channel Address Register
VCADDR_9	uint32_t	Virtual Channel Address Register
VCADDR_9ColdResetValue	uint32_t	Virtual Channel Address Register
VCADDR_9ForcedBits	uint32_t	Virtual Channel Address Register
VCADDR_9ForcedFlippedBits	uint32_t	Virtual Channel Address Register

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Name	Type	Description
VCADDR_9ReadMask	uint32_t	Virtual Channel Address Register
VCADDR_9ResetMask	uint32_t	Virtual Channel Address Register
VCADDR_9ResetValue	uint32_t	Virtual Channel Address Register
VCADDR_9WriteMask	uint32_t	Virtual Channel Address Register
VCCTRL_0	uint32_t	Virtual Channel Control Register
VCCTRL_0ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_0ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_0ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_0ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_0ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_0ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_0WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_1	uint32_t	Virtual Channel Control Register
VCCTRL_10	uint32_t	Virtual Channel Control Register
VCCTRL_10ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_10ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_10ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_10ReadMask	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_10ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_10ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_10WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_11	uint32_t	Virtual Channel Control Register
VCCTRL_11ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_11ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_11ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_11ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_11ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_11ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_11WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_12	uint32_t	Virtual Channel Control Register
VCCTRL_12ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_12ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_12ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_12ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_12ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_12ResetValue	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_12WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_13	uint32_t	Virtual Channel Control Register
VCCTRL_13ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_13ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_13ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_13ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_13ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_13ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_13WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_14	uint32_t	Virtual Channel Control Register
VCCTRL_14ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_14ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_14ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_14ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_14ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_14ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_14WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_15	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_15ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_15ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_15ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_15ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_15ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_15ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_15WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_16	uint32_t	Virtual Channel Control Register
VCCTRL_16ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_16ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_16ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_16ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_16ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_16ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_16WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_17	uint32_t	Virtual Channel Control Register
VCCTRL_17ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_17ForcedBits	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_17ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_17ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_17ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_17ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_17WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_18	uint32_t	Virtual Channel Control Register
VCCTRL_18ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_18ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_18ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_18ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_18ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_18ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_18WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_19	uint32_t	Virtual Channel Control Register
VCCTRL_19ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_19ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_19ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_19ReadMask	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_19ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_19ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_19WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_1ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_1ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_1ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_1ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_1ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_1ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_1WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_2	uint32_t	Virtual Channel Control Register
VCCTRL_20	uint32_t	Virtual Channel Control Register
VCCTRL_20ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_20ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_20ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_20ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_20ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_20ResetValue	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_20WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_21	uint32_t	Virtual Channel Control Register
VCCTRL_21ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_21ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_21ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_21ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_21ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_21ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_21WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_22	uint32_t	Virtual Channel Control Register
VCCTRL_22ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_22ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_22ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_22ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_22ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_22ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_22WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_23	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_23ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_23ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_23ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_23ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_23ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_23ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_23WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_24	uint32_t	Virtual Channel Control Register
VCCTRL_24ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_24ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_24ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_24ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_24ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_24ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_24WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_25	uint32_t	Virtual Channel Control Register
VCCTRL_25ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_25ForcedBits	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_25ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_25ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_25ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_25ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_25WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_26	uint32_t	Virtual Channel Control Register
VCCTRL_26ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_26ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_26ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_26ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_26ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_26ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_26WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_27	uint32_t	Virtual Channel Control Register
VCCTRL_27ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_27ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_27ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_27ReadMask	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_27ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_27ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_27WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_28	uint32_t	Virtual Channel Control Register
VCCTRL_28ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_28ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_28ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_28ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_28ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_28ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_28WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_29	uint32_t	Virtual Channel Control Register
VCCTRL_29ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_29ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_29ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_29ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_29ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_29ResetValue	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_29WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_2ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_2ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_2ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_2ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_2ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_2ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_2WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_3	uint32_t	Virtual Channel Control Register
VCCTRL_30	uint32_t	Virtual Channel Control Register
VCCTRL_30ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_30ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_30ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_30ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_30ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_30ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_30WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_31	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_31ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_31ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_31ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_31ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_31ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_31ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_31WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_3ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_3ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_3ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_3ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_3ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_3ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_3WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_4	uint32_t	Virtual Channel Control Register
VCCTRL_4ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_4ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_4ForcedFlippedBits	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_4ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_4ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_4ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_4WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_5	uint32_t	Virtual Channel Control Register
VCCTRL_5ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_5ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_5ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_5ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_5ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_5ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_5WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_6	uint32_t	Virtual Channel Control Register
VCCTRL_6ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_6ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_6ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_6ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_6ResetMask	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_6ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_6WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_7	uint32_t	Virtual Channel Control Register
VCCTRL_7ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_7ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_7ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_7ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_7ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_7ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_7WriteMask	uint32_t	Virtual Channel Control Register
VCCTRL_8	uint32_t	Virtual Channel Control Register
VCCTRL_8ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_8ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_8ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_8ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_8ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_8ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_8WriteMask	uint32_t	Virtual Channel Control Register

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Name	Type	Description
VCCTRL_9	uint32_t	Virtual Channel Control Register
VCCTRL_9ColdResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_9ForcedBits	uint32_t	Virtual Channel Control Register
VCCTRL_9ForcedFlippedBits	uint32_t	Virtual Channel Control Register
VCCTRL_9ReadMask	uint32_t	Virtual Channel Control Register
VCCTRL_9ResetMask	uint32_t	Virtual Channel Control Register
VCCTRL_9ResetValue	uint32_t	Virtual Channel Control Register
VCCTRL_9WriteMask	uint32_t	Virtual Channel Control Register
VCDCTRL_0	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_0ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_0ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_0ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_0ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_0ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_0ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_0WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_1	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_10	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_10ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_10ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_10ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_10ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_10ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_10ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_10WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_11	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_11ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_11ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_11ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_11ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_11ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_11ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_11WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_12	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_12ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_12ForcedBits	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_12ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_12ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_12ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_12ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_12WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_13	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_13ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_13ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_13ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_13ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_13ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_13ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_13WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_14	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_14ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_14ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_14ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_14ReadMask	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_14ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_14ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_14WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_15	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_15ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_15ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_15ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_15ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_15ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_15ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_15WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_16	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_16ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_16ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_16ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_16ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_16ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_16ResetValue	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_16WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_17	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_17ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_17ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_17ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_17ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_17ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_17ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_17WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_18	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_18ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_18ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_18ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_18ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_18ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_18ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_18WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_19	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_19ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_19ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_19ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_19ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_19ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_19ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_19WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_1ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_1ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_1ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_1ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_1ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_1ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_1WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_2	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_20	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_20ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_20ForcedBits	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_20ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_20ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_20ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_20ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_20WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_21	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_21ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_21ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_21ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_21ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_21ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_21ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_21WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_22	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_22ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_22ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_22ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_22ReadMask	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_22ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_22ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_22WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_23	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_23ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_23ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_23ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_23ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_23ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_23ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_23WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_24	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_24ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_24ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_24ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_24ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_24ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_24ResetValue	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_24WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_25	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_25ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_25ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_25ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_25ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_25ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_25ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_25WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_26	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_26ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_26ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_26ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_26ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_26ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_26ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_26WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_27	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_27ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_27ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_27ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_27ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_27ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_27ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_27WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_28	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_28ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_28ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_28ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_28ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_28ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_28ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_28WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_29	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_29ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_29ForcedBits	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_29ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_29ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_29ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_29ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_29WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_2ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_2ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_2ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_2ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_2ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_2ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_2WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_3	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_30	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_30ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_30ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_30ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_30ReadMask	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_30ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_30ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_30WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_31	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_31ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_31ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_31ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_31ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_31ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_31ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_31WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_3ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_3ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_3ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_3ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_3ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_3ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_3WriteMask	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_4	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_4ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_4ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_4ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_4ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_4ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_4ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_4WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_5	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_5ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_5ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_5ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_5ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_5ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_5ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_5WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_6	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_6ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_6ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_6ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_6ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_6ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_6ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_6WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_7	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_7ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_7ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_7ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_7ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_7ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_7ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_7WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_8	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_8ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_8ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_8ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register

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Name	Type	Description
VCDCTRL_8ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_8ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_8ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_8WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_9	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_9ColdResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_9ForcedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_9ForcedFlippedBits	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_9ReadMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_9ResetMask	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_9ResetValue	uint32_t	Virtual Channel Descriptor Control Register
VCDCTRL_9WriteMask	uint32_t	Virtual Channel Descriptor Control Register
VCKEY_0	uint32_t	Virtual Channel Destination Key Register
VCKEY_0ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_0ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_0ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_0ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_0ResetMask	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_0ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_0WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_1	uint32_t	Virtual Channel Destination Key Register
VCKEY_10	uint32_t	Virtual Channel Destination Key Register
VCKEY_10ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_10ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_10ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_10ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_10ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_10ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_10WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_11	uint32_t	Virtual Channel Destination Key Register
VCKEY_11ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_11ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_11ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_11ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_11ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_11ResetValue	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_11WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_12	uint32_t	Virtual Channel Destination Key Register
VCKEY_12ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_12ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_12ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_12ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_12ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_12ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_12WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_13	uint32_t	Virtual Channel Destination Key Register
VCKEY_13ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_13ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_13ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_13ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_13ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_13ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_13WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_14	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_14ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_14ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_14ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_14ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_14ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_14ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_14WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_15	uint32_t	Virtual Channel Destination Key Register
VCKEY_15ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_15ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_15ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_15ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_15ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_15ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_15WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_16	uint32_t	Virtual Channel Destination Key Register
VCKEY_16ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_16ForcedBits	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_16ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_16ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_16ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_16ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_16WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_17	uint32_t	Virtual Channel Destination Key Register
VCKEY_17ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_17ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_17ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_17ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_17ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_17ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_17WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_18	uint32_t	Virtual Channel Destination Key Register
VCKEY_18ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_18ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_18ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_18ReadMask	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_18ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_18ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_18WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_19	uint32_t	Virtual Channel Destination Key Register
VCKEY_19ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_19ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_19ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_19ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_19ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_19ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_19WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_1ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_1ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_1ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_1ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_1ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_1ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_1WriteMask	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_2	uint32_t	Virtual Channel Destination Key Register
VCKEY_20	uint32_t	Virtual Channel Destination Key Register
VCKEY_20ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_20ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_20ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_20ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_20ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_20ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_20WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_21	uint32_t	Virtual Channel Destination Key Register
VCKEY_21ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_21ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_21ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_21ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_21ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_21ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_21WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_22	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_22ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_22ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_22ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_22ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_22ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_22ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_22WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_23	uint32_t	Virtual Channel Destination Key Register
VCKEY_23ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_23ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_23ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_23ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_23ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_23ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_23WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_24	uint32_t	Virtual Channel Destination Key Register
VCKEY_24ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_24ForcedBits	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_24ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_24ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_24ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_24ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_24WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_25	uint32_t	Virtual Channel Destination Key Register
VCKEY_25ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_25ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_25ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_25ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_25ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_25ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_25WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_26	uint32_t	Virtual Channel Destination Key Register
VCKEY_26ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_26ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_26ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_26ReadMask	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_26ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_26ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_26WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_27	uint32_t	Virtual Channel Destination Key Register
VCKEY_27ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_27ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_27ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_27ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_27ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_27ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_27WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_28	uint32_t	Virtual Channel Destination Key Register
VCKEY_28ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_28ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_28ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_28ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_28ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_28ResetValue	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_28WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_29	uint32_t	Virtual Channel Destination Key Register
VCKEY_29ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_29ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_29ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_29ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_29ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_29ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_29WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_2ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_2ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_2ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_2ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_2ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_2ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_2WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_3	uint32_t	Virtual Channel Destination Key Register
VCKEY_30	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_30ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_30ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_30ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_30ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_30ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_30ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_30WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_31	uint32_t	Virtual Channel Destination Key Register
VCKEY_31ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_31ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_31ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_31ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_31ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_31ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_31WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_3ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_3ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_3ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_3ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_3ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_3ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_3WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_4	uint32_t	Virtual Channel Destination Key Register
VCKEY_4ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_4ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_4ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_4ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_4ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_4ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_4WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_5	uint32_t	Virtual Channel Destination Key Register
VCKEY_5ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_5ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_5ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_5ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_5ResetMask	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_5ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_5WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_6	uint32_t	Virtual Channel Destination Key Register
VCKEY_6ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_6ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_6ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_6ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_6ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_6ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_6WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_7	uint32_t	Virtual Channel Destination Key Register
VCKEY_7ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_7ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_7ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_7ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_7ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_7ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_7WriteMask	uint32_t	Virtual Channel Destination Key Register

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Name	Type	Description
VCKEY_8	uint32_t	Virtual Channel Destination Key Register
VCKEY_8ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_8ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_8ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_8ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_8ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_8ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_8WriteMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_9	uint32_t	Virtual Channel Destination Key Register
VCKEY_9ColdResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_9ForcedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_9ForcedFlippedBits	uint32_t	Virtual Channel Destination Key Register
VCKEY_9ReadMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_9ResetMask	uint32_t	Virtual Channel Destination Key Register
VCKEY_9ResetValue	uint32_t	Virtual Channel Destination Key Register
VCKEY_9WriteMask	uint32_t	Virtual Channel Destination Key Register
VCMAXLEN_0	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_0ColdResetValue	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_0ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_0ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_0ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_0ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_0ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_0WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_1	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_10	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_10ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_10ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_10ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_10ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_10ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_10ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_10WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_11	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_11ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_11ForcedBits	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_11ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_11ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_11ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_11ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_11WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_12	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_12ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_12ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_12ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_12ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_12ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_12ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_12WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_13	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_13ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_13ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_13ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_13ReadMask	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_13ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_13ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_13WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_14	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_14ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_14ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_14ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_14ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_14ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_14ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_14WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_15	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_15ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_15ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_15ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_15ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_15ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_15ResetValue	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_15WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_16	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_16ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_16ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_16ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_16ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_16ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_16ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_16WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_17	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_17ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_17ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_17ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_17ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_17ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_17ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_17WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_18	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_18ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_18ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_18ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_18ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_18ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_18ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_18WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_19	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_19ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_19ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_19ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_19ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_19ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_19ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_19WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_1ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_1ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_1ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_1ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_1ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_1ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_1WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_2	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_20	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_20ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_20ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_20ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_20ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_20ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_20ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_20WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_21	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_21ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_21ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_21ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_21ReadMask	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_21ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_21ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_21WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_22	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_22ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_22ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_22ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_22ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_22ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_22ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_22WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_23	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_23ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_23ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_23ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_23ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_23ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_23ResetValue	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_23WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_24	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_24ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_24ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_24ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_24ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_24ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_24ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_24WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_25	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_25ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_25ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_25ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_25ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_25ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_25ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_25WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_26	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_26ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_26ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_26ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_26ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_26ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_26ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_26WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_27	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_27ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_27ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_27ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_27ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_27ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_27ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_27WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_28	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_28ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_28ForcedBits	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_28ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_28ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_28ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_28ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_28WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_29	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_29ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_29ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_29ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_29ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_29ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_29ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_29WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_2ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_2ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_2ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_2ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_2ResetMask	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_2ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_2WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_3	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_30	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_30ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_30ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_30ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_30ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_30ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_30ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_30WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_31	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_31ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_31ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_31ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_31ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_31ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_31ResetValue	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_31WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_3ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_3ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_3ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_3ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_3ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_3ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_3WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_4	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_4ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_4ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_4ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_4ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_4ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_4ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_4WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_5	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_5ColdResetValue	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_5ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_5ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_5ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_5ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_5ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_5WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_6	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_6ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_6ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_6ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_6ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_6ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_6ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_6WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_7	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_7ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_7ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_7ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_7ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_7ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_7ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_7WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_8	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_8ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_8ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_8ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_8ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_8ResetMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_8ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_8WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_9	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_9ColdResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_9ForcedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_9ForcedFlippedBits	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_9ReadMask	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_9ResetMask	uint32_t	Virtual Channel RX Max Length Register

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Name	Type	Description
VCMAXLEN_9ResetValue	uint32_t	Virtual Channel RX Max Length Register
VCMAXLEN_9WriteMask	uint32_t	Virtual Channel RX Max Length Register
VCRXDADDR_0	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_0ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_0ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_0ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_0ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_0ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_0ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_0WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_1	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_10	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_10ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_10ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_10ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_10ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_10ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_10ResetValue	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_10WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_11	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_11ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_11ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_11ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_11ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_11ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_11ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_11WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_12	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_12ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_12ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_12ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_12ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_12ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_12ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_12WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_13	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_13ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_13ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_13ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_13ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_13ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_13ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_13WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_14	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_14ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_14ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_14ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_14ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_14ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_14ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_14WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_15	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_15ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_15ForcedBits	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_15ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_15ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_15ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_15ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_15WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_16	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_16ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_16ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_16ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_16ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_16ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_16ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_16WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_17	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_17ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_17ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_17ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_17ReadMask	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_17ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_17ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_17WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_18	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_18ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_18ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_18ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_18ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_18ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_18ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_18WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_19	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_19ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_19ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_19ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_19ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_19ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_19ResetValue	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_19WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_1ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_1ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_1ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_1ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_1ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_1ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_1WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_2	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_20	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_20ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_20ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_20ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_20ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_20ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_20ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_20WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_21	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_21ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_21ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_21ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_21ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_21ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_21ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_21WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_22	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_22ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_22ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_22ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_22ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_22ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_22ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_22WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_23	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_23ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_23ForcedBits	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_23ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_23ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_23ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_23ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_23WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_24	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_24ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_24ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_24ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_24ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_24ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_24ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_24WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_25	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_25ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_25ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_25ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_25ReadMask	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_25ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_25ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_25WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_26	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_26ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_26ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_26ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_26ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_26ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_26ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_26WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_27	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_27ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_27ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_27ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_27ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_27ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_27ResetValue	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_27WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_28	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_28ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_28ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_28ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_28ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_28ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_28ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_28WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_29	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_29ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_29ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_29ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_29ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_29ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_29ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_29WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_2ColdResetValue	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_2ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_2ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_2ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_2ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_2ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_2WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_3	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_30	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_30ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_30ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_30ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_30ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_30ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_30ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_30WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_31	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_31ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_31ForcedBits	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_31ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_31ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_31ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_31ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_31WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_3ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_3ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_3ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_3ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_3ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_3ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_3WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_4	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_4ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_4ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_4ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_4ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_4ResetMask	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_4ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_4WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_5	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_5ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_5ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_5ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_5ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_5ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_5ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_5WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_6	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_6ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_6ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_6ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_6ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_6ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_6ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_6WriteMask	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_7	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_7ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_7ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_7ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_7ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_7ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_7ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_7WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_8	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_8ColdResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_8ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_8ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_8ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_8ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_8ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_8WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_9	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_9ColdResetValue	uint32_t	VC RX Descriptor Table Address Register

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Name	Type	Description
VCRXDADDR_9ForcedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_9ForcedFlippedBits	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_9ReadMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_9ResetMask	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_9ResetValue	uint32_t	VC RX Descriptor Table Address Register
VCRXDADDR_9WriteMask	uint32_t	VC RX Descriptor Table Address Register
VCSTAT_0	uint32_t	Virtual Channel Status Register
VCSTAT_0ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_0ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_0ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_0ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_0ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_0ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_0WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_1	uint32_t	Virtual Channel Status Register
VCSTAT_10	uint32_t	Virtual Channel Status Register
VCSTAT_10ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_10ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_10ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_10ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_10ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_10ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_10WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_11	uint32_t	Virtual Channel Status Register
VCSTAT_11ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_11ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_11ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_11ReadMask	uint32_t	Virtual Channel Status Register

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Name	Type	Description
VCSTAT_11ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_11ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_11WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_12	uint32_t	Virtual Channel Status Register
VCSTAT_12ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_12ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_12ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_12ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_12ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_12ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_12WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_13	uint32_t	Virtual Channel Status Register
VCSTAT_13ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_13ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_13ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_13ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_13ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_13ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_13WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_14	uint32_t	Virtual Channel Status Register
VCSTAT_14ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_14ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_14ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_14ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_14ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_14ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_14WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_15	uint32_t	Virtual Channel Status Register
VCSTAT_15ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_15ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_15ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_15ReadMask	uint32_t	Virtual Channel Status Register

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Name	Type	Description
VCSTAT_15ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_15ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_15WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_16	uint32_t	Virtual Channel Status Register
VCSTAT_16ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_16ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_16ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_16ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_16ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_16ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_16WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_17	uint32_t	Virtual Channel Status Register
VCSTAT_17ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_17ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_17ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_17ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_17ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_17ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_17WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_18	uint32_t	Virtual Channel Status Register
VCSTAT_18ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_18ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_18ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_18ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_18ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_18ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_18WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_19	uint32_t	Virtual Channel Status Register
VCSTAT_19ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_19ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_19ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_19ReadMask	uint32_t	Virtual Channel Status Register

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Name	Type	Description
VCSTAT_19ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_19ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_19WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_1ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_1ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_1ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_1ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_1ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_1ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_1WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_2	uint32_t	Virtual Channel Status Register
VCSTAT_20	uint32_t	Virtual Channel Status Register
VCSTAT_20ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_20ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_20ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_20ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_20ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_20ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_20WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_21	uint32_t	Virtual Channel Status Register
VCSTAT_21ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_21ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_21ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_21ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_21ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_21ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_21WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_22	uint32_t	Virtual Channel Status Register
VCSTAT_22ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_22ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_22ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_22ReadMask	uint32_t	Virtual Channel Status Register

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Name	Type	Description
VCSTAT_22ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_22ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_22WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_23	uint32_t	Virtual Channel Status Register
VCSTAT_23ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_23ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_23ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_23ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_23ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_23ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_23WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_24	uint32_t	Virtual Channel Status Register
VCSTAT_24ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_24ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_24ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_24ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_24ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_24ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_24WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_25	uint32_t	Virtual Channel Status Register
VCSTAT_25ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_25ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_25ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_25ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_25ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_25ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_25WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_26	uint32_t	Virtual Channel Status Register
VCSTAT_26ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_26ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_26ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_26ReadMask	uint32_t	Virtual Channel Status Register

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Name	Type	Description
VCSTAT_26ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_26ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_26WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_27	uint32_t	Virtual Channel Status Register
VCSTAT_27ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_27ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_27ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_27ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_27ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_27ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_27WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_28	uint32_t	Virtual Channel Status Register
VCSTAT_28ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_28ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_28ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_28ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_28ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_28ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_28WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_29	uint32_t	Virtual Channel Status Register
VCSTAT_29ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_29ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_29ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_29ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_29ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_29ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_29WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_2ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_2ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_2ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_2ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_2ResetMask	uint32_t	Virtual Channel Status Register

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Name	Type	Description
VCSTAT_2ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_2WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_3	uint32_t	Virtual Channel Status Register
VCSTAT_30	uint32_t	Virtual Channel Status Register
VCSTAT_30ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_30ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_30ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_30ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_30ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_30ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_30WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_31	uint32_t	Virtual Channel Status Register
VCSTAT_31ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_31ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_31ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_31ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_31ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_31ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_31WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_3ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_3ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_3ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_3ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_3ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_3ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_3WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_4	uint32_t	Virtual Channel Status Register
VCSTAT_4ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_4ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_4ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_4ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_4ResetMask	uint32_t	Virtual Channel Status Register

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Name	Type	Description
VCSTAT_4ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_4WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_5	uint32_t	Virtual Channel Status Register
VCSTAT_5ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_5ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_5ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_5ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_5ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_5ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_5WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_6	uint32_t	Virtual Channel Status Register
VCSTAT_6ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_6ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_6ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_6ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_6ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_6ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_6WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_7	uint32_t	Virtual Channel Status Register
VCSTAT_7ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_7ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_7ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_7ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_7ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_7ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_7WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_8	uint32_t	Virtual Channel Status Register
VCSTAT_8ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_8ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_8ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_8ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_8ResetMask	uint32_t	Virtual Channel Status Register

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Name	Type	Description
VCSTAT_8ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_8WriteMask	uint32_t	Virtual Channel Status Register
VCSTAT_9	uint32_t	Virtual Channel Status Register
VCSTAT_9ColdResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_9ForcedBits	uint32_t	Virtual Channel Status Register
VCSTAT_9ForcedFlippedBits	uint32_t	Virtual Channel Status Register
VCSTAT_9ReadMask	uint32_t	Virtual Channel Status Register
VCSTAT_9ResetMask	uint32_t	Virtual Channel Status Register
VCSTAT_9ResetValue	uint32_t	Virtual Channel Status Register
VCSTAT_9WriteMask	uint32_t	Virtual Channel Status Register
VCTS1_0	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_0ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_0ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_0ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_0ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_0ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_0ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_0WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_1	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_10	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_10ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_10ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_10ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_10ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_10ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_10ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_10WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_11	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_11ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_11ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_11ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_11ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_11ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_11ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_11WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_12	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_12ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_12ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_12ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_12ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_12ResetMask	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_12ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_12WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_13	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_13ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_13ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_13ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_13ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_13ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_13ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_13WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_14	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_14ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_14ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_14ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_14ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_14ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_14ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_14WriteMask	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_15	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_15ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_15ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_15ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_15ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_15ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_15ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_15WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_16	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_16ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_16ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_16ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_16ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_16ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_16ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_16WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_17	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_17ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_17ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_17ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_17ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_17ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_17ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_17WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_18	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_18ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_18ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_18ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_18ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_18ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_18ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_18WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_19	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_19ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_19ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_19ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_19ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_19ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_19ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_19WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_1ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_1ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_1ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_1ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_1ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_1ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_1WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_2	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_20	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_20ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_20ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_20ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_20ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_20ResetMask	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_20ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_20WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_21	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_21ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_21ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_21ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_21ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_21ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_21ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_21WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_22	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_22ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_22ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_22ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_22ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_22ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_22ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_22WriteMask	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_23	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_23ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_23ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_23ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_23ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_23ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_23ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_23WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_24	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_24ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_24ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_24ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_24ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_24ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_24ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_24WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_25	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_25ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_25ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_25ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_25ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_25ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_25ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_25WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_26	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_26ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_26ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_26ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_26ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_26ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_26ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_26WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_27	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_27ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_27ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_27ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_27ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_27ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_27ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_27WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_28	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_28ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_28ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_28ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_28ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_28ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_28ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_28WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_29	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_29ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_29ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_29ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_29ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_29ResetMask	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_29ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_29WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_2ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_2ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_2ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_2ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_2ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_2ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_2WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_3	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_30	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_30ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_30ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_30ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_30ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_30ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_30ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_30WriteMask	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_31	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_31ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_31ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_31ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_31ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_31ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_31ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_31WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_3ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_3ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_3ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_3ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_3ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_3ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_3WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_4	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_4ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_4ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_4ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_4ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_4ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_4ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_4WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_5	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_5ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_5ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_5ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_5ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_5ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_5ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_5WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_6	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_6ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_6ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_6ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_6ReadMask	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_6ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_6ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_6WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_7	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_7ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_7ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_7ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_7ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_7ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_7ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_7WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_8	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_8ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_8ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_8ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_8ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_8ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_8ResetValue	uint32_t	Virtual Channel Time-slot 1 Register

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Name	Type	Description
VCTS1_8WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_9	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_9ColdResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_9ForcedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_9ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_9ReadMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_9ResetMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_9ResetValue	uint32_t	Virtual Channel Time-slot 1 Register
VCTS1_9WriteMask	uint32_t	Virtual Channel Time-slot 1 Register
VCTS2_0	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_0ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_0ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_0ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_0ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_0ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_0ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_0WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_1	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_10	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_10ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_10ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_10ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_10ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_10ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_10ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_10WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_11	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_11ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_11ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_11ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_11ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_11ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_11ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_11WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_12	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_12ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_12ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_12ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_12ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_12ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_12ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_12WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_13	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_13ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_13ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_13ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_13ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_13ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_13ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_13WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_14	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_14ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_14ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_14ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_14ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_14ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_14ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_14WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_15	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_15ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_15ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_15ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_15ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_15ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_15ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_15WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_16	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_16ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_16ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_16ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_16ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_16ResetMask	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_16ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_16WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_17	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_17ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_17ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_17ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_17ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_17ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_17ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_17WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_18	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_18ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_18ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_18ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_18ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_18ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_18ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_18WriteMask	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_19	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_19ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_19ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_19ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_19ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_19ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_19ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_19WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_1ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_1ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_1ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_1ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_1ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_1ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_1WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_2	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_20	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_20ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_20ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_20ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_20ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_20ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_20ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_20WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_21	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_21ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_21ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_21ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_21ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_21ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_21ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_21WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_22	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_22ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_22ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_22ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_22ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_22ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_22ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_22WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_23	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_23ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_23ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_23ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_23ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_23ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_23ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_23WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_24	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_24ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_24ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_24ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_24ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_24ResetMask	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_24ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_24WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_25	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_25ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_25ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_25ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_25ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_25ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_25ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_25WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_26	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_26ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_26ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_26ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_26ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_26ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_26ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_26WriteMask	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_27	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_27ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_27ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_27ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_27ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_27ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_27ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_27WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_28	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_28ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_28ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_28ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_28ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_28ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_28ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_28WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_29	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_29ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_29ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_29ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_29ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_29ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_29ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_29WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_2ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_2ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_2ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_2ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_2ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_2ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_2WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_3	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_30	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_30ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_30ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_30ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_30ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_30ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_30ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_30WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_31	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_31ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_31ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_31ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_31ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_31ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_31ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_31WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_3ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_3ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_3ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_3ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_3ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_3ResetValue	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_3WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_4	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_4ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_4ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_4ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_4ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_4ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_4ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_4WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_5	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_5ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_5ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_5ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_5ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_5ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_5ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_5WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_6	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_6ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_6ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_6ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_6ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_6ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_6ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_6WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_7	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_7ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_7ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_7ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_7ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_7ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_7ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_7WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_8	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_8ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_8ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register

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Name	Type	Description
VCTS2_8ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_8ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_8ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_8ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_8WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_9	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_9ColdResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_9ForcedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_9ForcedFlippedBits	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_9ReadMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_9ResetMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_9ResetValue	uint32_t	Virtual Channel Time-slot 2 Register
VCTS2_9WriteMask	uint32_t	Virtual Channel Time-slot 2 Register
VCTXDADDR_0	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_0ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_0ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_0ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_0ReadMask	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_0ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_0ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_0WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_1	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_10	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_10ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_10ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_10ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_10ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_10ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_10ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_10WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_11	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_11ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_11ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_11ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_11ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_11ResetMask	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_11ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_11WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_12	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_12ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_12ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_12ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_12ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_12ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_12ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_12WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_13	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_13ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_13ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_13ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_13ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_13ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_13ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_13WriteMask	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_14	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_14ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_14ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_14ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_14ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_14ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_14ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_14WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_15	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_15ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_15ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_15ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_15ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_15ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_15ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_15WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_16	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_16ColdResetValue	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_16ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_16ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_16ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_16ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_16ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_16WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_17	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_17ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_17ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_17ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_17ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_17ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_17ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_17WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_18	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_18ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_18ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_18ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_18ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_18ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_18ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_18WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_19	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_19ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_19ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_19ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_19ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_19ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_19ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_19WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_1ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_1ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_1ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_1ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_1ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_1ResetValue	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_1WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_2	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_20	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_20ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_20ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_20ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_20ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_20ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_20ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_20WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_21	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_21ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_21ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_21ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_21ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_21ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_21ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_21WriteMask	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_22	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_22ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_22ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_22ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_22ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_22ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_22ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_22WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_23	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_23ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_23ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_23ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_23ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_23ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_23ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_23WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_24	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_24ColdResetValue	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_24ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_24ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_24ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_24ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_24ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_24WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_25	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_25ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_25ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_25ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_25ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_25ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_25ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_25WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_26	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_26ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_26ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_26ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_26ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_26ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_26ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_26WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_27	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_27ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_27ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_27ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_27ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_27ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_27ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_27WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_28	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_28ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_28ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_28ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_28ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_28ResetMask	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_28ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_28WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_29	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_29ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_29ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_29ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_29ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_29ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_29ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_29WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_2ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_2ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_2ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_2ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_2ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_2ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_2WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_3	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_30	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_30ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_30ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_30ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_30ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_30ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_30ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_30WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_31	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_31ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_31ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_31ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_31ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_31ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_31ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_31WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_3ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_3ForcedBits	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_3ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_3ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_3ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_3ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_3WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_4	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_4ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_4ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_4ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_4ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_4ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_4ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_4WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_5	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_5ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_5ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_5ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_5ReadMask	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_5ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_5ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_5WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_6	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_6ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_6ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_6ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_6ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_6ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_6ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_6WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_7	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_7ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_7ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_7ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_7ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_7ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_7ResetValue	uint32_t	VC TX Descriptor Table Address Register

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Name	Type	Description
VCTXDADDR_7WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_8	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_8ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_8ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_8ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_8ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_8ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_8ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_8WriteMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_9	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_9ColdResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_9ForcedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_9ForcedFlippedBits	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_9ReadMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_9ResetMask	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_9ResetValue	uint32_t	VC TX Descriptor Table Address Register
VCTXDADDR_9WriteMask	uint32_t	VC TX Descriptor Table Address Register
config.flowControl	uint8_t	If set, model SpaceFibre virtual-channel flow control (FCT/credit).

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Name	Type	Description
config.irq	uint8_t	Interrupt number
config.littleEndian	uint8_t	Endianess of memory interface.
config.numDMAChannels	uint8_t	Number of DMA channels/engines available (1-8).
config.numExternalFIFOs	uint8_t	Number of external FIFO interfaces available (0-32).
config.numRXDescs	uint32_t	Number of RX descriptors held in VCRXDADDR tables (128, 256, 512 or 1024).
config.numTXDescs	uint32_t	Number of TX descriptors held in VCTXDADDR tables (64, 128, 256 or 512).
config.numVirtualChannels	uint8_t	Number of virtual channels available (1-32).
config.transmitter.infiniteSpeed	uint8_t	If set, packets are delivered instantly (no link timing).
config.transmitter.lineRate	uint64_t	Aggregate SpaceFibre transmitter line rate in bits/s (8b/10b encoded). Used to model packet delivery time.
externalFIFOs	[temu_IfaceRef; 32]/ <unknown>	External FIFO interfaces (e.g. for connections to the GRSPWROUTER)
internal.linkBusy	uint8_t	Whether the physical link is currently transmitting.
internal.linkPending.active	uint8_t	An in-flight link transmission is present.
internal.linkPending.channel	uint8_t	In-flight packet channel.
internal.linkPending.data	temu_Buff	In-flight link transmission payload.
internal.linkPending.descAddr	uint32_t	TX descriptor address to write back on completion.
internal.linkPending.descInterruptEnable	uint8_t	In-flight TX raises an interrupt.
internal.linkPending.descWord0	uint32_t	TX descriptor word 0 to write back on completion.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
internal.linkPending.dmaEngineIdx	uint32_t	Owning DMA engine of the in-flight TX.
internal.linkPending.flags	uint32_t	In-flight packet flags.
internal.linkPending.isBroadcast	uint8_t	In-flight transmission is a broadcast.
internal.linkPending.type	uint8_t	In-flight packet broadcast type.
internal.linkPending.vcIndex	uint32_t	Owning virtual channel of the in-flight TX.
internal.nextTxVC	uint32_t	Round-robin TX arbitration cursor.
internal.rxCreditGranted	[uint32_t; 32]	Per-VC outstanding RX credit granted to the peer, in bytes.
internal.txCredit	[uint32_t; 32]	Per-VC transmit credit in bytes.
irqCtrl	temu_IfaceRef/ <unknown>	IRQ controller.
packetQueues	[temu_Vector; 33]	Reception Packet queues
pnp.bar	uint32_t	AMBA plug and play base address register
pnp.config	uint32_t	AMBA plug and play config word

Interfaces

Name	Type	Description
ApbIface	ApbIface	APB P&P interface.
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
SpfiPortIface	temu::SpfiPortIface	SpaceFibre Port Interface of this device.

Commands

Name	Description
delete	Dispose instance of GRSPFI

9.28.5. Limitations

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

GRSPFI ignores any incoming flow control token (FTC) control words, and does not send out any FTCs either.

It has a virtually infinitely large receive buffer for every virtual channel, but will never send out any FTCs to the other end in order to communicate that.

When GRSPFI sends out packets, it will ignore any FTCs received for the channel it wants to send over. Even if the other side indicates that this channel has ran out of credits for a VC, GRSPFI will send packets.

9.29. SPICTRL

The SPICTRL device is part of the GRLIB IP library. It is available in `libTEMUSPICTRL.so`.

9.29.1. Loading the Plugin

```
import SPICTRL
```

9.29.2. Configuration

After instantiating an object set the capability registers to the desired configuration. Do not change the capability registers during operation.

9.29.3. @SPICTRL Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Commands

Name	Description
delete	Dispose instance of @SPICTRL
new	Create new instance of SPICTRL

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

9.29.4. SPICTRL Reference

Properties

Name	Type	Description
AMCFG	uint32_t	AM configuration register
AMCFGColdResetValue	uint32_t	AM configuration register
AMCFGForcedBits	uint32_t	AM configuration register
AMCFGForcedFlippedBits	uint32_t	AM configuration register
AMCFGReadMask	uint32_t	AM configuration register
AMCFGResetMask	uint32_t	AM configuration register
AMCFGResetValue	uint32_t	AM configuration register
AMCFGWriteMask	uint32_t	AM configuration register
AMPER	uint32_t	AM period register
AMPERColdResetValue	uint32_t	AM period register
AMPERForcedBits	uint32_t	AM period register
AMPERForcedFlippedBits	uint32_t	AM period register
AMPERReadMask	uint32_t	AM period register
AMPERResetMask	uint32_t	AM period register
AMPERResetValue	uint32_t	AM period register
AMPERWriteMask	uint32_t	AM period register
ASLVSEL	uint32_t	Automatic slave select register
ASLVSELColdResetValue	uint32_t	Automatic slave select register
ASLVSELForcedBits	uint32_t	Automatic slave select register
ASLVSELForcedFlippedBits	uint32_t	Automatic slave select register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ASLVSELReadMask	uint32_t	Automatic slave select register
ASLVSELResetMask	uint32_t	Automatic slave select register
ASLVSELResetValue	uint32_t	Automatic slave select register
ASLVSELWriteMask	uint32_t	Automatic slave select register
CAP0	uint32_t	Capability register 0
CAP1	uint32_t	Capability register 1
CAP2ColdResetValue	uint32_t	Capability register 1
CAP2ForcedBits	uint32_t	Capability register 1
CAP2ForcedFlippedBits	uint32_t	Capability register 1
CAP2ReadMask	uint32_t	Capability register 1
CAP2ResetMask	uint32_t	Capability register 1
CAP2ResetValue	uint32_t	Capability register 1
CAP2WriteMask	uint32_t	Capability register 1
CAPColdResetValue	uint32_t	Capability register 0
CAPForcedBits	uint32_t	Capability register 0
CAPForcedFlippedBits	uint32_t	Capability register 0
CAPReadMask	uint32_t	Capability register 0
CAPResetMask	uint32_t	Capability register 0
CAPResetValue	uint32_t	Capability register 0
CAPWriteMask	uint32_t	Capability register 0
CMD	uint32_t	Command register
CMDColdResetValue	uint32_t	Command register
CMDForcedBits	uint32_t	Command register
CMDForcedFlippedBits	uint32_t	Command register
CMDReadMask	uint32_t	Command register
CMDResetMask	uint32_t	Command register
CMDResetValue	uint32_t	Command register
CMDWriteMask	uint32_t	Command register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
EVENT	uint32_t	Event register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
EVENTColdResetValue	uint32_t	Event register
EVENTForcedBits	uint32_t	Event register
EVENTForcedFlippedBits	uint32_t	Event register
EVENTReadMask	uint32_t	Event register
EVENTResetMask	uint32_t	Event register
EVENTResetValue	uint32_t	Event register
EVENTWriteMask	uint32_t	Event register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
MASK	uint32_t	Mask register
MASKColdResetValue	uint32_t	Mask register
MASKForcedBits	uint32_t	Mask register
MASKForcedFlippedBits	uint32_t	Mask register
MASKReadMask	uint32_t	Mask register
MASKResetMask	uint32_t	Mask register
MASKResetValue	uint32_t	Mask register
MASKWriteMask	uint32_t	Mask register
MODE	uint32_t	Mode register
MODEColdResetValue	uint32_t	Mode register
MODEForcedBits	uint32_t	Mode register
MODEForcedFlippedBits	uint32_t	Mode register
MODEReadMask	uint32_t	Mode register
MODEResetMask	uint32_t	Mode register
MODEResetValue	uint32_t	Mode register
MODEWriteMask	uint32_t	Mode register
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
RXC	uint32_t	Receive register
RXCColdResetValue	uint32_t	Receive register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
RXCForcedBits	uint32_t	Receive register
RXCForcedFlippedBits	uint32_t	Receive register
RXCReadMask	uint32_t	Receive register
RXCResetMask	uint32_t	Receive register
RXCResetValue	uint32_t	Receive register
RXCWriteMask	uint32_t	Receive register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
SLVSEL	uint32_t	Slave select register
SLVSELColdResetValue	uint32_t	Slave select register
SLVSELForcedBits	uint32_t	Slave select register
SLVSELForcedFlippedBits	uint32_t	Slave select register
SLVSELReadMask	uint32_t	Slave select register
SLVSELResetMask	uint32_t	Slave select register
SLVSELResetValue	uint32_t	Slave select register
SLVSELWriteMask	uint32_t	Slave select register
TX	uint32_t	Transmit register
TXColdResetValue	uint32_t	Transmit register
TXForcedBits	uint32_t	Transmit register
TXForcedFlippedBits	uint32_t	Transmit register
TXReadMask	uint32_t	Transmit register
TXResetMask	uint32_t	Transmit register
TXResetValue	uint32_t	Transmit register
TXWriteMask	uint32_t	Transmit register
TimeSource	*void	Time source object
chipNumber	uint8_t	chipSelect ID of the device
config.irq	uint8_t	Interrupt number
irqCtrl	temu_IfaceRef/ <unknown>	IRQ controller.
pnp.bar	uint32_t	AMBA plug and play base address register
pnp.config	uint32_t	AMBA plug and play config word
rxFifo	temu_Vector	RX FIFO

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
spiBus	temu_IfaceRef/ <unknown>	Spi bus
txFifo	temu_Vector	TX FIFO

Interfaces

Name	Type	Description
ApbIface	ApbIface	APB P&P interface.
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
SpiSlaveDevice2Iface	temu::SpiSlaveDevice2Iface	Communication interface.

Registers



Register support is currently experimental!

Register Bank Regs

Register CAP

Description

Capability register 0

Reset value

0x020b0485

Warm reset mask

0xffffffff

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSSZ								MAXWLEN				TWEN	AMODE	ASELA	SSEN	FDEPTH								SR	FT		REV				
ro								ro				ro	ro	ro	ro	ro								ro	ro		ro				
2								0				1	0	1	1	4								1	0		5				

Field	Mask	Reset	Description
SSSZ	0xff000000	0x2	Slave Select register size
MAXWLEN	0x00f00000	0x0	Maximum word length
TWEN	0x00080000	0x1	Three-wire mode enable
AMODE	0x00040000	0x0	Auto mode
ASELA	0x00020000	0x1	Automatic slave select available
SSEN	0x00010000	0x1	Slave Select enable

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
FDEPTH	0x0000ff00	0x4	FIFO depth
SR	0x00000080	0x1	Syncram
FT	0x00000060	0x0	Fault-tolerance
REV	0x0000001f	0x5	Core revision

Register CAP2

Description

Capability register 1

Reset value

0x00000000

Warm reset mask

0x00000003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																														PROT	
-																														ro	
-																														0	

Field	Mask	Reset	Description
PROT	0x00000003	0x0	Supported protocol

Register MODE

Description

Mode register

Reset value

0x00000000

Warm reset mask

0x7ffffffe

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	LOOP	CPOL	CPHA	DIV16	REV	MS	EN	LEN				PM				TW	ASEL	FACT	OD	CG					ASELDEL		TAC	TTO	IGSEL	CITE	-
-	rw	rw	rw	rw	rw	rw	rw	rw				rw				rw	rw	rw	rw	rw					rw		rw	rw	rw	rw	-
-	0	0	0	0	0	0	0	0				0				0	0	0	0	0					0		0	0	0	0	-

Field	Mask	Reset	Description
LOOP	0x40000000	0x0	Loop mode
CPOL	0x20000000	0x0	Clock polarity
CPHA	0x10000000	0x0	Clock phase
DIV16	0x08000000	0x0	Divide by 16

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
REV	0x04000000	0x0	Reverse data
MS	0x02000000	0x0	Master/Slave
EN	0x01000000	0x0	Enable core
LEN	0x00f00000	0x0	Word length
PM	0x000f0000	0x0	Prescale modulus
TW	0x00008000	0x0	Three-wire mode
ASEL	0x00004000	0x0	Automatic slave select
FACT	0x00002000	0x0	PM factor
OD	0x00001000	0x0	Open drain mode
CG	0x00000f80	0x0	Clock gap
ASELDEL	0x00000060	0x0	Automatic slave select delay
TAC	0x00000010	0x0	Toggle automatic slave select during clock gap
TTO	0x00000008	0x0	3-wire transfer order
IGSEL	0x00000004	0x0	Ignore SPISEL input
CITE	0x00000002	0x0	Require clock idle for transfer end

Register EVENT

Description

Event register

Reset value

0x00000000

Warm reset mask

0x80000300

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIP	-																LT	-	OV	UN	MME	NE	NF	-							
ro	-																rw	-	rw	rw	rw	ro	ro	-							
0	-																-	-	-	-	-	0	0	-							

Field	Mask	Reset	Description
TIP	0x80000000	0x0	Transfer in progress
LT	0x00004000	-	Last character
OV	0x00001000	-	Overrun
UN	0x00000800	-	Underrun
MME	0x00000400	-	Multiple-master error

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
NE	0x00000200	0x0	Not empty
NF	0x00000100	0x0	Not full

Register MASK

Description

Mask register

Reset value

0x00000000

Warm reset mask

0x80005f00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIPE	-																LTE	-	OVE	UNE	MMEE	NEE	NFE	-							
rw	-																rw	-	rw	rw	rw	rw	rw	-							
0	-																0	-	0	0	0	0	0	-							

Field	Mask	Reset	Description
TIPE	0x80000000	0x0	Transfer in progress enable
LTE	0x00004000	0x0	Last character enable
OVE	0x00001000	0x0	Overrun enable
UNE	0x00000800	0x0	Underrun enable
MMEE	0x00000400	0x0	Multiple-master error enable
NEE	0x00000200	0x0	Not empty enable
NFE	0x00000100	0x0	Not full enable

Register CMD

Description

Command register

Reset value

0x00000000

Warm reset mask

0x00000007

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-									LST	-																		PGRD	DIR	SPROT	
-									wo	-																		wo	rw	rw	
-									-	-																		-	0	0	

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
LST	0x00400000	-	Last
PGRD	0x00000008	-	Protocol guard
DIR	0x00000004	0x0	Direction
SPROT	0x00000003	0x0	SPI protocol

Register TX

Description

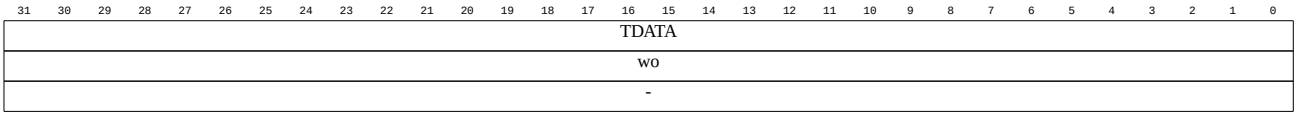
Transmit register

Reset value

0x00000000

Warm reset mask

0x00000000



Field	Mask	Reset	Description
TDATA	0xffffffff	-	Transmit data

Register RXC

Description

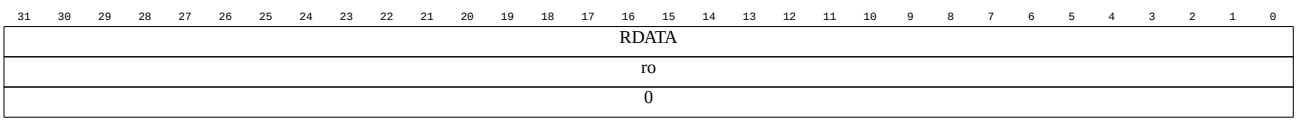
Receive register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
RDATA	0xffffffff	0x0	Receive data

Register SLVSEL

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Description

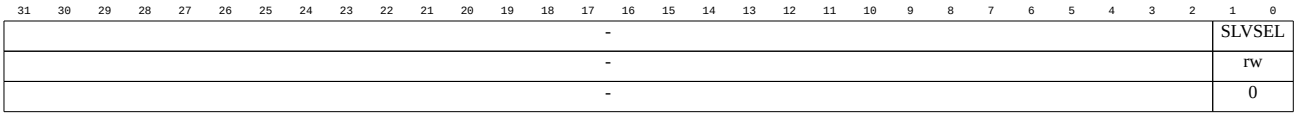
Slave select register

Reset value

0x00000000

Warm reset mask

0x00000003



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																														SLVSEL	
-																														rw	
-																														0	

Field	Mask	Reset	Description
SLVSEL	0x00000003	0x0	Slave select

Register ASLVSEL

Description

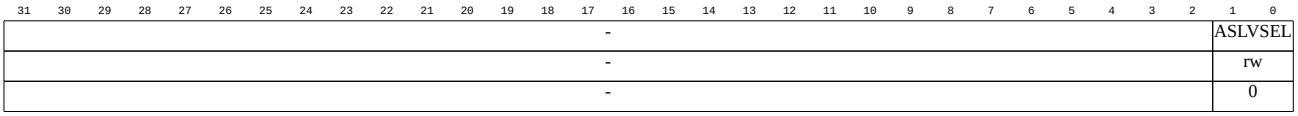
Automatic slave select register

Reset value

0x00000000

Warm reset mask

0x00000003



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																														ASLVSEL	
-																														rw	
-																														0	

Field	Mask	Reset	Description
ASLVSEL	0x00000003	0x0	Automatic slave select

Register AMCFG

Description

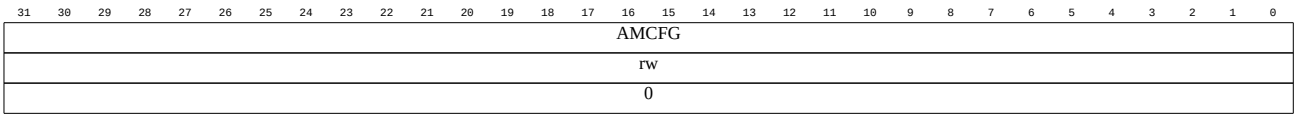
AM configuration register

Reset value

0x00000000

Warm reset mask

0xffffffff



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AMCFG																															
rw																															
0																															

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Field	Mask	Reset	Description
AMCFG	0xffffffff	0x0	Automatic mode configuration

Register AMPER

Description

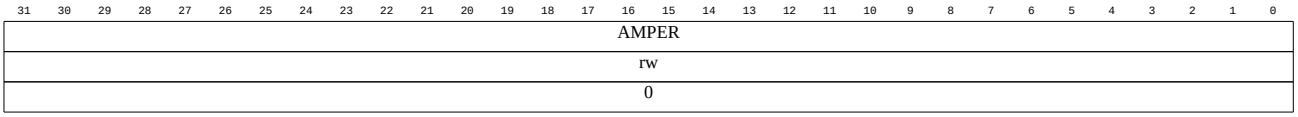
AM period register

Reset value

0x00000000

Warm reset mask

0xffffffff



Field	Mask	Reset	Description
AMPER	0xffffffff	0x0	Automatic mode period

Commands

Name	Description
delete	Dispose instance of SPICTRL

9.29.5. Limitations

- Transmission delays and other timing effects are not modelled
- The Slave Select functionality is not implemented
- Automated periodic transfers are not implemented
- Fault tolerance capabilities are not modelled

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Chapter 10. P2020

10.1. CCSRGU

This section describes the model of the P2020 CCSR General Utilities model. The device models the General Utilities part in CCSR space. CCSRGU includes the local configuration control and local access parts, handling the remapping of the dynamic physical address space.

10.1.1. Loading the Plugin

```
import P2020
```

10.1.2. Configuration

10.1.3. @CCSRGU Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @CCSRGU
new	Create new instance of CCSRGU

Command new Arguments

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Required	Description
name	string	yes	Name of object to create

10.1.4. CCSRGU Reference

Properties

Name	Type	Description
ALTCAR	uint32_t	Alternate configuration attribute register
ALTCARColdResetValue	uint32_t	Alternate configuration attribute register
ALTCARForcedBits	uint32_t	Alternate configuration attribute register
ALTCARForcedFlippedBits	uint32_t	Alternate configuration attribute register
ALTCARReadMask	uint32_t	Alternate configuration attribute register
ALTCARResetMask	uint32_t	Alternate configuration attribute register
ALTCARResetValue	uint32_t	Alternate configuration attribute register
ALTCARWriteMask	uint32_t	Alternate configuration attribute register
ALTCBAR	uint32_t	Alternate configuration base address register
ALTCBARColdResetValue	uint32_t	Alternate configuration base address register
ALTCBARForcedBits	uint32_t	Alternate configuration base address register
ALTCBARForcedFlippedBits	uint32_t	Alternate configuration base address register
ALTCBARReadMask	uint32_t	Alternate configuration base address register
ALTCBARResetMask	uint32_t	Alternate configuration base address register
ALTCBARResetValue	uint32_t	Alternate configuration base address register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ALTCBARWriteMask	uint32_t	Alternate configuration base address register
BPTR	uint32_t	Boot page translation register
BPTRColdResetValue	uint32_t	Boot page translation register
BPTRForcedBits	uint32_t	Boot page translation register
BPTRForcedFlippedBits	uint32_t	Boot page translation register
BPTRReadMask	uint32_t	Boot page translation register
BPTRResetMask	uint32_t	Boot page translation register
BPTRResetValue	uint32_t	Boot page translation register
BPTRWriteMask	uint32_t	Boot page translation register
CCSRBAR	uint32_t	Configuration, control, and status registers base address register
CCSRBARColdResetValue	uint32_t	Configuration, control, and status registers base address register
CCSRBARForcedBits	uint32_t	Configuration, control, and status registers base address register
CCSRBARForcedFlippedBits	uint32_t	Configuration, control, and status registers base address register
CCSRBARReadMask	uint32_t	Configuration, control, and status registers base address register
CCSRBARResetMask	uint32_t	Configuration, control, and status registers base address register
CCSRBARResetValue	uint32_t	Configuration, control, and status registers base address register
CCSRBARWriteMask	uint32_t	Configuration, control, and status registers base address register
Class	*void	Class object
Component	*void	Pointer to component object if part of component

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LAWAR	[uint32_t; 12]	Local access window attribute register
LAWBAR	[uint32_t; 12]	Local access window base address register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
ddr	temu_IfaceRef/ <unknown>	DDR memory controller
ddrCtrl	temu_IfaceRef/ <unknown>	DDR registers.
dmaCtrl	[temu_IfaceRef; 2]/ <unknown>	DMA registers
duartCtrl	[temu_IfaceRef; 2]/ <unknown>	DUART registers
ecmCtrl	temu_IfaceRef/ <unknown>	ECM registers
elbc	temu_IfaceRef/ <unknown>	Enhanced local bus
elbcCtrl	temu_IfaceRef/ <unknown>	eLBC registers
esdhcCtrl	temu_IfaceRef/ <unknown>	eSDHC registers
espiCtrl	temu_IfaceRef/ <unknown>	eSPI registers
etsecCtrl	[temu_IfaceRef; 3]/ <unknown>	eTSEC registers
globalUtilitiesCtrl	temu_IfaceRef/ <unknown>	Global utilities registers
gpioCtrl	temu_IfaceRef/ <unknown>	GPIO registers
i2cCtrl	temu_IfaceRef/ <unknown>	I2C registers
l2CacheCtrl	temu_IfaceRef/ <unknown>	L2 Cache regsiters
localAccess	temu_IfaceRef/ <unknown>	Reference to device itself
memSpace	temu_IfaceRef/ <unknown>	Memory space
pci	[temu_IfaceRef; 3]/ <unknown>	PCI bridges
pcixCtrl	[temu_IfaceRef; 3]/ <unknown>	PCIx registers
picCtrl	temu_IfaceRef/ <unknown>	PIC registers

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Name	Type	Description
secCtrl	temu_IfaceRef/ <unknown>	SEC registers
srio	[temu_IfaceRef; 2]/ <unknown>	SRIO
usbCtrl	temu_IfaceRef/ <unknown>	USB registers

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	Device Interface
MemAccessIface	MemAccessIface	Memory access interface
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	Reset Interface

Commands

Name	Description
delete	Dispose instance of CCSRGU

10.1.5. Limitations

10.2. DDR

This section describes the DDR controller model.

The model supports the handling of SEU and MEU events (i.e. correctable and uncorrectable ECC errors). Such events will update the counters and raise interrupts accordingly.

10.2.1. Loading the Plugin

```
import P2020
```

10.2.2. Configuration

To use SEU and MEU events connect the memoryspace upset/faulty handlers to the DDR model and allow interrupts as follows:

Listing 26. Connecting SEU and MEU events via Command Line

```
# Connect the memoryspace upset/faulty handlers to the ddr
connect a=mem.upsetHandlers b=ddr:CorrectableErrorIface
connect a=mem.faultyHandlers b=ddr:UncorrectableErrorIface
```

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```
# Enable ECC error interrupts
ddr.ERR_INT_EN = 0x0000000c

# Set/clear faulty attribute on the given memory range
memory-set-faulty addr=0x08 obj=mem
memory-clear-faulty addr=0x08 obj=mem

# Set/clear upset attribute on the given memory range
memory-set-upset addr=0x08 obj=mem
memory-clear-upset addr=0x08 obj=mem
```

Listing 27. Connecting SEU and MEU events via API

```
// Connect the memoryspace upset/faulty handlers to the ddr
temu_connect(mem, "upsetHandlers", ddr, "CorrectableErrorIface");
temu_connect(mem, "faultyHandlers", ddr, "UncorrectableErrorIface");

// Enable ECC error interrupts
temu_writeValueU32(ddr, "ERR_INT_EN", 0x0000000c, 0);

// Set/clear faulty attribute on the given memory range
temu_memorySetAttr(mem, 0x08, 4, teMA_Faulty);
temu_memoryClearAttr(mem, 0x08, 4, teMA_Faulty);

// Set/clear upset attribute on the given memory range
temu_memorySetAttr(mem, 0x08, 4, teMA_Upset);
temu_memoryClearAttr(mem, 0x08, 4, teMA_Upset);
```

10.2.3. @DDR Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.

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Name	Type	Description
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @DDR
new	Create new instance of DDR

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

10.2.4. DDR Reference

Properties

Name	Type	Description
CAPTURE_ADDRESS	uint32_t	Memory error address capture
CAPTURE_ADDRESSColdResetValue	uint32_t	Memory error address capture
CAPTURE_ADDRESSForcedBits	uint32_t	Memory error address capture
CAPTURE_ADDRESSForcedFlippedBits	uint32_t	Memory error address capture
CAPTURE_ADDRESSReadMask	uint32_t	Memory error address capture
CAPTURE_ADDRESSResetMask	uint32_t	Memory error address capture
CAPTURE_ADDRESSResetValue	uint32_t	Memory error address capture
CAPTURE_ADDRESSWriteMask	uint32_t	Memory error address capture
CAPTURE_ATTRIBUTES	uint32_t	Memory error attributes capture
CAPTURE_ATTRIBUTESColdResetValue	uint32_t	Memory error attributes capture
CAPTURE_ATTRIBUTESForcedBits	uint32_t	Memory error attributes capture

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Name	Type	Description
CAPTURE_ATTRIBUTESForcedFlippedBits	uint32_t	Memory error attributes capture
CAPTURE_ATTRIBUTESReadMask	uint32_t	Memory error attributes capture
CAPTURE_ATTRIBUTESResetMask	uint32_t	Memory error attributes capture
CAPTURE_ATTRIBUTESResetValue	uint32_t	Memory error attributes capture
CAPTURE_ATTRIBUTESWriteMask	uint32_t	Memory error attributes capture
CAPTURE_DATA_HI	uint32_t	Memory data path read capture high
CAPTURE_DATA_HIColdResetValue	uint32_t	Memory data path read capture high
CAPTURE_DATA_HIForcedBits	uint32_t	Memory data path read capture high
CAPTURE_DATA_HIForcedFlippedBits	uint32_t	Memory data path read capture high
CAPTURE_DATA_HIReadMask	uint32_t	Memory data path read capture high
CAPTURE_DATA_HIResetMask	uint32_t	Memory data path read capture high
CAPTURE_DATA_HIResetValue	uint32_t	Memory data path read capture high
CAPTURE_DATA_HIWriteMask	uint32_t	Memory data path read capture high
CAPTURE_DATA_LO	uint32_t	Memory data path read capture low
CAPTURE_DATA_LOColdResetValue	uint32_t	Memory data path read capture low
CAPTURE_DATA_LOForcedBits	uint32_t	Memory data path read capture low
CAPTURE_DATA_LOForcedFlippedBits	uint32_t	Memory data path read capture low
CAPTURE_DATA_LOReadMask	uint32_t	Memory data path read capture low

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Name	Type	Description
CAPTURE_DATA_LOResetMask	uint32_t	Memory data path read capture low
CAPTURE_DATA_LOResetValue	uint32_t	Memory data path read capture low
CAPTURE_DATA_LOWriteMask	uint32_t	Memory data path read capture low
CAPTURE_ECC	uint32_t	Memory data path read capture ECC
CAPTURE_ECCColdResetValue	uint32_t	Memory data path read capture ECC
CAPTURE_ECCForcedBits	uint32_t	Memory data path read capture ECC
CAPTURE_ECCForcedFlippedBits	uint32_t	Memory data path read capture ECC
CAPTURE_ECCReadMask	uint32_t	Memory data path read capture ECC
CAPTURE_ECCResetMask	uint32_t	Memory data path read capture ECC
CAPTURE_ECCResetValue	uint32_t	Memory data path read capture ECC
CAPTURE_ECCWriteMask	uint32_t	Memory data path read capture ECC
CAPTURE_EXT_ADDRESS	uint32_t	Memory error extended address capture
CAPTURE_EXT_ADDRESSColdResetValue	uint32_t	Memory error extended address capture
CAPTURE_EXT_ADDRESSForcedBits	uint32_t	Memory error extended address capture
CAPTURE_EXT_ADDRESSForcedFlippedBits	uint32_t	Memory error extended address capture
CAPTURE_EXT_ADDRESSReadMask	uint32_t	Memory error extended address capture
CAPTURE_EXT_ADDRESSResetMask	uint32_t	Memory error extended address capture
CAPTURE_EXT_ADDRESSResetValue	uint32_t	Memory error extended address capture

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
CAPTURE_EXT_ADDRESSWriteMask	uint32_t	Memory error extended address capture
CS_BNDS	[uint32_t; 4]	Chip select memory bounds register
CS_CONFIG	[uint32_t; 4]	Chip select configuration register
CS_CONFIG_2	[uint32_t; 4]	Chip select configuration 2 register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
DATA_ERR_INJECT_HI	uint32_t	Memory data path error injection mask high
DATA_ERR_INJECT_HIColdResetValue	uint32_t	Memory data path error injection mask high
DATA_ERR_INJECT_HIForcedBits	uint32_t	Memory data path error injection mask high
DATA_ERR_INJECT_HIForcedFlippedBits	uint32_t	Memory data path error injection mask high
DATA_ERR_INJECT_HIReadMask	uint32_t	Memory data path error injection mask high
DATA_ERR_INJECT_HIResetMask	uint32_t	Memory data path error injection mask high
DATA_ERR_INJECT_HIResetValue	uint32_t	Memory data path error injection mask high
DATA_ERR_INJECT_HIWriteMask	uint32_t	Memory data path error injection mask high
DATA_ERR_INJECT_LO	uint32_t	Memory data path error injection mask low
DATA_ERR_INJECT_LOColdResetValue	uint32_t	Memory data path error injection mask low
DATA_ERR_INJECT_LOForcedBits	uint32_t	Memory data path error injection mask low
DATA_ERR_INJECT_LOForcedFlippedBits	uint32_t	Memory data path error injection mask low
DATA_ERR_INJECT_LOReadMask	uint32_t	Memory data path error injection mask low

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DATA_ERR_INJECT_LOResetMask	uint32_t	Memory data path error injection mask low
DATA_ERR_INJECT_LOResetValue	uint32_t	Memory data path error injection mask low
DATA_ERR_INJECT_LOWriteMask	uint32_t	Memory data path error injection mask low
DATA_INIT	uint32_t	DDR SDRAM data initialization
DATA_INITColdResetValue	uint32_t	DDR SDRAM data initialization
DATA_INITForcedBits	uint32_t	DDR SDRAM data initialization
DATA_INITForcedFlippedBits	uint32_t	DDR SDRAM data initialization
DATA_INITReadMask	uint32_t	DDR SDRAM data initialization
DATA_INITResetMask	uint32_t	DDR SDRAM data initialization
DATA_INITResetValue	uint32_t	DDR SDRAM data initialization
DATA_INITWriteMask	uint32_t	DDR SDRAM data initialization
DDRCDR_1	uint32_t	DDR control driver register 1
DDRCDR_1ColdResetValue	uint32_t	DDR control driver register 1
DDRCDR_1ForcedBits	uint32_t	DDR control driver register 1
DDRCDR_1ForcedFlippedBits	uint32_t	DDR control driver register 1
DDRCDR_1ReadMask	uint32_t	DDR control driver register 1
DDRCDR_1ResetMask	uint32_t	DDR control driver register 1
DDRCDR_1ResetValue	uint32_t	DDR control driver register 1
DDRCDR_1WriteMask	uint32_t	DDR control driver register 1
DDRCDR_2	uint32_t	DDR control driver register 2
DDRCDR_2ColdResetValue	uint32_t	DDR control driver register 2
DDRCDR_2ForcedBits	uint32_t	DDR control driver register 2
DDRCDR_2ForcedFlippedBits	uint32_t	DDR control driver register 2
DDRCDR_2ReadMask	uint32_t	DDR control driver register 2
DDRCDR_2ResetMask	uint32_t	DDR control driver register 2
DDRCDR_2ResetValue	uint32_t	DDR control driver register 2
DDRCDR_2WriteMask	uint32_t	DDR control driver register 2
DDRDSR_1	uint32_t	DDR debug status register 1
DDRDSR_1ColdResetValue	uint32_t	DDR debug status register 1
DDRDSR_1ForcedBits	uint32_t	DDR debug status register 1

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Name	Type	Description
DDRDSR_1ForcedFlippedBits	uint32_t	DDR debug status register 1
DDRDSR_1ReadMask	uint32_t	DDR debug status register 1
DDRDSR_1ResetMask	uint32_t	DDR debug status register 1
DDRDSR_1ResetValue	uint32_t	DDR debug status register 1
DDRDSR_1WriteMask	uint32_t	DDR debug status register 1
DDRDSR_2	uint32_t	DDR debug status register 2
DDRDSR_2ColdResetValue	uint32_t	DDR debug status register 2
DDRDSR_2ForcedBits	uint32_t	DDR debug status register 2
DDRDSR_2ForcedFlippedBits	uint32_t	DDR debug status register 2
DDRDSR_2ReadMask	uint32_t	DDR debug status register 2
DDRDSR_2ResetMask	uint32_t	DDR debug status register 2
DDRDSR_2ResetValue	uint32_t	DDR debug status register 2
DDRDSR_2WriteMask	uint32_t	DDR debug status register 2
ERR_DETECT	uint32_t	Memory error detect
ERR_DETECTColdResetValue	uint32_t	Memory error detect
ERR_DETECTForcedBits	uint32_t	Memory error detect
ERR_DETECTForcedFlippedBits	uint32_t	Memory error detect
ERR_DETECTReadMask	uint32_t	Memory error detect
ERR_DETECTResetMask	uint32_t	Memory error detect
ERR_DETECTResetValue	uint32_t	Memory error detect
ERR_DETECTWriteMask	uint32_t	Memory error detect
ERR_DISABLE	uint32_t	Memory error disable
ERR_DISABLEColdResetValue	uint32_t	Memory error disable
ERR_DISABLEForcedBits	uint32_t	Memory error disable
ERR_DISABLEForcedFlippedBits	uint32_t	Memory error disable
ERR_DISABLEReadMask	uint32_t	Memory error disable
ERR_DISABLEResetMask	uint32_t	Memory error disable
ERR_DISABLEResetValue	uint32_t	Memory error disable
ERR_DISABLEWriteMask	uint32_t	Memory error disable
ERR_INJECT	uint32_t	Memory data path error injection mask ECC

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Name	Type	Description
ERR_INJECTColdResetValue	uint32_t	Memory data path error injection mask ECC
ERR_INJECTForcedBits	uint32_t	Memory data path error injection mask ECC
ERR_INJECTForcedFlippedBits	uint32_t	Memory data path error injection mask ECC
ERR_INJECTReadMask	uint32_t	Memory data path error injection mask ECC
ERR_INJECTResetMask	uint32_t	Memory data path error injection mask ECC
ERR_INJECTResetValue	uint32_t	Memory data path error injection mask ECC
ERR_INJECTWriteMask	uint32_t	Memory data path error injection mask ECC
ERR_INT_EN	uint32_t	Memory error interrupt enable
ERR_INT_ENColdResetValue	uint32_t	Memory error interrupt enable
ERR_INT_ENForcedBits	uint32_t	Memory error interrupt enable
ERR_INT_ENForcedFlippedBits	uint32_t	Memory error interrupt enable
ERR_INT_ENReadMask	uint32_t	Memory error interrupt enable
ERR_INT_ENResetMask	uint32_t	Memory error interrupt enable
ERR_INT_ENResetValue	uint32_t	Memory error interrupt enable
ERR_INT_ENWriteMask	uint32_t	Memory error interrupt enable
ERR_SBE	uint32_t	Single-bit ECC memory error management
ERR_SBEColdResetValue	uint32_t	Single-bit ECC memory error management
ERR_SBEForcedBits	uint32_t	Single-bit ECC memory error management
ERR_SBEForcedFlippedBits	uint32_t	Single-bit ECC memory error management
ERR_SBEReadMask	uint32_t	Single-bit ECC memory error management
ERR_SBEResetMask	uint32_t	Single-bit ECC memory error management
ERR_SBEResetValue	uint32_t	Single-bit ECC memory error management

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Name	Type	Description
ERR_SBEWriteMask	uint32_t	Single-bit ECC memory error management
INIT_ADDR	uint32_t	DDR training initialization address
INIT_ADDRColdResetValue	uint32_t	DDR training initialization address
INIT_ADDRForcedBits	uint32_t	DDR training initialization address
INIT_ADDRForcedFlippedBits	uint32_t	DDR training initialization address
INIT_ADDRReadMask	uint32_t	DDR training initialization address
INIT_ADDRResetMask	uint32_t	DDR training initialization address
INIT_ADDRResetValue	uint32_t	DDR training initialization address
INIT_ADDRWriteMask	uint32_t	DDR training initialization address
INIT_EXT_ADDR	uint32_t	DDR training initialization extended address
INIT_EXT_ADDRColdResetValue	uint32_t	DDR training initialization extended address
INIT_EXT_ADDRForcedBits	uint32_t	DDR training initialization extended address
INIT_EXT_ADDRForcedFlippedBits	uint32_t	DDR training initialization extended address
INIT_EXT_ADDRReadMask	uint32_t	DDR training initialization extended address
INIT_EXT_ADDRResetMask	uint32_t	DDR training initialization extended address
INIT_EXT_ADDRResetValue	uint32_t	DDR training initialization extended address
INIT_EXT_ADDRWriteMask	uint32_t	DDR training initialization extended address
IP_REV1	uint32_t	DDR IP block revision 1
IP_REV1ColdResetValue	uint32_t	DDR IP block revision 1
IP_REV1ForcedBits	uint32_t	DDR IP block revision 1

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Name	Type	Description
IP_REV1ForcedFlippedBits	uint32_t	DDR IP block revision 1
IP_REV1ReadMask	uint32_t	DDR IP block revision 1
IP_REV1ResetMask	uint32_t	DDR IP block revision 1
IP_REV1ResetValue	uint32_t	DDR IP block revision 1
IP_REV1WriteMask	uint32_t	DDR IP block revision 1
IP_REV2	uint32_t	DDR IP block revision 2
IP_REV2ColdResetValue	uint32_t	DDR IP block revision 2
IP_REV2ForcedBits	uint32_t	DDR IP block revision 2
IP_REV2ForcedFlippedBits	uint32_t	DDR IP block revision 2
IP_REV2ReadMask	uint32_t	DDR IP block revision 2
IP_REV2ResetMask	uint32_t	DDR IP block revision 2
IP_REV2ResetValue	uint32_t	DDR IP block revision 2
IP_REV2WriteMask	uint32_t	DDR IP block revision 2
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
SDRAM_CFG	uint32_t	DDR SDRAM control configuration
SDRAM_CFGColdResetValue	uint32_t	DDR SDRAM control configuration
SDRAM_CFGForcedBits	uint32_t	DDR SDRAM control configuration
SDRAM_CFGForcedFlippedBits	uint32_t	DDR SDRAM control configuration
SDRAM_CFGReadMask	uint32_t	DDR SDRAM control configuration
SDRAM_CFGResetMask	uint32_t	DDR SDRAM control configuration

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
SDRAM_CFGResetValue	uint32_t	DDR SDRAM control configuration
SDRAM_CFGWriteMask	uint32_t	DDR SDRAM control configuration
SDRAM_CFG_2	uint32_t	DDR SDRAM control configuration 2
SDRAM_CFG_2ColdResetValue	uint32_t	DDR SDRAM control configuration 2
SDRAM_CFG_2ForcedBits	uint32_t	DDR SDRAM control configuration 2
SDRAM_CFG_2ForcedFlippedBits	uint32_t	DDR SDRAM control configuration 2
SDRAM_CFG_2ReadMask	uint32_t	DDR SDRAM control configuration 2
SDRAM_CFG_2ResetMask	uint32_t	DDR SDRAM control configuration 2
SDRAM_CFG_2ResetValue	uint32_t	DDR SDRAM control configuration 2
SDRAM_CFG_2WriteMask	uint32_t	DDR SDRAM control configuration 2
SDRAM_CLK_CNTL	uint32_t	DDR SDRAM clock control
SDRAM_CLK_CNTLColdResetValue	uint32_t	DDR SDRAM clock control
SDRAM_CLK_CNTLForcedBits	uint32_t	DDR SDRAM clock control
SDRAM_CLK_CNTLForcedFlippedBits	uint32_t	DDR SDRAM clock control
SDRAM_CLK_CNTLReadMask	uint32_t	DDR SDRAM clock control
SDRAM_CLK_CNTLResetMask	uint32_t	DDR SDRAM clock control
SDRAM_CLK_CNTLResetValue	uint32_t	DDR SDRAM clock control
SDRAM_CLK_CNTLWriteMask	uint32_t	DDR SDRAM clock control
SDRAM_INTERVAL	uint32_t	DDR SDRAM interval configuration
SDRAM_INTERVALColdResetValue	uint32_t	DDR SDRAM interval configuration
SDRAM_INTERVALForcedBits	uint32_t	DDR SDRAM interval configuration

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Name	Type	Description
SDRAM_INTERVALForcedFlippedBits	uint32_t	DDR SDRAM interval configuration
SDRAM_INTERVALReadMask	uint32_t	DDR SDRAM interval configuration
SDRAM_INTERVALResetMask	uint32_t	DDR SDRAM interval configuration
SDRAM_INTERVALResetValue	uint32_t	DDR SDRAM interval configuration
SDRAM_INTERVALWriteMask	uint32_t	DDR SDRAM interval configuration
SDRAM_MD_CNTL	uint32_t	DDR SDRAM mode control
SDRAM_MD_CNTLColdResetValue	uint32_t	DDR SDRAM mode control
SDRAM_MD_CNTLForcedBits	uint32_t	DDR SDRAM mode control
SDRAM_MD_CNTLForcedFlippedBits	uint32_t	DDR SDRAM mode control
SDRAM_MD_CNTLReadMask	uint32_t	DDR SDRAM mode control
SDRAM_MD_CNTLResetMask	uint32_t	DDR SDRAM mode control
SDRAM_MD_CNTLResetValue	uint32_t	DDR SDRAM mode control
SDRAM_MD_CNTLWriteMask	uint32_t	DDR SDRAM mode control
SDRAM_MODE	uint32_t	DDR SDRAM mode configuration
SDRAM_MODEColdResetValue	uint32_t	DDR SDRAM mode configuration
SDRAM_MODEForcedBits	uint32_t	DDR SDRAM mode configuration
SDRAM_MODEForcedFlippedBits	uint32_t	DDR SDRAM mode configuration
SDRAM_MODEReadMask	uint32_t	DDR SDRAM mode configuration
SDRAM_MODEResetMask	uint32_t	DDR SDRAM mode configuration
SDRAM_MODEResetValue	uint32_t	DDR SDRAM mode configuration
SDRAM_MODEWriteMask	uint32_t	DDR SDRAM mode configuration

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Name	Type	Description
SDRAM_MODE_2	uint32_t	DDR SDRAM mode configuration 2
SDRAM_MODE_2ColdResetValue	uint32_t	DDR SDRAM mode configuration 2
SDRAM_MODE_2ForcedBits	uint32_t	DDR SDRAM mode configuration 2
SDRAM_MODE_2ForcedFlippedBits	uint32_t	DDR SDRAM mode configuration 2
SDRAM_MODE_2ReadMask	uint32_t	DDR SDRAM mode configuration 2
SDRAM_MODE_2ResetMask	uint32_t	DDR SDRAM mode configuration 2
SDRAM_MODE_2ResetValue	uint32_t	DDR SDRAM mode configuration 2
SDRAM_MODE_2WriteMask	uint32_t	DDR SDRAM mode configuration 2
SDRAM_RCW_1	uint32_t	DDR register control words 1
SDRAM_RCW_1ColdResetValue	uint32_t	DDR register control words 1
SDRAM_RCW_1ForcedBits	uint32_t	DDR register control words 1
SDRAM_RCW_1ForcedFlippedBits	uint32_t	DDR register control words 1
SDRAM_RCW_1ReadMask	uint32_t	DDR register control words 1
SDRAM_RCW_1ResetMask	uint32_t	DDR register control words 1
SDRAM_RCW_1ResetValue	uint32_t	DDR register control words 1
SDRAM_RCW_1WriteMask	uint32_t	DDR register control words 1
SDRAM_RCW_2	uint32_t	DDR register control words 2
SDRAM_RCW_2ColdResetValue	uint32_t	DDR register control words 2
SDRAM_RCW_2ForcedBits	uint32_t	DDR register control words 2
SDRAM_RCW_2ForcedFlippedBits	uint32_t	DDR register control words 2
SDRAM_RCW_2ReadMask	uint32_t	DDR register control words 2
SDRAM_RCW_2ResetMask	uint32_t	DDR register control words 2
SDRAM_RCW_2ResetValue	uint32_t	DDR register control words 2
SDRAM_RCW_2WriteMask	uint32_t	DDR register control words 2
SR_CNTR	uint32_t	DDR self refresh counter

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Name	Type	Description
SR_CNTRColdResetValue	uint32_t	DDR self refresh counter
SR_CNTRForcedBits	uint32_t	DDR self refresh counter
SR_CNTRForcedFlippedBits	uint32_t	DDR self refresh counter
SR_CNTRReadMask	uint32_t	DDR self refresh counter
SR_CNTRResetMask	uint32_t	DDR self refresh counter
SR_CNTRResetValue	uint32_t	DDR self refresh counter
SR_CNTRWriteMask	uint32_t	DDR self refresh counter
TIMING_CFG_0	uint32_t	DDR SDRAM timing configuration 0
TIMING_CFG_0ColdResetValue	uint32_t	DDR SDRAM timing configuration 0
TIMING_CFG_0ForcedBits	uint32_t	DDR SDRAM timing configuration 0
TIMING_CFG_0ForcedFlippedBits	uint32_t	DDR SDRAM timing configuration 0
TIMING_CFG_0ReadMask	uint32_t	DDR SDRAM timing configuration 0
TIMING_CFG_0ResetMask	uint32_t	DDR SDRAM timing configuration 0
TIMING_CFG_0ResetValue	uint32_t	DDR SDRAM timing configuration 0
TIMING_CFG_0WriteMask	uint32_t	DDR SDRAM timing configuration 0
TIMING_CFG_1	uint32_t	DDR SDRAM timing configuration 1
TIMING_CFG_1ColdResetValue	uint32_t	DDR SDRAM timing configuration 1
TIMING_CFG_1ForcedBits	uint32_t	DDR SDRAM timing configuration 1
TIMING_CFG_1ForcedFlippedBits	uint32_t	DDR SDRAM timing configuration 1
TIMING_CFG_1ReadMask	uint32_t	DDR SDRAM timing configuration 1
TIMING_CFG_1ResetMask	uint32_t	DDR SDRAM timing configuration 1

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Name	Type	Description
TIMING_CFG_1ResetValue	uint32_t	DDR SDRAM timing configuration 1
TIMING_CFG_1WriteMask	uint32_t	DDR SDRAM timing configuration 1
TIMING_CFG_2	uint32_t	DDR SDRAM timing configuration 2
TIMING_CFG_2ColdResetValue	uint32_t	DDR SDRAM timing configuration 2
TIMING_CFG_2ForcedBits	uint32_t	DDR SDRAM timing configuration 2
TIMING_CFG_2ForcedFlippedBits	uint32_t	DDR SDRAM timing configuration 2
TIMING_CFG_2ReadMask	uint32_t	DDR SDRAM timing configuration 2
TIMING_CFG_2ResetMask	uint32_t	DDR SDRAM timing configuration 2
TIMING_CFG_2ResetValue	uint32_t	DDR SDRAM timing configuration 2
TIMING_CFG_2WriteMask	uint32_t	DDR SDRAM timing configuration 2
TIMING_CFG_3	uint32_t	DDR SDRAM timing configuration 3
TIMING_CFG_3ColdResetValue	uint32_t	DDR SDRAM timing configuration 3
TIMING_CFG_3ForcedBits	uint32_t	DDR SDRAM timing configuration 3
TIMING_CFG_3ForcedFlippedBits	uint32_t	DDR SDRAM timing configuration 3
TIMING_CFG_3ReadMask	uint32_t	DDR SDRAM timing configuration 3
TIMING_CFG_3ResetMask	uint32_t	DDR SDRAM timing configuration 3
TIMING_CFG_3ResetValue	uint32_t	DDR SDRAM timing configuration 3
TIMING_CFG_3WriteMask	uint32_t	DDR SDRAM timing configuration 3

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Name	Type	Description
TIMING_CFG_4	uint32_t	DDR SDRAM timing configuration 4
TIMING_CFG_4ColdResetValue	uint32_t	DDR SDRAM timing configuration 4
TIMING_CFG_4ForcedBits	uint32_t	DDR SDRAM timing configuration 4
TIMING_CFG_4ForcedFlippedBits	uint32_t	DDR SDRAM timing configuration 4
TIMING_CFG_4ReadMask	uint32_t	DDR SDRAM timing configuration 4
TIMING_CFG_4ResetMask	uint32_t	DDR SDRAM timing configuration 4
TIMING_CFG_4ResetValue	uint32_t	DDR SDRAM timing configuration 4
TIMING_CFG_4WriteMask	uint32_t	DDR SDRAM timing configuration 4
TIMING_CFG_5	uint32_t	DDR SDRAM timing configuration 5
TIMING_CFG_5ColdResetValue	uint32_t	DDR SDRAM timing configuration 5
TIMING_CFG_5ForcedBits	uint32_t	DDR SDRAM timing configuration 5
TIMING_CFG_5ForcedFlippedBits	uint32_t	DDR SDRAM timing configuration 5
TIMING_CFG_5ReadMask	uint32_t	DDR SDRAM timing configuration 5
TIMING_CFG_5ResetMask	uint32_t	DDR SDRAM timing configuration 5
TIMING_CFG_5ResetValue	uint32_t	DDR SDRAM timing configuration 5
TIMING_CFG_5WriteMask	uint32_t	DDR SDRAM timing configuration 5
TimeSource	*void	Time source object
WRLVL_CNTL	uint32_t	DDR write leveling control
WRLVL_CNTLColdResetValue	uint32_t	DDR write leveling control
WRLVL_CNTLForcedBits	uint32_t	DDR write leveling control

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
WRLVL_CNTLForcedFlippedBits	uint32_t	DDR write leveling control
WRLVL_CNTLReadMask	uint32_t	DDR write leveling control
WRLVL_CNTLResetMask	uint32_t	DDR write leveling control
WRLVL_CNTLResetValue	uint32_t	DDR write leveling control
WRLVL_CNTLWriteMask	uint32_t	DDR write leveling control
WRLVL_CNTL_2	uint32_t	DDR write leveling control 2
WRLVL_CNTL_2ColdResetValue	uint32_t	DDR write leveling control 2
WRLVL_CNTL_2ForcedBits	uint32_t	DDR write leveling control 2
WRLVL_CNTL_2ForcedFlippedBits	uint32_t	DDR write leveling control 2
WRLVL_CNTL_2ReadMask	uint32_t	DDR write leveling control 2
WRLVL_CNTL_2ResetMask	uint32_t	DDR write leveling control 2
WRLVL_CNTL_2ResetValue	uint32_t	DDR write leveling control 2
WRLVL_CNTL_2WriteMask	uint32_t	DDR write leveling control 2
WRLVL_CNTL_3	uint32_t	DDR write leveling control 3
WRLVL_CNTL_3ColdResetValue	uint32_t	DDR write leveling control 3
WRLVL_CNTL_3ForcedBits	uint32_t	DDR write leveling control 3
WRLVL_CNTL_3ForcedFlippedBits	uint32_t	DDR write leveling control 3
WRLVL_CNTL_3ReadMask	uint32_t	DDR write leveling control 3
WRLVL_CNTL_3ResetMask	uint32_t	DDR write leveling control 3
WRLVL_CNTL_3ResetValue	uint32_t	DDR write leveling control 3
WRLVL_CNTL_3WriteMask	uint32_t	DDR write leveling control 3
ZQ_CNTL	uint32_t	DDR ZQ calibration control
ZQ_CNTLColdResetValue	uint32_t	DDR ZQ calibration control
ZQ_CNTLForcedBits	uint32_t	DDR ZQ calibration control
ZQ_CNTLForcedFlippedBits	uint32_t	DDR ZQ calibration control
ZQ_CNTLReadMask	uint32_t	DDR ZQ calibration control
ZQ_CNTLResetMask	uint32_t	DDR ZQ calibration control
ZQ_CNTLResetValue	uint32_t	DDR ZQ calibration control
ZQ_CNTLWriteMask	uint32_t	DDR ZQ calibration control
config.IRQ	uint8_t	

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Name	Type	Description
irqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller
memorySpace	temu_IfaceRef/ <unknown>	Memory space.

Interfaces

Name	Type	Description
CorrectableErrorIface	MemAccessIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	
UncorrectableErrorIface	MemAccessIface	

Commands

Name	Description
delete	Dispose instance of DDR

10.2.5. Limitations

Only registers handling SEU and MEU events are implemented, other parts of the model are dummy non-functional registers.

10.3. DMA

This section describes the P2020 DMA model.

The DMA controller transfers blocks of data between the interface and functional modules of this chip, independent of the cores or external hosts. It has four high-speed DMA channels. Both the cores and external devices can initiate DMA transfers.

The DMA module has two modes of operation: basic and extended. Basic mode is the DMA legacy mode, which does not support advanced features. Extended mode supports advanced features such as striding and flexible descriptor structures. These two basic modes allow users to initiate and end DMA transfers in various ways:

- Direct mode: no descriptors are involved, software/user must initialize such required fields as source address and attributes and destination address and attributes.
- Chaining mode: software must initialize descriptors in memory and such fields as link/list descriptor address before starting a transfer.

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- Single-write start mode: DMA process can be started using a single-write command to either the descriptor address register in one of the chaining modes or the source/destination address registers in one of the direct modes.

10.3.1. Loading the Plugin

```
import P2020
```

10.3.2. Configuration

The DMA programmable registers that occupy memory-mapped space are named according to P2020 QorIQ integrated processor reference manual. All 4 DMA channels have the same set of registers, so the register index is the channels id (from 0 to 3).

Listing 28. Setting registers via Command Line

```
# set source address for channel 3
dma.SAR[3] = 0x40000000
```

Listing 29. Setting registers via API

```
// set source address for channel 3
temu_writeValueU32(dma, "SAR", 0x40000000, 3);
```

10.3.3. @DMA Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @DMA
new	Create new instance of DMA

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

10.3.4. DMA Reference

Properties

Name	Type	Description
BCR	[uint32_t; 4]	DMA byte count register
CLNDAR	[uint32_t; 4]	DMA current link descriptor address register
CLSDAR	[uint32_t; 4]	DMA current list descriptor address register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
DAR	[uint32_t; 4]	DMA destination address register
DATR	[uint32_t; 4]	DMA destination attributes register
DGSR	uint32_t	DMA general status register
DGSRColdResetValue	uint32_t	DMA general status register
DGSRForcedBits	uint32_t	DMA general status register
DGSRForcedFlippedBits	uint32_t	DMA general status register
DGSRReadMask	uint32_t	DMA general status register
DGSRResetMask	uint32_t	DMA general status register
DGSRResetValue	uint32_t	DMA general status register

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Name	Type	Description
DGSRWriteMask	uint32_t	DMA general status register
DSR	[uint32_t; 4]	DMA destination stride register
ECLNDAR	[uint32_t; 4]	DMA current link descriptor extended address register
ECLSDAR	[uint32_t; 4]	DMA extended current list descriptor address register
ENLNDAR	[uint32_t; 4]	DMA extended next link descriptor address register
ENLSDAR	[uint32_t; 4]	DMA extended next list descriptor address register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
MR	[uint32_t; 4]	DMA channel mode register
NLNDAR	[uint32_t; 4]	DMA next link descriptor address register
NLSDAR	[uint32_t; 4]	DMA next list descriptor address register
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
SAR	[uint32_t; 4]	DMA source address register
SATR	[uint32_t; 4]	DMA source attributes register
SR	[uint32_t; 4]	DMA channel status register
SSR	[uint32_t; 4]	DMA source stride register
TimeSource	*void	Time source object
config.interrupt	[uint8_t; 4]	DMA IRQ number for each channel
irqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller
memAccess	temu_IfaceRef/ <unknown>	Memory access for DMA.

Interfaces

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DeviceIface	DeviceIface	Device Interface
MemAccessIface	MemAccessIface	Memory access interface.
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	Reset Interface

Commands

Name	Description
delete	Dispose instance of DMA

10.3.5. Limitations

None

10.4. DUART

This section describes the P2020 serial port (DUART) model. The DUART model supports both FIFO simualtion and infinite speed UARTs. In infinite speed mode bytes are sent directly when they are written to the data register. FIFO mode for both transmitter and receiver provides 16-byte FIFOs.

10.4.1. Loading the Plugin

```
import P2020
```

10.4.2. Configuration

config.infiniteUartSpeed
: Enable/disable immediate UART.

config.fifoSize
: maximum UART FIFO size.

config.clockDivider
: Clock devider (default 1).

To receive transmitted data from DUART device can be connected via the serial interface it implements:

Listing 30. Connecting via Command Line

```
# Connect DUART transmitter to device model
```

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

```
connect a=duart.tx b=mydevice:SerialIface
```

Listing 31. Connecting via API

```
// Connect DUART transmitter to device model
temu_connect(duart, "tx", mydevice, "SerialIface");
```

The DUART programmable registers that occupy memory-mapped space are named according to P2020 QorIQ integrated processor reference manual. All the DUART registers are one-byte wide.

To enables the transmitter and receiver FIFOs you need to set FIFO Control Register value as follows:

Listing 32. Setting registers via Command Line

```
duart.UFCR = 0x01;
```

Listing 33. Setting registers via API

```
temu_writeValueU8(duart, "UFCR", 0x01, 0);
```

10.4.3. @DUART Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Description
delete	Dispose instance of @DUART
new	Create new instance of DUART

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

10.4.4. DUART Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
UAFR	uint8_t	Alternate function register
UAFRColdResetValue	uint8_t	Alternate function register
UAFRForcedBits	uint8_t	Alternate function register
UAFRForcedFlippedBits	uint8_t	Alternate function register
UAFRReadMask	uint8_t	Alternate function register
UAFRResetMask	uint8_t	Alternate function register
UAFRResetValue	uint8_t	Alternate function register
UAFRWriteMask	uint8_t	Alternate function register
UDLB	uint8_t	Divisor least significant byte register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
UDLBColdResetValue	uint8_t	Divisor least significant byte register
UDLBForcedBits	uint8_t	Divisor least significant byte register
UDLBForcedFlippedBits	uint8_t	Divisor least significant byte register
UDLBReadMask	uint8_t	Divisor least significant byte register
UDLBResetMask	uint8_t	Divisor least significant byte register
UDLBResetValue	uint8_t	Divisor least significant byte register
UDLBWriteMask	uint8_t	Divisor least significant byte register
UDMB	uint8_t	Divisor most significant byte register
UDMBColdResetValue	uint8_t	Divisor most significant byte register
UDMBForcedBits	uint8_t	Divisor most significant byte register
UDMBForcedFlippedBits	uint8_t	Divisor most significant byte register
UDMBReadMask	uint8_t	Divisor most significant byte register
UDMBResetMask	uint8_t	Divisor most significant byte register
UDMBResetValue	uint8_t	Divisor most significant byte register
UDMBWriteMask	uint8_t	Divisor most significant byte register
UDSR	uint8_t	DMA status register
UDSRColdResetValue	uint8_t	DMA status register
UDSRForcedBits	uint8_t	DMA status register
UDSRForcedFlippedBits	uint8_t	DMA status register
UDSRReadMask	uint8_t	DMA status register
UDSRResetMask	uint8_t	DMA status register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
UDSRResetValue	uint8_t	DMA status register
UDSRWriteMask	uint8_t	DMA status register
UFCR	uint8_t	FIFO control register
UFCRColdResetValue	uint8_t	FIFO control register
UFCRForcedBits	uint8_t	FIFO control register
UFCRForcedFlippedBits	uint8_t	FIFO control register
UFCRReadMask	uint8_t	FIFO control register
UFCRResetMask	uint8_t	FIFO control register
UFCRResetValue	uint8_t	FIFO control register
UFCRWriteMask	uint8_t	FIFO control register
UIER	uint8_t	Interrupt enable register
UIERColdResetValue	uint8_t	Interrupt enable register
UIERForcedBits	uint8_t	Interrupt enable register
UIERForcedFlippedBits	uint8_t	Interrupt enable register
UIERReadMask	uint8_t	Interrupt enable register
UIERResetMask	uint8_t	Interrupt enable register
UIERResetValue	uint8_t	Interrupt enable register
UIERWriteMask	uint8_t	Interrupt enable register
UIIR	uint8_t	Interrupt ID register
UIIRColdResetValue	uint8_t	Interrupt ID register
UIIRForcedBits	uint8_t	Interrupt ID register
UIIRForcedFlippedBits	uint8_t	Interrupt ID register
UIIRReadMask	uint8_t	Interrupt ID register
UIIRResetMask	uint8_t	Interrupt ID register
UIIRResetValue	uint8_t	Interrupt ID register
UIIRWriteMask	uint8_t	Interrupt ID register
ULCR	uint8_t	Line control register
ULCRColdResetValue	uint8_t	Line control register
ULCRForcedBits	uint8_t	Line control register
ULCRForcedFlippedBits	uint8_t	Line control register
ULCRReadMask	uint8_t	Line control register
ULCRResetMask	uint8_t	Line control register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ULCRResetValue	uint8_t	Line control register
ULCRWriteMask	uint8_t	Line control register
ULSR	uint8_t	Line status register
ULSRColdResetValue	uint8_t	Line status register
ULSRForcedBits	uint8_t	Line status register
ULSRForcedFlippedBits	uint8_t	Line status register
ULSRReadMask	uint8_t	Line status register
ULSRResetMask	uint8_t	Line status register
ULSRResetValue	uint8_t	Line status register
ULSRWriteMask	uint8_t	Line status register
UMCR	uint8_t	Modem control register
UMCRColdResetValue	uint8_t	Modem control register
UMCRForcedBits	uint8_t	Modem control register
UMCRForcedFlippedBits	uint8_t	Modem control register
UMCRReadMask	uint8_t	Modem control register
UMCRResetMask	uint8_t	Modem control register
UMCRResetValue	uint8_t	Modem control register
UMCRWriteMask	uint8_t	Modem control register
UMSR	uint8_t	Modem status register
UMSRColdResetValue	uint8_t	Modem status register
UMSRForcedBits	uint8_t	Modem status register
UMSRForcedFlippedBits	uint8_t	Modem status register
UMSRReadMask	uint8_t	Modem status register
UMSRResetMask	uint8_t	Modem status register
UMSRResetValue	uint8_t	Modem status register
UMSRWriteMask	uint8_t	Modem status register
URBR	uint8_t	Receiver buffer register
URBRColdResetValue	uint8_t	Receiver buffer register
URBRForcedBits	uint8_t	Receiver buffer register
URBRForcedFlippedBits	uint8_t	Receiver buffer register
URBRReadMask	uint8_t	Receiver buffer register
URBRResetMask	uint8_t	Receiver buffer register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
URBRResetValue	uint8_t	Receiver buffer register
URBRWriteMask	uint8_t	Receiver buffer register
USCR	uint8_t	Scratch register
USCRColdResetValue	uint8_t	Scratch register
USCRForcedBits	uint8_t	Scratch register
USCRForcedFlippedBits	uint8_t	Scratch register
USCRReadMask	uint8_t	Scratch register
USCRResetMask	uint8_t	Scratch register
USCRResetValue	uint8_t	Scratch register
USCRWriteMask	uint8_t	Scratch register
UTHR	uint8_t	Transmitter holding register
UTHRColdResetValue	uint8_t	Transmitter holding register
UTHRForcedBits	uint8_t	Transmitter holding register
UTHRForcedFlippedBits	uint8_t	Transmitter holding register
UTHRReadMask	uint8_t	Transmitter holding register
UTHRResetMask	uint8_t	Transmitter holding register
UTHRResetValue	uint8_t	Transmitter holding register
UTHRWriteMask	uint8_t	Transmitter holding register
config.clockDivider	uint32_t	Clock divider
config.fifoSize	uint8_t	UART FIFO size
config.infiniteUartSpeed	uint8_t	Set to 1 to enable immediate UARTs
config.interrupt	uint8_t	Interrupt number
dataArrivedSinceLastRead	uint8_t	Set to 1 if data has arrived on the serial port since the last read.
irqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller
rxFifo.data	[uint8_t; 32]	RX FIFO data
rxFifo.size	uint8_t	RX size
rxFifo.start	uint8_t	RX start index
rxFifo.usage	uint8_t	RX usage
rxTriggerLevel	uint8_t	Internal state (rx trigger level).
tx	temu_IfaceRef/ <unknown>	Transmit target

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
txFifo.data	[uint8_t; 32]	TX FIFO data
txFifo.size	uint8_t	TX size
txFifo.start	uint8_t	TX start index
txFifo.usage	uint8_t	TX usage
txShift	uint8_t	UART shift register

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	Device interface.
MemAccessIface	MemAccessIface	Memory access interface.
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	Reset interface.
UartIface	SerialIface	Serial input interface.

Ports

Prop	Iface	Description
tx	UartIface	serial port

Commands

Name	Description
delete	Dispose instance of DUART

10.4.5. Limitations

- Control flow (cts and rts) is not supported.
- Loop back mode is not supported.

10.5. ECM

This section describes the P2020 ECM model. The model is a dummy providing only non-functional registers.

10.5.1. Loading the Plugin

```
import P2020
```

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

10.5.2. Configuration

10.5.3. @ECM Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @ECM
new	Create new instance of ECM

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

10.5.4. ECM Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
EEATR	uint32_t	ECM error attributes capture register
EEATRColdResetValue	uint32_t	ECM error attributes capture register
EEATRForcedBits	uint32_t	ECM error attributes capture register
EEATRForcedFlippedBits	uint32_t	ECM error attributes capture register
EEATRReadMask	uint32_t	ECM error attributes capture register
EEATRResetMask	uint32_t	ECM error attributes capture register
EEATRResetValue	uint32_t	ECM error attributes capture register
EEATRWriteMask	uint32_t	ECM error attributes capture register
EEBACR	uint32_t	ECM CCB address configuration register
EEBACRColdResetValue	uint32_t	ECM CCB address configuration register
EEBACRForcedBits	uint32_t	ECM CCB address configuration register
EEBACRForcedFlippedBits	uint32_t	ECM CCB address configuration register
EEBACRReadMask	uint32_t	ECM CCB address configuration register
EEBACRResetMask	uint32_t	ECM CCB address configuration register
EEBACRResetValue	uint32_t	ECM CCB address configuration register
EEBACRWriteMask	uint32_t	ECM CCB address configuration register
EEBPCR	uint32_t	ECM CCB port configuration register
EEBPCRColdResetValue	uint32_t	ECM CCB port configuration register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
EEBPCRForcedBits	uint32_t	ECM CCB port configuration register
EEBPCRForcedFlippedBits	uint32_t	ECM CCB port configuration register
EEBPCRReadMask	uint32_t	ECM CCB port configuration register
EEBPCRResetMask	uint32_t	ECM CCB port configuration register
EEBPCRResetValue	uint32_t	ECM CCB port configuration register
EEBPCRWriteMask	uint32_t	ECM CCB port configuration register
EEDR	uint32_t	ECM error detect register
EEDRColdResetValue	uint32_t	ECM error detect register
EEDRForcedBits	uint32_t	ECM error detect register
EEDRForcedFlippedBits	uint32_t	ECM error detect register
EEDRReadMask	uint32_t	ECM error detect register
EEDRResetMask	uint32_t	ECM error detect register
EEDRResetValue	uint32_t	ECM error detect register
EEDRWriteMask	uint32_t	ECM error detect register
EEER	uint32_t	ECM error enable register
EEERColdResetValue	uint32_t	ECM error enable register
EEERForcedBits	uint32_t	ECM error enable register
EEERForcedFlippedBits	uint32_t	ECM error enable register
EEERReadMask	uint32_t	ECM error enable register
EEERResetMask	uint32_t	ECM error enable register
EEERResetValue	uint32_t	ECM error enable register
EEERWriteMask	uint32_t	ECM error enable register
EEHADR	uint32_t	ECM error high address capture register
EEHADRColdResetValue	uint32_t	ECM error high address capture register
EEHADRForcedBits	uint32_t	ECM error high address capture register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
EEHADRForcedFlippedBits	uint32_t	ECM error high address capture register
EEHADRReadMask	uint32_t	ECM error high address capture register
EEHADRResetMask	uint32_t	ECM error high address capture register
EEHADRResetValue	uint32_t	ECM error high address capture register
EEHADRWriteMask	uint32_t	ECM error high address capture register
EELADR	uint32_t	ECM error low address capture register
EELADRColdResetValue	uint32_t	ECM error low address capture register
EELADRForcedBits	uint32_t	ECM error low address capture register
EELADRForcedFlippedBits	uint32_t	ECM error low address capture register
EELADRReadMask	uint32_t	ECM error low address capture register
EELADRResetMask	uint32_t	ECM error low address capture register
EELADRResetValue	uint32_t	ECM error low address capture register
EELADRWriteMask	uint32_t	ECM error low address capture register
EIPBRR1	uint32_t	ECM IP block revision register 1
EIPBRR1ColdResetValue	uint32_t	ECM IP block revision register 1
EIPBRR1ForcedBits	uint32_t	ECM IP block revision register 1
EIPBRR1ForcedFlippedBits	uint32_t	ECM IP block revision register 1
EIPBRR1ReadMask	uint32_t	ECM IP block revision register 1
EIPBRR1ResetMask	uint32_t	ECM IP block revision register 1
EIPBRR1ResetValue	uint32_t	ECM IP block revision register 1
EIPBRR1WriteMask	uint32_t	ECM IP block revision register 1
EIPBRR2	uint32_t	ECM IP block revision register 2
EIPBRR2ColdResetValue	uint32_t	ECM IP block revision register 2

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
EIPBRR2ForcedBits	uint32_t	ECM IP block revision register 2
EIPBRR2ForcedFlippedBits	uint32_t	ECM IP block revision register 2
EIPBRR2ReadMask	uint32_t	ECM IP block revision register 2
EIPBRR2ResetMask	uint32_t	ECM IP block revision register 2
EIPBRR2ResetValue	uint32_t	ECM IP block revision register 2
EIPBRR2WriteMask	uint32_t	ECM IP block revision register 2
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Commands

Name	Description
delete	Dispose instance of ECM

10.5.5. Limitations

The model is a dummy providing only non-functional registers.

10.6. eSPI

This section describes the P2020 Enhanced Serial Peripheral Interface (eSPI) model.

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

The eSPI is a full-duplex, synchronous, character-oriented channel that supports a simple interface (receive, transmit and chip selects).



eSPI model contains names which include master/slave terminology. The TEMU project does not use such terms normally, however given that the hardware specification, this header deals with, use these terms they are reused here for consistency.

10.6.1. Loading the Plugin

```
import P2020
```

10.6.2. Configuration

Master device does not have a direct access to slave devices(and vice versa). Transmission and reception process is done through bus, the bus route on chip select signals.

The eSPI bus model can be configured by connecting it to a temu_SpiBus2 bus model.

Listing 34. Connecting via Command Line

```
# Connect bus to the eSPI model
connect a=espi.spiBus b=spiBus:SpiBus2Iface
```

Listing 35. Connecting via API

```
// Connect SPI bus SpiBus2Iface to eSPI
temu_connect(espi, "spiBus", spiBus, "SpiBus2Iface")
```

The eSPI programmable registers that occupy memory-mapped space are named according to P2020 QorIQ integrated processor reference manual. All the registers are 4-byte wide:

Listing 36. Setting registers via Command Line

```
# Configure SPMODE register to enable normal operation
espi.SPMODE = 0x8000100F;
```

Listing 37. Setting registers via API

```
// Configure SPMODE register to enable normal operation
temu_writeValueU32(espi, "SPMODE", 0x8000100F, 0);
```

10.6.3. @eSPI Reference

Properties

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @eSPI
new	Create new instance of eSPI

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

10.6.4. eSPI Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
SPCOM	uint32_t	eSPI command register
SPCOMColdResetValue	uint32_t	eSPI command register
SPCOMForcedBits	uint32_t	eSPI command register
SPCOMForcedFlippedBits	uint32_t	eSPI command register
SPCOMReadMask	uint32_t	eSPI command register
SPCOMResetMask	uint32_t	eSPI command register
SPCOMResetValue	uint32_t	eSPI command register
SPCOMWriteMask	uint32_t	eSPI command register
SPIE	uint32_t	eSPI event register
SPIEColdResetValue	uint32_t	eSPI event register
SPIEForcedBits	uint32_t	eSPI event register
SPIEForcedFlippedBits	uint32_t	eSPI event register
SPIEReadMask	uint32_t	eSPI event register
SPIEResetMask	uint32_t	eSPI event register
SPIEResetValue	uint32_t	eSPI event register
SPIEWriteMask	uint32_t	eSPI event register
SPIM	uint32_t	eSPI mask register
SPIMColdResetValue	uint32_t	eSPI mask register
SPIMForcedBits	uint32_t	eSPI mask register
SPIMForcedFlippedBits	uint32_t	eSPI mask register
SPIMReadMask	uint32_t	eSPI mask register
SPIMResetMask	uint32_t	eSPI mask register
SPIMResetValue	uint32_t	eSPI mask register
SPIMWriteMask	uint32_t	eSPI mask register
SPIRF	uint32_t	eSPI receive FIFO access register
SPIRFColdResetValue	uint32_t	eSPI receive FIFO access register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
SPIRFForcedBits	uint32_t	eSPI receive FIFO access register
SPIRFForcedFlippedBits	uint32_t	eSPI receive FIFO access register
SPIRFReadMask	uint32_t	eSPI receive FIFO access register
SPIRFResetMask	uint32_t	eSPI receive FIFO access register
SPIRFResetValue	uint32_t	eSPI receive FIFO access register
SPIRFWriteMask	uint32_t	eSPI receive FIFO access register
SPITF	uint32_t	eSPI transmit FIFO access register
SPITFColdResetValue	uint32_t	eSPI transmit FIFO access register
SPITFForcedBits	uint32_t	eSPI transmit FIFO access register
SPITFForcedFlippedBits	uint32_t	eSPI transmit FIFO access register
SPITFReadMask	uint32_t	eSPI transmit FIFO access register
SPITFResetMask	uint32_t	eSPI transmit FIFO access register
SPITFResetValue	uint32_t	eSPI transmit FIFO access register
SPITFWriteMask	uint32_t	eSPI transmit FIFO access register
SPMODE	uint32_t	eSPI mode register
SPMODE0	uint32_t	eSPI CS0 mode register
SPMODE0ColdResetValue	uint32_t	eSPI CS0 mode register
SPMODE0ForcedBits	uint32_t	eSPI CS0 mode register
SPMODE0ForcedFlippedBits	uint32_t	eSPI CS0 mode register
SPMODE0ReadMask	uint32_t	eSPI CS0 mode register
SPMODE0ResetMask	uint32_t	eSPI CS0 mode register
SPMODE0ResetValue	uint32_t	eSPI CS0 mode register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
SPMODE0WriteMask	uint32_t	eSPI CS0 mode register
SPMODE1	uint32_t	eSPI CS1 mode register
SPMODE1ColdResetValue	uint32_t	eSPI CS1 mode register
SPMODE1ForcedBits	uint32_t	eSPI CS1 mode register
SPMODE1ForcedFlippedBits	uint32_t	eSPI CS1 mode register
SPMODE1ReadMask	uint32_t	eSPI CS1 mode register
SPMODE1ResetMask	uint32_t	eSPI CS1 mode register
SPMODE1ResetValue	uint32_t	eSPI CS1 mode register
SPMODE1WriteMask	uint32_t	eSPI CS1 mode register
SPMODE2	uint32_t	eSPI CS2 mode register
SPMODE2ColdResetValue	uint32_t	eSPI CS2 mode register
SPMODE2ForcedBits	uint32_t	eSPI CS2 mode register
SPMODE2ForcedFlippedBits	uint32_t	eSPI CS2 mode register
SPMODE2ReadMask	uint32_t	eSPI CS2 mode register
SPMODE2ResetMask	uint32_t	eSPI CS2 mode register
SPMODE2ResetValue	uint32_t	eSPI CS2 mode register
SPMODE2WriteMask	uint32_t	eSPI CS2 mode register
SPMODE3	uint32_t	eSPI CS3 mode register
SPMODE3ColdResetValue	uint32_t	eSPI CS3 mode register
SPMODE3ForcedBits	uint32_t	eSPI CS3 mode register
SPMODE3ForcedFlippedBits	uint32_t	eSPI CS3 mode register
SPMODE3ReadMask	uint32_t	eSPI CS3 mode register
SPMODE3ResetMask	uint32_t	eSPI CS3 mode register
SPMODE3ResetValue	uint32_t	eSPI CS3 mode register
SPMODE3WriteMask	uint32_t	eSPI CS3 mode register
SPMODEColdResetValue	uint32_t	eSPI mode register
SPMODEForcedBits	uint32_t	eSPI mode register
SPMODEForcedFlippedBits	uint32_t	eSPI mode register
SPMODEReadMask	uint32_t	eSPI mode register
SPMODEResetMask	uint32_t	eSPI mode register
SPMODEResetValue	uint32_t	eSPI mode register
SPMODEWriteMask	uint32_t	eSPI mode register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
TimeSource	*void	Time source object
charsSent	uint32_t	
chipType	uint8_t	Chip type
config.interrupt	uint8_t	eSPI IRQ number
irqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller
isActive	uint8_t	
isDone	uint8_t	
rxFifo.data	[uint8_t; 32]	RX FIFO data
rxFifo.size	uint8_t	RX size
rxFifo.start	uint8_t	RX start index
rxFifo.usage	uint8_t	RX usage
spiBus	temu_IfaceRef/ <unknown>	Spi bus
state.isActive	uint8_t	SPI transaction in progress
txFifo.data	[uint8_t; 32]	TX FIFO data
txFifo.size	uint8_t	TX size
txFifo.start	uint8_t	TX start index
txFifo.usage	uint8_t	TX usage

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	Device Interface
MemAccessIface	MemAccessIface	Memory access interface.
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	Reset Interface

Commands

Name	Description
delete	Dispose instance of eSPI

10.6.5. Limitations

- eSPI doesn’t generate the transfer clock SPI_CLK signal and doesn’t implement the eSPI baud rate generator (BRG).

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10.7. eTSEC

This section describes the P2020 eTSEC Ethernet controller model.

The eTSECs of the device include these distinctive features:

- TCP/IP off-load:
  - IP v4 and IP v6 header recognition on receive;
  - IP v4 header checksum verification and generation;
  - TCP and UDP checksum verification and generation;
  - Per-packet configurable off-load.
- Support for different Ethernet physical interfaces (MII, GMII, RMII, RGMII, TBI and RTBI.).

10.7.1. Loading the Plugin

```
import P2020
```

10.7.2. Configuration

config.interfaceMode

Interface Mode (MII 10/100 Mbps, RMII 100 Mbps, RMII 10 Mbps, GMII 1Gbps, etc).

The GenericPHY is a PHY / MII device which supports both the MDIO interface and the PHY interface for sending/receiving ethernet frames. It is connected to MDIO bus via MDIOIface and to eTSEC via PHYIface. An ethernet link must be connected to its attached PHYs via EthernetIface;

The MDIO bus distributes MDIO control messages and supports routing of them. The MDIO bus use the same interface as an MDIO device. It is connected to eTSEC via MDIOIface.

Before starting the communications all mentioned above models should be created and connected as follows:

Listing 38. Setting Ethernet controller via API

```
// connect MDIO bus with MAC controller and PHY circuit.
temu_connect(miibus, "macDevice", etsec, "MACIface");
temu_connect(miibus, "phyDevices", phy, "MDIOIface");
// connect eTSEC with MDIO bus and PHY
temu_connect(etsec, "mdioBus", miibus, "MDIOIface");
temu_connect(etsec, "phy", phy, "PHYIface");

// connect MAC device to PHY
temu_connect(phy, "macDevice", etsec, "MACIface");
// connect ethernet link
```

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```
temu_connect(phy, "ethernetLink", ethlink, "EthernetIface");
```

Listing 39. Setting Ethernet controller via Command Line

```
# connect MDIO bus with MAC controller and PHY circuit.
connect a=miibus.macDevice b=etsec:MACIface
connect a=miibus.phyDevices b=phy:MDIOIface

# connect eTSEC with MDIO bus and PHY
connect a=etsec.mdioBus b=miibus:MDIOIface
connect a=etsec.phy b=phy:PHYIface

#  connect MAC device to PHY
connect a=phy.macDevice b=etsec:MACIface
# connect ethernet link
connect a=phy.ethernetLink b=ethlink:EthernetIface
```

An ethernet link must be connected to its attached PHYs. Connection is done using the `connect` command.

Listing 40. Connect Syntax

```
ethlink.connect device=phy:PHYIface
```

The eTSEC programmable registers that occupy memory-mapped space are named according to P2020 QorIQ integrated processor reference manual. All the eTSEC registers are 4-byte wide.

To set MAC address MACSTNADDR1 and MACSTNADDR2 registers should be filled. The value of the station address written into MACSTNADDR1 and MACSTNADDR2 is byte reversed from how it would appear in the DA field of a frame in memory. For example, for a station address of 0x12345678ABCD, MACSTNADDR1 is set to 0xCDAB7856 and MACSTNADDR2 is set to 0x34120000.

Listing 41. Setting registers via API

```
// Write MACSTNADDR1 register value to set MAC to 00:00:00:00:00:01
temu_writeValueU32(etsec, "MACSTNADDR1", 0x01000000, 0);
```

Listing 42. Setting registers via Command Line

```
# Write MACSTNADDR1 register value to set MAC to 00:00:00:00:00:01
etsec.MACSTNADDR1 = 0x01000000
```

MAC address also can be set via setMAC command:

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Listing 43. Set MAC

```
etsec.setMAC mac=\"00:00:00:00:00:01\"
```

10.7.3. @eTSEC Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @eTSEC
new	Create new instance of eTSEC

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

10.7.4. eTSEC Reference

Properties

Name	Type	Description
ATTR	uint32_t	Attribute register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ATTRColdResetValue	uint32_t	Attribute register
ATTRELI	uint32_t	Attribute extract length and extract index register
ATTRELIColdResetValue	uint32_t	Attribute extract length and extract index register
ATTRELIForcedBits	uint32_t	Attribute extract length and extract index register
ATTRELIForcedFlippedBits	uint32_t	Attribute extract length and extract index register
ATTRELIReadMask	uint32_t	Attribute extract length and extract index register
ATTRELIResetMask	uint32_t	Attribute extract length and extract index register
ATTRELIResetValue	uint32_t	Attribute extract length and extract index register
ATTRELIWriteMask	uint32_t	Attribute extract length and extract index register
ATTRForcedBits	uint32_t	Attribute register
ATTRForcedFlippedBits	uint32_t	Attribute register
ATTRReadMask	uint32_t	Attribute register
ATTRResetMask	uint32_t	Attribute register
ATTRResetValue	uint32_t	Attribute register
ATTRWriteMask	uint32_t	Attribute register
CAM	[uint32_t; 2]	Carry mask register
CAR	[uint32_t; 2]	Carry register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
DFVLAN	uint32_t	Default VLAN control word
DFVLANColdResetValue	uint32_t	Default VLAN control word
DFVLANForcedBits	uint32_t	Default VLAN control word
DFVLANForcedFlippedBits	uint32_t	Default VLAN control word
DFVLANReadMask	uint32_t	Default VLAN control word
DFVLANResetMask	uint32_t	Default VLAN control word

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
DFVLANResetValue	uint32_t	Default VLAN control word
DFVLANWriteMask	uint32_t	Default VLAN control word
DMACTRL	uint32_t	DMA control register
DMACTRLColdResetValue	uint32_t	DMA control register
DMACTRLForcedBits	uint32_t	DMA control register
DMACTRLForcedFlippedBits	uint32_t	DMA control register
DMACTRLReadMask	uint32_t	DMA control register
DMACTRLResetMask	uint32_t	DMA control register
DMACTRLResetValue	uint32_t	DMA control register
DMACTRLWriteMask	uint32_t	DMA control register
ECNTRL	uint32_t	Ethernet control register
ECNTRLColdResetValue	uint32_t	Ethernet control register
ECNTRLForcedBits	uint32_t	Ethernet control register
ECNTRLForcedFlippedBits	uint32_t	Ethernet control register
ECNTRLReadMask	uint32_t	Ethernet control register
ECNTRLResetMask	uint32_t	Ethernet control register
ECNTRLResetValue	uint32_t	Ethernet control register
ECNTRLWriteMask	uint32_t	Ethernet control register
EDIS	uint32_t	Error disabled register
EDISColdResetValue	uint32_t	Error disabled register
EDISForcedBits	uint32_t	Error disabled register
EDISForcedFlippedBits	uint32_t	Error disabled register
EDISReadMask	uint32_t	Error disabled register
EDISResetMask	uint32_t	Error disabled register
EDISResetValue	uint32_t	Error disabled register
EDISWriteMask	uint32_t	Error disabled register
GADDR	[uint32_t; 8]	Group address register n
HAFDUP	uint32_t	Half-duplex control register
HAFDUPColdResetValue	uint32_t	Half-duplex control register
HAFDUPForcedBits	uint32_t	Half-duplex control register
HAFDUPForcedFlippedBits	uint32_t	Half-duplex control register
HAFDUPReadMask	uint32_t	Half-duplex control register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
HAFDUPResetMask	uint32_t	Half-duplex control register
HAFDUPResetValue	uint32_t	Half-duplex control register
HAFDUPWriteMask	uint32_t	Half-duplex control register
IEVENT	uint32_t	Interrupt event register
IEVENTColdResetValue	uint32_t	Interrupt event register
IEVENTForcedBits	uint32_t	Interrupt event register
IEVENTForcedFlippedBits	uint32_t	Interrupt event register
IEVENTReadMask	uint32_t	Interrupt event register
IEVENTResetMask	uint32_t	Interrupt event register
IEVENTResetValue	uint32_t	Interrupt event register
IEVENTWriteMask	uint32_t	Interrupt event register
IFSTAT	uint32_t	Interface status register
IFSTATColdResetValue	uint32_t	Interface status register
IFSTATForcedBits	uint32_t	Interface status register
IFSTATForcedFlippedBits	uint32_t	Interface status register
IFSTATReadMask	uint32_t	Interface status register
IFSTATResetMask	uint32_t	Interface status register
IFSTATResetValue	uint32_t	Interface status register
IFSTATWriteMask	uint32_t	Interface status register
IGADDR	[uint32_t; 8]	Individual/group address register n
IMASK	uint32_t	Interrupt mask register
IMASKColdResetValue	uint32_t	Interrupt mask register
IMASKForcedBits	uint32_t	Interrupt mask register
IMASKForcedFlippedBits	uint32_t	Interrupt mask register
IMASKReadMask	uint32_t	Interrupt mask register
IMASKResetMask	uint32_t	Interrupt mask register
IMASKResetValue	uint32_t	Interrupt mask register
IMASKWriteMask	uint32_t	Interrupt mask register
IPGIFG	uint32_t	Inter-packet/inter-frame gap register
IPGIFGColdResetValue	uint32_t	Inter-packet/inter-frame gap register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
IPGIFGForcedBits	uint32_t	Inter-packet/inter-frame gap register
IPGIFGForcedFlippedBits	uint32_t	Inter-packet/inter-frame gap register
IPGIFGReadMask	uint32_t	Inter-packet/inter-frame gap register
IPGIFGResetMask	uint32_t	Inter-packet/inter-frame gap register
IPGIFGResetValue	uint32_t	Inter-packet/inter-frame gap register
IPGIFGWriteMask	uint32_t	Inter-packet/inter-frame gap register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
MACCFG1	uint32_t	MAC configuration register 1
MACCFG1ColdResetValue	uint32_t	MAC configuration register 1
MACCFG1ForcedBits	uint32_t	MAC configuration register 1
MACCFG1ForcedFlippedBits	uint32_t	MAC configuration register 1
MACCFG1ReadMask	uint32_t	MAC configuration register 1
MACCFG1ResetMask	uint32_t	MAC configuration register 1
MACCFG1ResetValue	uint32_t	MAC configuration register 1
MACCFG1WriteMask	uint32_t	MAC configuration register 1
MACCFG2	uint32_t	MAC configuration register 2
MACCFG2ColdResetValue	uint32_t	MAC configuration register 2
MACCFG2ForcedBits	uint32_t	MAC configuration register 2
MACCFG2ForcedFlippedBits	uint32_t	MAC configuration register 2
MACCFG2ReadMask	uint32_t	MAC configuration register 2
MACCFG2ResetMask	uint32_t	MAC configuration register 2
MACCFG2ResetValue	uint32_t	MAC configuration register 2
MACCFG2WriteMask	uint32_t	MAC configuration register 2
MACSTNADDR1	uint32_t	MAC station address register 1

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
MACSTNADDR1ColdResetValue	uint32_t	MAC station address register 1
MACSTNADDR1ForcedBits	uint32_t	MAC station address register 1
MACSTNADDR1ForcedFlippedBits	uint32_t	MAC station address register 1
MACSTNADDR1ReadMask	uint32_t	MAC station address register 1
MACSTNADDR1ResetMask	uint32_t	MAC station address register 1
MACSTNADDR1ResetValue	uint32_t	MAC station address register 1
MACSTNADDR1WriteMask	uint32_t	MAC station address register 1
MACSTNADDR2	uint32_t	MAC station address register 2
MACSTNADDR2ColdResetValue	uint32_t	MAC station address register 2
MACSTNADDR2ForcedBits	uint32_t	MAC station address register 2
MACSTNADDR2ForcedFlippedBits	uint32_t	MAC station address register 2
MACSTNADDR2ReadMask	uint32_t	MAC station address register 2
MACSTNADDR2ResetMask	uint32_t	MAC station address register 2
MACSTNADDR2ResetValue	uint32_t	MAC station address register 2
MACSTNADDR2WriteMask	uint32_t	MAC station address register 2
MACnADDR1	[uint32_t; 15]	MAC exact match address n, part 1
MACnADDR2	[uint32_t; 15]	MAC exact match address n, part 2
MAXFRM	uint32_t	Maximum frame length register
MAXFRMColdResetValue	uint32_t	Maximum frame length register
MAXFRMForcedBits	uint32_t	Maximum frame length register
MAXFRMForcedFlippedBits	uint32_t	Maximum frame length register
MAXFRMReadMask	uint32_t	Maximum frame length register
MAXFRMResetMask	uint32_t	Maximum frame length register
MAXFRMResetValue	uint32_t	Maximum frame length register
MAXFRMWriteMask	uint32_t	Maximum frame length register
MIIMADD	uint32_t	MII management address register
MIIMADDColdResetValue	uint32_t	MII management address register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
MIIMADDForcedBits	uint32_t	MII management address register
MIIMADDForcedFlippedBits	uint32_t	MII management address register
MIIMADDReadMask	uint32_t	MII management address register
MIIMADDResetMask	uint32_t	MII management address register
MIIMADDResetValue	uint32_t	MII management address register
MIIMADDWriteMask	uint32_t	MII management address register
MIIMCFG	uint32_t	MII management configuration register
MIIMCFGColdResetValue	uint32_t	MII management configuration register
MIIMCFGForcedBits	uint32_t	MII management configuration register
MIIMCFGForcedFlippedBits	uint32_t	MII management configuration register
MIIMCFGReadMask	uint32_t	MII management configuration register
MIIMCFGResetMask	uint32_t	MII management configuration register
MIIMCFGResetValue	uint32_t	MII management configuration register
MIIMCFGWriteMask	uint32_t	MII management configuration register
MIIMCOM	uint32_t	MII management command register
MIIMCOMColdResetValue	uint32_t	MII management command register
MIIMCOMForcedBits	uint32_t	MII management command register
MIIMCOMForcedFlippedBits	uint32_t	MII management command register

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Name	Type	Description
MIIMCOMReadMask	uint32_t	MII management command register
MIIMCOMResetMask	uint32_t	MII management command register
MIIMCOMResetValue	uint32_t	MII management command register
MIIMCOMWriteMask	uint32_t	MII management command register
MIIMCON	uint32_t	MII management control register
MIIMCONColdResetValue	uint32_t	MII management control register
MIIMCONForcedBits	uint32_t	MII management control register
MIIMCONForcedFlippedBits	uint32_t	MII management control register
MIIMCONReadMask	uint32_t	MII management control register
MIIMCONResetMask	uint32_t	MII management control register
MIIMCONResetValue	uint32_t	MII management control register
MIIMCONWriteMask	uint32_t	MII management control register
MIIMIND	uint32_t	MII management indicator register
MIIMINDColdResetValue	uint32_t	MII management indicator register
MIIMINDForcedBits	uint32_t	MII management indicator register
MIIMINDForcedFlippedBits	uint32_t	MII management indicator register
MIIMINDReadMask	uint32_t	MII management indicator register
MIIMINDResetMask	uint32_t	MII management indicator register

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Name	Type	Description
MIIMINDResetValue	uint32_t	MII management indicator register
MIIMINDWriteMask	uint32_t	MII management indicator register
MIIMSTAT	uint32_t	MII management status register
MIIMSTATColdResetValue	uint32_t	MII management status register
MIIMSTATForcedBits	uint32_t	MII management status register
MIIMSTATForcedFlippedBits	uint32_t	MII management status register
MIIMSTATReadMask	uint32_t	MII management status register
MIIMSTATResetMask	uint32_t	MII management status register
MIIMSTATResetValue	uint32_t	MII management status register
MIIMSTATWriteMask	uint32_t	MII management status register
MRBLR	uint32_t	Maximum receive buffer length register
MRBLRColdResetValue	uint32_t	Maximum receive buffer length register
MRBLRForcedBits	uint32_t	Maximum receive buffer length register
MRBLRForcedFlippedBits	uint32_t	Maximum receive buffer length register
MRBLRReadMask	uint32_t	Maximum receive buffer length register
MRBLRResetMask	uint32_t	Maximum receive buffer length register
MRBLRResetValue	uint32_t	Maximum receive buffer length register
MRBLRWriteMask	uint32_t	Maximum receive buffer length register
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
PTV	uint32_t	Pause time value register
PTVColdResetValue	uint32_t	Pause time value register
PTVForcedBits	uint32_t	Pause time value register
PTVForcedFlippedBits	uint32_t	Pause time value register
PTVReadMask	uint32_t	Pause time value register

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Name	Type	Description
PTVResetMask	uint32_t	Pause time value register
PTVResetValue	uint32_t	Pause time value register
PTVWriteMask	uint32_t	Pause time value register
RALN	uint32_t	Receive alignment error counter
RALNColdResetValue	uint32_t	Receive alignment error counter
RALNForcedBits	uint32_t	Receive alignment error counter
RALNForcedFlippedBits	uint32_t	Receive alignment error counter
RALNReadMask	uint32_t	Receive alignment error counter
RALNResetMask	uint32_t	Receive alignment error counter
RALNResetValue	uint32_t	Receive alignment error counter
RALNWriteMask	uint32_t	Receive alignment error counter
RBASE	[uint32_t; 8]	RxBD base address of ring n
RBASEH	uint32_t	RxBD base address high bits
RBASEHColdResetValue	uint32_t	RxBD base address high bits
RBASEHForcedBits	uint32_t	RxBD base address high bits
RBASEHForcedFlippedBits	uint32_t	RxBD base address high bits
RBASEHReadMask	uint32_t	RxBD base address high bits
RBASEHResetMask	uint32_t	RxBD base address high bits
RBASEHResetValue	uint32_t	RxBD base address high bits
RBASEHWriteMask	uint32_t	RxBD base address high bits
RBCA	uint32_t	Receive broadcast packet counter
RBCAColdResetValue	uint32_t	Receive broadcast packet counter
RBCAForcedBits	uint32_t	Receive broadcast packet counter

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Name	Type	Description
RBCAForcedFlippedBits	uint32_t	Receive broadcast packet counter
RBCAReadMask	uint32_t	Receive broadcast packet counter
RBCAResetMask	uint32_t	Receive broadcast packet counter
RBCAResetValue	uint32_t	Receive broadcast packet counter
RBCAWriteMask	uint32_t	Receive broadcast packet counter
RBDBPH	uint32_t	Rx data buffer pointer high bits
RBDBPHColdResetValue	uint32_t	Rx data buffer pointer high bits
RBDBPHForcedBits	uint32_t	Rx data buffer pointer high bits
RBDBPHForcedFlippedBits	uint32_t	Rx data buffer pointer high bits
RBDBPHReadMask	uint32_t	Rx data buffer pointer high bits
RBDBPHResetMask	uint32_t	Rx data buffer pointer high bits
RBDBPHResetValue	uint32_t	Rx data buffer pointer high bits
RBDBPHWriteMask	uint32_t	Rx data buffer pointer high bits
RBIFX	uint32_t	Receive bit field extract control register
RBIFXColdResetValue	uint32_t	Receive bit field extract control register
RBIFXForcedBits	uint32_t	Receive bit field extract control register
RBIFXForcedFlippedBits	uint32_t	Receive bit field extract control register
RBIFXReadMask	uint32_t	Receive bit field extract control register
RBIFXResetMask	uint32_t	Receive bit field extract control register
RBIFXResetValue	uint32_t	Receive bit field extract control register
RBIFXWriteMask	uint32_t	Receive bit field extract control register
RBPTR	[uint32_t; 8]	RxBD pointer for ring n
RBYT	uint32_t	Receive byte counter

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Name	Type	Description
RBYTColdResetValue	uint32_t	Receive byte counter
RBYTForcedBits	uint32_t	Receive byte counter
RBYTForcedFlippedBits	uint32_t	Receive byte counter
RBYTReadMask	uint32_t	Receive byte counter
RBYTResetMask	uint32_t	Receive byte counter
RBYTResetValue	uint32_t	Receive byte counter
RBYTWriteMask	uint32_t	Receive byte counter
RCSE	uint32_t	Receive carrier sense error counter
RCSEColdResetValue	uint32_t	Receive carrier sense error counter
RCSEForcedBits	uint32_t	Receive carrier sense error counter
RCSEForcedFlippedBits	uint32_t	Receive carrier sense error counter
RCSEReadMask	uint32_t	Receive carrier sense error counter
RCSEResetMask	uint32_t	Receive carrier sense error counter
RCSEResetValue	uint32_t	Receive carrier sense error counter
RCSEWriteMask	uint32_t	Receive carrier sense error counter
RCTRL	uint32_t	Receive control register
RCTRLColdResetValue	uint32_t	Receive control register
RCTRLForcedBits	uint32_t	Receive control register
RCTRLForcedFlippedBits	uint32_t	Receive control register
RCTRLReadMask	uint32_t	Receive control register
RCTRLResetMask	uint32_t	Receive control register
RCTRLResetValue	uint32_t	Receive control register
RCTRLWriteMask	uint32_t	Receive control register
RDRP	uint32_t	Receive drop counter
RDRPColdResetValue	uint32_t	Receive drop counter
RDRPForcedBits	uint32_t	Receive drop counter

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Name	Type	Description
RDRPForcedFlippedBits	uint32_t	Receive drop counter
RDRPReadMask	uint32_t	Receive drop counter
RDRPResetMask	uint32_t	Receive drop counter
RDRPResetValue	uint32_t	Receive drop counter
RDRPWriteMask	uint32_t	Receive drop counter
RFBPTR	[uint32_t; 8]	Last free RxBD pointer for ring n
RFCS	uint32_t	Receive FCS error counter
RFCSColdResetValue	uint32_t	Receive FCS error counter
RFCSForcedBits	uint32_t	Receive FCS error counter
RFCSForcedFlippedBits	uint32_t	Receive FCS error counter
RFCSReadMask	uint32_t	Receive FCS error counter
RFCSResetMask	uint32_t	Receive FCS error counter
RFCSResetValue	uint32_t	Receive FCS error counter
RFCSWriteMask	uint32_t	Receive FCS error counter
RFLR	uint32_t	Receive frame length error counter
RFLRColdResetValue	uint32_t	Receive frame length error counter
RFLRForcedBits	uint32_t	Receive frame length error counter
RFLRForcedFlippedBits	uint32_t	Receive frame length error counter
RFLRReadMask	uint32_t	Receive frame length error counter
RFLRResetMask	uint32_t	Receive frame length error counter
RFLRResetValue	uint32_t	Receive frame length error counter
RFLRWriteMask	uint32_t	Receive frame length error counter
RFRG	uint32_t	Receive fragments counter
RFRGColdResetValue	uint32_t	Receive fragments counter
RFRGForcedBits	uint32_t	Receive fragments counter

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Name	Type	Description
RFRGForcedFlippedBits	uint32_t	Receive fragments counter
RFRGReadMask	uint32_t	Receive fragments counter
RFRGResetMask	uint32_t	Receive fragments counter
RFRGResetValue	uint32_t	Receive fragments counter
RFRGWriteMask	uint32_t	Receive fragments counter
RJBR	uint32_t	Receive jabber counter
RJBRColdResetValue	uint32_t	Receive jabber counter
RJBRForcedBits	uint32_t	Receive jabber counter
RJBRForcedFlippedBits	uint32_t	Receive jabber counter
RJBRReadMask	uint32_t	Receive jabber counter
RJBRResetMask	uint32_t	Receive jabber counter
RJBRResetValue	uint32_t	Receive jabber counter
RJBRWriteMask	uint32_t	Receive jabber counter
RMCA	uint32_t	Receive multicast packet counter
RMCAColdResetValue	uint32_t	Receive multicast packet counter
RMCAForcedBits	uint32_t	Receive multicast packet counter
RMCAForcedFlippedBits	uint32_t	Receive multicast packet counter
RMCAReadMask	uint32_t	Receive multicast packet counter
RMCAResetMask	uint32_t	Receive multicast packet counter
RMCAResetValue	uint32_t	Receive multicast packet counter
RMCAWriteMask	uint32_t	Receive multicast packet counter
ROVR	uint32_t	Receive oversize packet counter
ROVRColdResetValue	uint32_t	Receive oversize packet counter
ROVRForcedBits	uint32_t	Receive oversize packet counter
ROVRForcedFlippedBits	uint32_t	Receive oversize packet counter
ROVRReadMask	uint32_t	Receive oversize packet counter

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Name	Type	Description
ROVRResetMask	uint32_t	Receive oversize packet counter
ROVRResetValue	uint32_t	Receive oversize packet counter
ROVRWriteMask	uint32_t	Receive oversize packet counter
RPKT	uint32_t	Receive packet counter
RPKTColdResetValue	uint32_t	Receive packet counter
RPKTForcedBits	uint32_t	Receive packet counter
RPKTForcedFlippedBits	uint32_t	Receive packet counter
RPKTReadMask	uint32_t	Receive packet counter
RPKTResetMask	uint32_t	Receive packet counter
RPKTResetValue	uint32_t	Receive packet counter
RPKTWriteMask	uint32_t	Receive packet counter
RQFAR	uint32_t	Receive queue filing table address register
RQFARColdResetValue	uint32_t	Receive queue filing table address register
RQFARForcedBits	uint32_t	Receive queue filing table address register
RQFARForcedFlippedBits	uint32_t	Receive queue filing table address register
RQFARReadMask	uint32_t	Receive queue filing table address register
RQFARResetMask	uint32_t	Receive queue filing table address register
RQFARResetValue	uint32_t	Receive queue filing table address register
RQFARWriteMask	uint32_t	Receive queue filing table address register
RQFCR	uint32_t	Receive queue filing table control register
RQFCRColdResetValue	uint32_t	Receive queue filing table control register
RQFCRForcedBits	uint32_t	Receive queue filing table control register
RQFCRForcedFlippedBits	uint32_t	Receive queue filing table control register

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Name	Type	Description
RQFCRReadMask	uint32_t	Receive queue filing table control register
RQFCRResetMask	uint32_t	Receive queue filing table control register
RQFCRResetValue	uint32_t	Receive queue filing table control register
RQFCRWriteMask	uint32_t	Receive queue filing table control register
RQFPR	uint32_t	Receive queue filing table property register
RQFPRColdResetValue	uint32_t	Receive queue filing table property register
RQFPRForcedBits	uint32_t	Receive queue filing table property register
RQFPRForcedFlippedBits	uint32_t	Receive queue filing table property register
RQFPRReadMask	uint32_t	Receive queue filing table property register
RQFPRResetMask	uint32_t	Receive queue filing table property register
RQFPRResetValue	uint32_t	Receive queue filing table property register
RQFPRWriteMask	uint32_t	Receive queue filing table property register
RQPRM	[uint32_t; 8]	Receive queue parameters register
RQUEUE	uint32_t	Receive queue control register
RQUEUEColdResetValue	uint32_t	Receive queue control register
RQUEUEForcedBits	uint32_t	Receive queue control register
RQUEUEForcedFlippedBits	uint32_t	Receive queue control register
RQUEUEReadMask	uint32_t	Receive queue control register
RQUEUEResetMask	uint32_t	Receive queue control register
RQUEUEResetValue	uint32_t	Receive queue control register
RQUEUEWriteMask	uint32_t	Receive queue control register
RREJ	uint32_t	Receive filer rejected packet counter

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Name	Type	Description
RREJColdResetValue	uint32_t	Receive filer rejected packet counter
RREJForcedBits	uint32_t	Receive filer rejected packet counter
RREJForcedFlippedBits	uint32_t	Receive filer rejected packet counter
RREJReadMask	uint32_t	Receive filer rejected packet counter
RREJResetMask	uint32_t	Receive filer rejected packet counter
RREJResetValue	uint32_t	Receive filer rejected packet counter
RREJWriteMask	uint32_t	Receive filer rejected packet counter
RSTAT	uint32_t	Receive status register
RSTATColdResetValue	uint32_t	Receive status register
RSTATForcedBits	uint32_t	Receive status register
RSTATForcedFlippedBits	uint32_t	Receive status register
RSTATReadMask	uint32_t	Receive status register
RSTATResetMask	uint32_t	Receive status register
RSTATResetValue	uint32_t	Receive status register
RSTATWriteMask	uint32_t	Receive status register
RUND	uint32_t	Receive undersize packet counter
RUNDColdResetValue	uint32_t	Receive undersize packet counter
RUNDForcedBits	uint32_t	Receive undersize packet counter
RUNDForcedFlippedBits	uint32_t	Receive undersize packet counter
RUNDReadMask	uint32_t	Receive undersize packet counter
RUNDResetMask	uint32_t	Receive undersize packet counter
RUNDResetValue	uint32_t	Receive undersize packet counter

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Name	Type	Description
RUNDWriteMask	uint32_t	Receive undersize packet counter
RXCF	uint32_t	Receive control frame counter
RXCFColdResetValue	uint32_t	Receive control frame counter
RXCFForcedBits	uint32_t	Receive control frame counter
RXCFForcedFlippedBits	uint32_t	Receive control frame counter
RXCFReadMask	uint32_t	Receive control frame counter
RXCFResetMask	uint32_t	Receive control frame counter
RXCFResetValue	uint32_t	Receive control frame counter
RXCFWriteMask	uint32_t	Receive control frame counter
RXIC	uint32_t	Receive interrupt coalescing register
RXICColdResetValue	uint32_t	Receive interrupt coalescing register
RXICForcedBits	uint32_t	Receive interrupt coalescing register
RXICForcedFlippedBits	uint32_t	Receive interrupt coalescing register
RXICReadMask	uint32_t	Receive interrupt coalescing register
RXICResetMask	uint32_t	Receive interrupt coalescing register
RXICResetValue	uint32_t	Receive interrupt coalescing register
RXICWriteMask	uint32_t	Receive interrupt coalescing register
RXPF	uint32_t	Receive PAUSE frame counter
RXPFColdResetValue	uint32_t	Receive PAUSE frame counter
RXPFForcedBits	uint32_t	Receive PAUSE frame counter
RXPFForcedFlippedBits	uint32_t	Receive PAUSE frame counter
RXPFReadMask	uint32_t	Receive PAUSE frame counter
RXPFResetMask	uint32_t	Receive PAUSE frame counter
RXPFResetValue	uint32_t	Receive PAUSE frame counter
RXPFWriteMask	uint32_t	Receive PAUSE frame counter

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Name	Type	Description
RXUO	uint32_t	Receive unknown opcode counter
RXUOColdResetValue	uint32_t	Receive unknown opcode counter
RXUOForcedBits	uint32_t	Receive unknown opcode counter
RXUOForcedFlippedBits	uint32_t	Receive unknown opcode counter
RXUOReadMask	uint32_t	Receive unknown opcode counter
RXUOResetMask	uint32_t	Receive unknown opcode counter
RXUOResetValue	uint32_t	Receive unknown opcode counter
RXUOWriteMask	uint32_t	Receive unknown opcode counter
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TBASE	[uint32_t; 8]	TxBD base address of ring n
TBASEH	uint32_t	TxBD base address high bits
TBASEHColdResetValue	uint32_t	TxBD base address high bits
TBASEHForcedBits	uint32_t	TxBD base address high bits
TBASEHForcedFlippedBits	uint32_t	TxBD base address high bits
TBASEHReadMask	uint32_t	TxBD base address high bits
TBASEHResetMask	uint32_t	TxBD base address high bits
TBASEHResetValue	uint32_t	TxBD base address high bits
TBASEHWriteMask	uint32_t	TxBD base address high bits
TBCA	uint32_t	Transmit broadcast packet counter
TBCAColdResetValue	uint32_t	Transmit broadcast packet counter
TBCAForcedBits	uint32_t	Transmit broadcast packet counter
TBCAForcedFlippedBits	uint32_t	Transmit broadcast packet counter

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Name	Type	Description
TBCAReadMask	uint32_t	Transmit broadcast packet counter
TBCAResetMask	uint32_t	Transmit broadcast packet counter
TBCAResetValue	uint32_t	Transmit broadcast packet counter
TBCAWriteMask	uint32_t	Transmit broadcast packet counter
TBDBPH	uint32_t	Tx data buffer pointer high bits
TBDBPHColdResetValue	uint32_t	Tx data buffer pointer high bits
TBDBPHForcedBits	uint32_t	Tx data buffer pointer high bits
TBDBPHForcedFlippedBits	uint32_t	Tx data buffer pointer high bits
TBDBPHReadMask	uint32_t	Tx data buffer pointer high bits
TBDBPHResetMask	uint32_t	Tx data buffer pointer high bits
TBDBPHResetValue	uint32_t	Tx data buffer pointer high bits
TBDBPHWriteMask	uint32_t	Tx data buffer pointer high bits
TBIPA	uint32_t	TBI PHY address register
TBIPAColdResetValue	uint32_t	TBI PHY address register
TBIPAForcedBits	uint32_t	TBI PHY address register
TBIPAForcedFlippedBits	uint32_t	TBI PHY address register
TBIPAReadMask	uint32_t	TBI PHY address register
TBIPAResetMask	uint32_t	TBI PHY address register
TBIPAResetValue	uint32_t	TBI PHY address register
TBIPAWriteMask	uint32_t	TBI PHY address register
TBPTR	[uint32_t; 8]	TxBD pointer for ring n
TBYT	uint32_t	Transmit byte counter
TBYTColdResetValue	uint32_t	Transmit byte counter
TBYTForcedBits	uint32_t	Transmit byte counter
TBYTForcedFlippedBits	uint32_t	Transmit byte counter
TBYTReadMask	uint32_t	Transmit byte counter
TBYTResetMask	uint32_t	Transmit byte counter
TBYTResetValue	uint32_t	Transmit byte counter
TBYTWriteMask	uint32_t	Transmit byte counter

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Name	Type	Description
TCTRL	uint32_t	Transmit control register
TCTRLColdResetValue	uint32_t	Transmit control register
TCTRLForcedBits	uint32_t	Transmit control register
TCTRLForcedFlippedBits	uint32_t	Transmit control register
TCTRLReadMask	uint32_t	Transmit control register
TCTRLResetMask	uint32_t	Transmit control register
TCTRLResetValue	uint32_t	Transmit control register
TCTRLWriteMask	uint32_t	Transmit control register
TDFR	uint32_t	Transmit deferral packet counter
TDFRColdResetValue	uint32_t	Transmit deferral packet counter
TDFRForcedBits	uint32_t	Transmit deferral packet counter
TDFRForcedFlippedBits	uint32_t	Transmit deferral packet counter
TDFRReadMask	uint32_t	Transmit deferral packet counter
TDFRResetMask	uint32_t	Transmit deferral packet counter
TDFRResetValue	uint32_t	Transmit deferral packet counter
TDFRWriteMask	uint32_t	Transmit deferral packet counter
TDRP	uint32_t	Transmit drop frame counter
TDRPColdResetValue	uint32_t	Transmit drop frame counter
TDRPForcedBits	uint32_t	Transmit drop frame counter
TDRPForcedFlippedBits	uint32_t	Transmit drop frame counter
TDRPReadMask	uint32_t	Transmit drop frame counter
TDRPResetMask	uint32_t	Transmit drop frame counter
TDRPResetValue	uint32_t	Transmit drop frame counter
TDRPWriteMask	uint32_t	Transmit drop frame counter
TEDF	uint32_t	Transmit excessive deferral packet counter

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Name	Type	Description
TEDFColdResetValue	uint32_t	Transmit excessive deferral packet counter
TEDFForcedBits	uint32_t	Transmit excessive deferral packet counter
TEDFForcedFlippedBits	uint32_t	Transmit excessive deferral packet counter
TEDFReadMask	uint32_t	Transmit excessive deferral packet counter
TEDFResetMask	uint32_t	Transmit excessive deferral packet counter
TEDFResetValue	uint32_t	Transmit excessive deferral packet counter
TEDFWriteMask	uint32_t	Transmit excessive deferral packet counter
TFCS	uint32_t	Transmit FCS error counter
TFCSColdResetValue	uint32_t	Transmit FCS error counter
TFCSForcedBits	uint32_t	Transmit FCS error counter
TFCSForcedFlippedBits	uint32_t	Transmit FCS error counter
TFCSReadMask	uint32_t	Transmit FCS error counter
TFCSResetMask	uint32_t	Transmit FCS error counter
TFCSResetValue	uint32_t	Transmit FCS error counter
TFCSWriteMask	uint32_t	Transmit FCS error counter
TFRG	uint32_t	Transmit fragments frame counter
TFRGColdResetValue	uint32_t	Transmit fragments frame counter
TFRGForcedBits	uint32_t	Transmit fragments frame counter
TFRGForcedFlippedBits	uint32_t	Transmit fragments frame counter
TFRGReadMask	uint32_t	Transmit fragments frame counter
TFRGResetMask	uint32_t	Transmit fragments frame counter
TFRGResetValue	uint32_t	Transmit fragments frame counter

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Name	Type	Description
TFRGWriteMask	uint32_t	Transmit fragments frame counter
TJBR	uint32_t	Transmit jabber frame counter
TJBRColdResetValue	uint32_t	Transmit jabber frame counter
TJBRForcedBits	uint32_t	Transmit jabber frame counter
TJBRForcedFlippedBits	uint32_t	Transmit jabber frame counter
TJBRReadMask	uint32_t	Transmit jabber frame counter
TJBRResetMask	uint32_t	Transmit jabber frame counter
TJBRResetValue	uint32_t	Transmit jabber frame counter
TJBRWriteMask	uint32_t	Transmit jabber frame counter
TLCL	uint32_t	Transmit late collision packet counter
TLCLColdResetValue	uint32_t	Transmit late collision packet counter
TLCLForcedBits	uint32_t	Transmit late collision packet counter
TLCLForcedFlippedBits	uint32_t	Transmit late collision packet counter
TLCLReadMask	uint32_t	Transmit late collision packet counter
TLCLResetMask	uint32_t	Transmit late collision packet counter
TLCLResetValue	uint32_t	Transmit late collision packet counter
TLCLWriteMask	uint32_t	Transmit late collision packet counter
TMCA	uint32_t	Transmit multicast packet counter
TMCAColdResetValue	uint32_t	Transmit multicast packet counter
TMCAForcedBits	uint32_t	Transmit multicast packet counter
TMCAForcedFlippedBits	uint32_t	Transmit multicast packet counter
TMCAReadMask	uint32_t	Transmit multicast packet counter

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Name	Type	Description
TMCAResetMask	uint32_t	Transmit multicast packet counter
TMCAResetValue	uint32_t	Transmit multicast packet counter
TMCAWriteMask	uint32_t	Transmit multicast packet counter
TMCL	uint32_t	Transmit multi collision packet counter
TMCLColdResetValue	uint32_t	Transmit multi collision packet counter
TMCLForcedBits	uint32_t	Transmit multi collision packet counter
TMCLForcedFlippedBits	uint32_t	Transmit multi collision packet counter
TMCLReadMask	uint32_t	Transmit multi collision packet counter
TMCLResetMask	uint32_t	Transmit multi collision packet counter
TMCLResetValue	uint32_t	Transmit multi collision packet counter
TMCLWriteMask	uint32_t	Transmit multi collision packet counter
TMROFF_H	uint32_t	Timer offset high register
TMROFF_HColdResetValue	uint32_t	Timer offset high register
TMROFF_HForcedBits	uint32_t	Timer offset high register
TMROFF_HForcedFlippedBits	uint32_t	Timer offset high register
TMROFF_HReadMask	uint32_t	Timer offset high register
TMROFF_HResetMask	uint32_t	Timer offset high register
TMROFF_HResetValue	uint32_t	Timer offset high register
TMROFF_HWriteMask	uint32_t	Timer offset high register
TMROFF_L	uint32_t	Timer offset low register
TMROFF_LColdResetValue	uint32_t	Timer offset low register
TMROFF_LForcedBits	uint32_t	Timer offset low register
TMROFF_LForcedFlippedBits	uint32_t	Timer offset low register
TMROFF_LReadMask	uint32_t	Timer offset low register

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Name	Type	Description
TMROFF_LResetMask	uint32_t	Timer offset low register
TMROFF_LResetValue	uint32_t	Timer offset low register
TMROFF_LWriteMask	uint32_t	Timer offset low register
TMR_ACC	uint32_t	Timer accumulator register
TMR_ACCColdResetValue	uint32_t	Timer accumulator register
TMR_ACCForcedBits	uint32_t	Timer accumulator register
TMR_ACCForcedFlippedBits	uint32_t	Timer accumulator register
TMR_ACCReadMask	uint32_t	Timer accumulator register
TMR_ACCResetMask	uint32_t	Timer accumulator register
TMR_ACCResetValue	uint32_t	Timer accumulator register
TMR_ACCWriteMask	uint32_t	Timer accumulator register
TMR_ADD	uint32_t	Timer drift compensation addend register
TMR_ADDColdResetValue	uint32_t	Timer drift compensation addend register
TMR_ADDForcedBits	uint32_t	Timer drift compensation addend register
TMR_ADDForcedFlippedBits	uint32_t	Timer drift compensation addend register
TMR_ADDReadMask	uint32_t	Timer drift compensation addend register
TMR_ADDResetMask	uint32_t	Timer drift compensation addend register
TMR_ADDResetValue	uint32_t	Timer drift compensation addend register
TMR_ADDWriteMask	uint32_t	Timer drift compensation addend register
TMR_ALARM_H	[uint32_t; 2]	Timer alarm high register
TMR_ALARM_L	[uint32_t; 2]	Timer alarm low register
TMR_CNT_H	uint32_t	Timer counter high register
TMR_CNT_HColdResetValue	uint32_t	Timer counter high register
TMR_CNT_HForcedBits	uint32_t	Timer counter high register
TMR_CNT_HForcedFlippedBits	uint32_t	Timer counter high register
TMR_CNT_HReadMask	uint32_t	Timer counter high register

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Name	Type	Description
TMR_CNT_HResetMask	uint32_t	Timer counter high register
TMR_CNT_HResetValue	uint32_t	Timer counter high register
TMR_CNT_HWriteMask	uint32_t	Timer counter high register
TMR_CNT_L	uint32_t	Timer counter low register
TMR_CNT_LColdResetValue	uint32_t	Timer counter low register
TMR_CNT_LForcedBits	uint32_t	Timer counter low register
TMR_CNT_LForcedFlippedBits	uint32_t	Timer counter low register
TMR_CNT_LReadMask	uint32_t	Timer counter low register
TMR_CNT_LResetMask	uint32_t	Timer counter low register
TMR_CNT_LResetValue	uint32_t	Timer counter low register
TMR_CNT_LWriteMask	uint32_t	Timer counter low register
TMR_CTRL	uint32_t	Timer control register
TMR_CTRLColdResetValue	uint32_t	Timer control register
TMR_CTRLForcedBits	uint32_t	Timer control register
TMR_CTRLForcedFlippedBits	uint32_t	Timer control register
TMR_CTRLReadMask	uint32_t	Timer control register
TMR_CTRLResetMask	uint32_t	Timer control register
TMR_CTRLResetValue	uint32_t	Timer control register
TMR_CTRLWriteMask	uint32_t	Timer control register
TMR_ETTS_H	[uint32_t; 2]	External trigger timestamp high register
TMR_ETTS_L	[uint32_t; 2]	External trigger timestamp low register
TMR_FIPER	[uint32_t; 2]	Timer fixed period interval register
TMR_PEMASK	uint32_t	PTP time stamp event mask register
TMR_PEMASKColdResetValue	uint32_t	PTP time stamp event mask register
TMR_PEMASKForcedBits	uint32_t	PTP time stamp event mask register
TMR_PEMASKForcedFlippedBits	uint32_t	PTP time stamp event mask register

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Name	Type	Description
TMR_PEMASKReadMask	uint32_t	PTP time stamp event mask register
TMR_PEMASKResetMask	uint32_t	PTP time stamp event mask register
TMR_PEMASKResetValue	uint32_t	PTP time stamp event mask register
TMR_PEMASKWriteMask	uint32_t	PTP time stamp event mask register
TMR_PEVENT	uint32_t	PTP time stamp event register
TMR_PEVENTColdResetValue	uint32_t	PTP time stamp event register
TMR_PEVENTForcedBits	uint32_t	PTP time stamp event register
TMR_PEVENTForcedFlippedBits	uint32_t	PTP time stamp event register
TMR_PEVENTReadMask	uint32_t	PTP time stamp event register
TMR_PEVENTResetMask	uint32_t	PTP time stamp event register
TMR_PEVENTResetValue	uint32_t	PTP time stamp event register
TMR_PEVENTWriteMask	uint32_t	PTP time stamp event register
TMR_PRSC	uint32_t	Timer prescale register
TMR_PRSCColdResetValue	uint32_t	Timer prescale register
TMR_PRSCForcedBits	uint32_t	Timer prescale register
TMR_PRSCForcedFlippedBits	uint32_t	Timer prescale register
TMR_PRSCReadMask	uint32_t	Timer prescale register
TMR_PRSCResetMask	uint32_t	Timer prescale register
TMR_PRSCResetValue	uint32_t	Timer prescale register
TMR_PRSCWriteMask	uint32_t	Timer prescale register
TMR_RXTS_H	uint32_t	Rx timer time stamp high
TMR_RXTS_HColdResetValue	uint32_t	Rx timer time stamp high
TMR_RXTS_HForcedBits	uint32_t	Rx timer time stamp high
TMR_RXTS_HForcedFlippedBits	uint32_t	Rx timer time stamp high
TMR_RXTS_HReadMask	uint32_t	Rx timer time stamp high
TMR_RXTS_HResetMask	uint32_t	Rx timer time stamp high
TMR_RXTS_HResetValue	uint32_t	Rx timer time stamp high
TMR_RXTS_HWriteMask	uint32_t	Rx timer time stamp high
TMR_RXTS_L	uint32_t	Rx timer time stamp low

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Name	Type	Description
TMR_RXTS_LColdResetValue	uint32_t	Rx timer time stamp low
TMR_RXTS_LForcedBits	uint32_t	Rx timer time stamp low
TMR_RXTS_LForcedFlippedBits	uint32_t	Rx timer time stamp low
TMR_RXTS_LReadMask	uint32_t	Rx timer time stamp low
TMR_RXTS_LResetMask	uint32_t	Rx timer time stamp low
TMR_RXTS_LResetValue	uint32_t	Rx timer time stamp low
TMR_RXTS_LWriteMask	uint32_t	Rx timer time stamp low
TMR_STAT	uint32_t	Time stamp status register
TMR_STATColdResetValue	uint32_t	Time stamp status register
TMR_STATForcedBits	uint32_t	Time stamp status register
TMR_STATForcedFlippedBits	uint32_t	Time stamp status register
TMR_STATReadMask	uint32_t	Time stamp status register
TMR_STATResetMask	uint32_t	Time stamp status register
TMR_STATResetValue	uint32_t	Time stamp status register
TMR_STATWriteMask	uint32_t	Time stamp status register
TMR_TEMASK	uint32_t	Timer event mask register
TMR_TEMASKColdResetValue	uint32_t	Timer event mask register
TMR_TEMASKForcedBits	uint32_t	Timer event mask register
TMR_TEMASKForcedFlippedBits	uint32_t	Timer event mask register
TMR_TEMASKReadMask	uint32_t	Timer event mask register
TMR_TEMASKResetMask	uint32_t	Timer event mask register
TMR_TEMASKResetValue	uint32_t	Timer event mask register
TMR_TEMASKWriteMask	uint32_t	Timer event mask register
TMR_TEVENT	uint32_t	Time stamp event register
TMR_TEVENTColdResetValue	uint32_t	Time stamp event register
TMR_TEVENTForcedBits	uint32_t	Time stamp event register
TMR_TEVENTForcedFlippedBits	uint32_t	Time stamp event register
TMR_TEVENTReadMask	uint32_t	Time stamp event register
TMR_TEVENTResetMask	uint32_t	Time stamp event register
TMR_TEVENTResetValue	uint32_t	Time stamp event register
TMR_TEVENTWriteMask	uint32_t	Time stamp event register

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Name	Type	Description
TMR_TXTS_H	[uint32_t; 2]	Tx time stamp high
TMR_TXTS_ID	[uint32_t; 2]	Tx time stamp identification tag register
TMR_TXTS_L	[uint32_t; 2]	Tx time stamp low
TNCL	uint32_t	Transmit total collision packet counter
TNCLColdResetValue	uint32_t	Transmit total collision packet counter
TNCLForcedBits	uint32_t	Transmit total collision packet counter
TNCLForcedFlippedBits	uint32_t	Transmit total collision packet counter
TNCLReadMask	uint32_t	Transmit total collision packet counter
TNCLResetMask	uint32_t	Transmit total collision packet counter
TNCLResetValue	uint32_t	Transmit total collision packet counter
TNCLWriteMask	uint32_t	Transmit total collision packet counter
TOVR	uint32_t	Transmit oversize frame counter
TOVRColdResetValue	uint32_t	Transmit oversize frame counter
TOVRForcedBits	uint32_t	Transmit oversize frame counter
TOVRForcedFlippedBits	uint32_t	Transmit oversize frame counter
TOVRReadMask	uint32_t	Transmit oversize frame counter
TOVRResetMask	uint32_t	Transmit oversize frame counter
TOVRResetValue	uint32_t	Transmit oversize frame counter
TOVRWriteMask	uint32_t	Transmit oversize frame counter
TPKT	uint32_t	Transmit packet counter

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Name	Type	Description
TPKTColdResetValue	uint32_t	Transmit packet counter
TPKTForcedBits	uint32_t	Transmit packet counter
TPKTForcedFlippedBits	uint32_t	Transmit packet counter
TPKTReadMask	uint32_t	Transmit packet counter
TPKTResetMask	uint32_t	Transmit packet counter
TPKTResetValue	uint32_t	Transmit packet counter
TPKTWriteMask	uint32_t	Transmit packet counter
TQUEUE	uint32_t	Transmit queue control register
TQUEUEColdResetValue	uint32_t	Transmit queue control register
TQUEUEForcedBits	uint32_t	Transmit queue control register
TQUEUEForcedFlippedBits	uint32_t	Transmit queue control register
TQUEUEReadMask	uint32_t	Transmit queue control register
TQUEUEResetMask	uint32_t	Transmit queue control register
TQUEUEResetValue	uint32_t	Transmit queue control register
TQUEUEWriteMask	uint32_t	Transmit queue control register
TR03WT	uint32_t	TxBD rings 0-3 round-robin weightings
TR03WTColdResetValue	uint32_t	TxBD rings 0-3 round-robin weightings
TR03WTForcedBits	uint32_t	TxBD rings 0-3 round-robin weightings
TR03WTForcedFlippedBits	uint32_t	TxBD rings 0-3 round-robin weightings
TR03WTReadMask	uint32_t	TxBD rings 0-3 round-robin weightings
TR03WTResetMask	uint32_t	TxBD rings 0-3 round-robin weightings
TR03WTResetValue	uint32_t	TxBD rings 0-3 round-robin weightings
TR03WTWriteMask	uint32_t	TxBD rings 0-3 round-robin weightings
TR127	uint32_t	Transmit and receive 65- to 127-byte frame counter
TR127ColdResetValue	uint32_t	Transmit and receive 65- to 127-byte frame counter

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Name	Type	Description
TR127ForcedBits	uint32_t	Transmit and receive 65- to 127-byte frame counter
TR127ForcedFlippedBits	uint32_t	Transmit and receive 65- to 127-byte frame counter
TR127ReadMask	uint32_t	Transmit and receive 65- to 127-byte frame counter
TR127ResetMask	uint32_t	Transmit and receive 65- to 127-byte frame counter
TR127ResetValue	uint32_t	Transmit and receive 65- to 127-byte frame counter
TR127WriteMask	uint32_t	Transmit and receive 65- to 127-byte frame counter
TR1K	uint32_t	Transmit and receive 512- to 1023-byte frame counter
TR1KColdResetValue	uint32_t	Transmit and receive 512- to 1023-byte frame counter
TR1KForcedBits	uint32_t	Transmit and receive 512- to 1023-byte frame counter
TR1KForcedFlippedBits	uint32_t	Transmit and receive 512- to 1023-byte frame counter
TR1KReadMask	uint32_t	Transmit and receive 512- to 1023-byte frame counter
TR1KResetMask	uint32_t	Transmit and receive 512- to 1023-byte frame counter
TR1KResetValue	uint32_t	Transmit and receive 512- to 1023-byte frame counter
TR1KWriteMask	uint32_t	Transmit and receive 512- to 1023-byte frame counter
TR255	uint32_t	Transmit and receive 128- to 255-byte frame counter
TR255ColdResetValue	uint32_t	Transmit and receive 128- to 255-byte frame counter
TR255ForcedBits	uint32_t	Transmit and receive 128- to 255-byte frame counter
TR255ForcedFlippedBits	uint32_t	Transmit and receive 128- to 255-byte frame counter

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Name	Type	Description
TR255ReadMask	uint32_t	Transmit and receive 128- to 255-byte frame counter
TR255ResetMask	uint32_t	Transmit and receive 128- to 255-byte frame counter
TR255ResetValue	uint32_t	Transmit and receive 128- to 255-byte frame counter
TR255WriteMask	uint32_t	Transmit and receive 128- to 255-byte frame counter
TR47WT	uint32_t	TxBD rings 4-7 round-robin weightings
TR47WTColdResetValue	uint32_t	TxBD rings 4-7 round-robin weightings
TR47WTForcedBits	uint32_t	TxBD rings 4-7 round-robin weightings
TR47WTForcedFlippedBits	uint32_t	TxBD rings 4-7 round-robin weightings
TR47WTReadMask	uint32_t	TxBD rings 4-7 round-robin weightings
TR47WTResetMask	uint32_t	TxBD rings 4-7 round-robin weightings
TR47WTResetValue	uint32_t	TxBD rings 4-7 round-robin weightings
TR47WTWriteMask	uint32_t	TxBD rings 4-7 round-robin weightings
TR511	uint32_t	Transmit and receive 256- to 511-byte frame counter
TR511ColdResetValue	uint32_t	Transmit and receive 256- to 511-byte frame counter
TR511ForcedBits	uint32_t	Transmit and receive 256- to 511-byte frame counter
TR511ForcedFlippedBits	uint32_t	Transmit and receive 256- to 511-byte frame counter
TR511ReadMask	uint32_t	Transmit and receive 256- to 511-byte frame counter
TR511ResetMask	uint32_t	Transmit and receive 256- to 511-byte frame counter

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Name	Type	Description
TR511ResetValue	uint32_t	Transmit and receive 256- to 511-byte frame counter
TR511WriteMask	uint32_t	Transmit and receive 256- to 511-byte frame counter
TR64	uint32_t	Transmit and receive 64-byte frame counter
TR64ColdResetValue	uint32_t	Transmit and receive 64-byte frame counter
TR64ForcedBits	uint32_t	Transmit and receive 64-byte frame counter
TR64ForcedFlippedBits	uint32_t	Transmit and receive 64-byte frame counter
TR64ReadMask	uint32_t	Transmit and receive 64-byte frame counter
TR64ResetMask	uint32_t	Transmit and receive 64-byte frame counter
TR64ResetValue	uint32_t	Transmit and receive 64-byte frame counter
TR64WriteMask	uint32_t	Transmit and receive 64-byte frame counter
TRMAX	uint32_t	Transmit and receive 1024- to 1518-byte frame counter
TRMAXColdResetValue	uint32_t	Transmit and receive 1024- to 1518-byte frame counter
TRMAXForcedBits	uint32_t	Transmit and receive 1024- to 1518-byte frame counter
TRMAXForcedFlippedBits	uint32_t	Transmit and receive 1024- to 1518-byte frame counter
TRMAXReadMask	uint32_t	Transmit and receive 1024- to 1518-byte frame counter
TRMAXResetMask	uint32_t	Transmit and receive 1024- to 1518-byte frame counter
TRMAXResetValue	uint32_t	Transmit and receive 1024- to 1518-byte frame counter
TRMAXWriteMask	uint32_t	Transmit and receive 1024- to 1518-byte frame counter

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Name	Type	Description
TRMGV	uint32_t	Transmit and receive good VLAN frame counter
TRMGVColdResetValue	uint32_t	Transmit and receive good VLAN frame counter
TRMGVForcedBits	uint32_t	Transmit and receive good VLAN frame counter
TRMGVForcedFlippedBits	uint32_t	Transmit and receive good VLAN frame counter
TRMGVReadMask	uint32_t	Transmit and receive good VLAN frame counter
TRMGVResetMask	uint32_t	Transmit and receive good VLAN frame counter
TRMGVResetValue	uint32_t	Transmit and receive good VLAN frame counter
TRMGVWriteMask	uint32_t	Transmit and receive good VLAN frame counter
TSCL	uint32_t	Transmit single collision packet counter
TSCLColdResetValue	uint32_t	Transmit single collision packet counter
TSCLForcedBits	uint32_t	Transmit single collision packet counter
TSCLForcedFlippedBits	uint32_t	Transmit single collision packet counter
TSCLReadMask	uint32_t	Transmit single collision packet counter
TSCLResetMask	uint32_t	Transmit single collision packet counter
TSCLResetValue	uint32_t	Transmit single collision packet counter
TSCLWriteMask	uint32_t	Transmit single collision packet counter
TSEC_ID	uint32_t	Controller ID register
TSEC_ID2	uint32_t	Controller ID register 2
TSEC_ID2ColdResetValue	uint32_t	Controller ID register 2
TSEC_ID2ForcedBits	uint32_t	Controller ID register 2

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Name	Type	Description
TSEC_ID2ForcedFlippedBits	uint32_t	Controller ID register 2
TSEC_ID2ReadMask	uint32_t	Controller ID register 2
TSEC_ID2ResetMask	uint32_t	Controller ID register 2
TSEC_ID2ResetValue	uint32_t	Controller ID register 2
TSEC_ID2WriteMask	uint32_t	Controller ID register 2
TSEC_IDColdResetValue	uint32_t	Controller ID register
TSEC_IDForcedBits	uint32_t	Controller ID register
TSEC_IDForcedFlippedBits	uint32_t	Controller ID register
TSEC_IDReadMask	uint32_t	Controller ID register
TSEC_IDResetMask	uint32_t	Controller ID register
TSEC_IDResetValue	uint32_t	Controller ID register
TSEC_IDWriteMask	uint32_t	Controller ID register
TSTAT	uint32_t	Transmit status register
TSTATColdResetValue	uint32_t	Transmit status register
TSTATForcedBits	uint32_t	Transmit status register
TSTATForcedFlippedBits	uint32_t	Transmit status register
TSTATReadMask	uint32_t	Transmit status register
TSTATResetMask	uint32_t	Transmit status register
TSTATResetValue	uint32_t	Transmit status register
TSTATWriteMask	uint32_t	Transmit status register
TUND	uint32_t	Transmit undersize frame counter
TUNDColdResetValue	uint32_t	Transmit undersize frame counter
TUNDForcedBits	uint32_t	Transmit undersize frame counter
TUNDForcedFlippedBits	uint32_t	Transmit undersize frame counter
TUNDReadMask	uint32_t	Transmit undersize frame counter
TUNDResetMask	uint32_t	Transmit undersize frame counter
TUNDResetValue	uint32_t	Transmit undersize frame counter

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Name	Type	Description
TUNDWriteMask	uint32_t	Transmit undersize frame counter
TXCF	uint32_t	Transmit control frame counter
TXCFColdResetValue	uint32_t	Transmit control frame counter
TXCFForcedBits	uint32_t	Transmit control frame counter
TXCFForcedFlippedBits	uint32_t	Transmit control frame counter
TXCFReadMask	uint32_t	Transmit control frame counter
TXCFResetMask	uint32_t	Transmit control frame counter
TXCFResetValue	uint32_t	Transmit control frame counter
TXCFWriteMask	uint32_t	Transmit control frame counter
TXCL	uint32_t	Transmit excessive collision packet counter
TXCLColdResetValue	uint32_t	Transmit excessive collision packet counter
TXCLForcedBits	uint32_t	Transmit excessive collision packet counter
TXCLForcedFlippedBits	uint32_t	Transmit excessive collision packet counter
TXCLReadMask	uint32_t	Transmit excessive collision packet counter
TXCLResetMask	uint32_t	Transmit excessive collision packet counter
TXCLResetValue	uint32_t	Transmit excessive collision packet counter
TXCLWriteMask	uint32_t	Transmit excessive collision packet counter
TXIC	uint32_t	Transmit interrupt coalescing register
TXICColdResetValue	uint32_t	Transmit interrupt coalescing register
TXICForcedBits	uint32_t	Transmit interrupt coalescing register
TXICForcedFlippedBits	uint32_t	Transmit interrupt coalescing register
TXICReadMask	uint32_t	Transmit interrupt coalescing register

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Name	Type	Description
TXICResetMask	uint32_t	Transmit interrupt coalescing register
TXICResetValue	uint32_t	Transmit interrupt coalescing register
TXICWriteMask	uint32_t	Transmit interrupt coalescing register
TXPF	uint32_t	Transmit PAUSE control frame counter
TXPFColdResetValue	uint32_t	Transmit PAUSE control frame counter
TXPFForcedBits	uint32_t	Transmit PAUSE control frame counter
TXPFForcedFlippedBits	uint32_t	Transmit PAUSE control frame counter
TXPFReadMask	uint32_t	Transmit PAUSE control frame counter
TXPFResetMask	uint32_t	Transmit PAUSE control frame counter
TXPFResetValue	uint32_t	Transmit PAUSE control frame counter
TXPFWriteMask	uint32_t	Transmit PAUSE control frame counter
TimeSource	*void	Time source object
config.checkCrc	uint8_t	Enable ethernet frame CRC checking.
config.generateCrc	uint8_t	Enable ethernet frame CRC generation.
config.interfaceMode	uint8_t	Set interface mode
config.irqError	uint8_t	IRQ number for eTSEC error
config.irqReceive	uint8_t	IRQ number for eTSEC receieve event
config.irqTransmit	uint8_t	IRQ number for eTSEC transmit event
config.logRegisterAccess	uint8_t	Enable logging of register accesses
config.logTraffic	uint8_t	Enable traffic logging

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Name	Type	Description
irqCtrl	temu_IfaceRef/ <unknown>	IRQ controller
mac	*char	Set MAC by string
mdioBus	temu_IfaceRef/ <unknown>	MDIO bus
memAccess	temu_IfaceRef/ <unknown>	Memory access (for DMA).
phy	temu_IfaceRef/ <unknown>	PHY device
state.GracefulTransmitStopDone	uint8_t	Graceful transmit-stop completed flag

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	Device Interface
MACIface	temu::MACIface	MAC interface
MemAccessIface	MemAccessIface	Mem access interface
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	Reset Interface

Commands

Name	Description
delete	Dispose instance of eTSEC
sendFrame	Send frame
setMAC	Set MAC address

Command sendFrame Arguments

Name	Type	Required	Description
mac	string	yes	MAC address of target

Command setMAC Arguments

Name	Type	Required	Description
mac	string	yes	MAC address to set

10.7.5. Limitations

- Multicast groups are not yet supported.

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10.8. GPIO

This section describes the P2020 GPIO device.

GPIO model simulates a 16 pin GPIO device by providing input and output via the SignalIface. Each signal can be set individually to act as input or output, according to application needs. All input ports can optionally generate an interrupt upon changing their state.

10.8.1. Loading the Plugin

```
import P2020
```

10.8.2. Configuration

Any device that implements SignalIface can be connected to GPIO and send signals via this interface to GPIO or receive them. GPIO implements 16 usable signals (signal 0 through 15). You can connect the signal interface as follows:

Listing 44. Connecting via Command Line

```
# Connect GPIO device signal 0 to device model
connect a=gpio.outSignals[0] b=mydevice:SignalIface

# Connect a device signal interface ref to GPIO device
connect a=mydevice.signal b=gpio:SignalIface[1]
```

Listing 45. Connecting via API

```
// Connect GPIO device signal 0 to device model
temu_connect(gpio, "outSignals[0]", mydevice, "SignalIface");

// Connect a device signal interface ref to GPIO device
temu_connect(mydevice, "signal", gpio, "SignalIface[1]");
```

The GPIO programmable registers that occupy memory-mapped space are named according to P2020 QorIQ integrated processor reference manual. You can set resgisters value as follows:

Listing 46. Setting registers via Command Line

```
# Set signal_0 as an output
gpio.GPDIR = 0x80000000;
```

Listing 47. Setting registers via API

```
// Set signal_0 as an output
```

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```
temu_writeValueU32(gpio, "GPDIR", 0x80000000, 0);
```

10.8.3. @GPIO Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GPIO
new	Create new instance of GPIO

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

10.8.4. GPIO Reference

Properties

Name	Type	Description
Class	*void	Class object

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Name	Type	Description
Component	*void	Pointer to component object if part of component
GPDAT	uint32_t	GPIO data register
GPDATColdResetValue	uint32_t	GPIO data register
GPDATForcedBits	uint32_t	GPIO data register
GPDATForcedFlippedBits	uint32_t	GPIO data register
GPDATReadMask	uint32_t	GPIO data register
GPDATResetMask	uint32_t	GPIO data register
GPDATResetValue	uint32_t	GPIO data register
GPDATWriteMask	uint32_t	GPIO data register
GPDIR	uint32_t	GPIO direction register
GPDIRColdResetValue	uint32_t	GPIO direction register
GPDIRForcedBits	uint32_t	GPIO direction register
GPDIRForcedFlippedBits	uint32_t	GPIO direction register
GPDIRReadMask	uint32_t	GPIO direction register
GPDIRResetMask	uint32_t	GPIO direction register
GPDIRResetValue	uint32_t	GPIO direction register
GPDIRWriteMask	uint32_t	GPIO direction register
GPICR	uint32_t	GPIO external interrupt control register
GPICRColdResetValue	uint32_t	GPIO external interrupt control register
GPICRForcedBits	uint32_t	GPIO external interrupt control register
GPICRForcedFlippedBits	uint32_t	GPIO external interrupt control register
GPICRReadMask	uint32_t	GPIO external interrupt control register
GPICRResetMask	uint32_t	GPIO external interrupt control register
GPICRResetValue	uint32_t	GPIO external interrupt control register
GPICRWriteMask	uint32_t	GPIO external interrupt control register

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Name	Type	Description
GPIER	uint32_t	GPIO interrupt event register
GPIERColdResetValue	uint32_t	GPIO interrupt event register
GPIERForcedBits	uint32_t	GPIO interrupt event register
GPIERForcedFlippedBits	uint32_t	GPIO interrupt event register
GPIERReadMask	uint32_t	GPIO interrupt event register
GPIERResetMask	uint32_t	GPIO interrupt event register
GPIERResetValue	uint32_t	GPIO interrupt event register
GPIERWriteMask	uint32_t	GPIO interrupt event register
GPIMR	uint32_t	GPIO interrupt mask register
GPIMRColdResetValue	uint32_t	GPIO interrupt mask register
GPIMRForcedBits	uint32_t	GPIO interrupt mask register
GPIMRForcedFlippedBits	uint32_t	GPIO interrupt mask register
GPIMRReadMask	uint32_t	GPIO interrupt mask register
GPIMRResetMask	uint32_t	GPIO interrupt mask register
GPIMRResetValue	uint32_t	GPIO interrupt mask register
GPIMRWriteMask	uint32_t	GPIO interrupt mask register
GPODR	uint32_t	GPIO open drain register
GPODRColdResetValue	uint32_t	GPIO open drain register
GPODRForcedBits	uint32_t	GPIO open drain register
GPODRForcedFlippedBits	uint32_t	GPIO open drain register
GPODRReadMask	uint32_t	GPIO open drain register
GPODRResetMask	uint32_t	GPIO open drain register
GPODRResetValue	uint32_t	GPIO open drain register
GPODRWriteMask	uint32_t	GPIO open drain register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
TimeSource	*void	Time source object
inputData	uint16_t	Input data register.
irqCtrl	temu_IfaceRef/ <unknown>	
outSignals	[temu_IfaceRef; 16]/ <unknown>	
outputData	uint16_t	Output data register.
pinLevel	uint32_t	Level sampled on the input pins (internal state, MSB-0 bit order). GPDAT reads return this for input pins.

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	
SignalIface	SignalIface	Incomming signals

Commands

Name	Description
delete	Dispose instance of GPIO

10.8.5. Limitations

- Open-drain capability is not supported, GPODR is a dummy register.

10.9. GUTS

This section describes the P2020 Global Utilities (GUTS) model.

10.9.1. Loading the Plugin

```
import P2020
```

10.9.2. Configuration

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

10.9.3. @GUTS Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @GUTS
new	Create new instance of GUTS

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

10.9.4. GUTS Reference

Properties

Name	Type	Description
AUTORSTSRColdResetValue	uint32_t	Automatic reset status register
AUTORSTSRForcedBits	uint32_t	Automatic reset status register
AUTORSTSRForcedFlippedBits	uint32_t	Automatic reset status register
AUTORSTSRReadMask	uint32_t	Automatic reset status register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
AUTORSTSRResetMask	uint32_t	Automatic reset status register
AUTORSTSRResetValue	uint32_t	Automatic reset status register
AUTORSTSRWriteMask	uint32_t	Automatic reset status register
AUTOSRTSR	uint32_t	Automatic reset status register
CLKOCR	uint32_t	Clock out control register
CLKOCRColdResetValue	uint32_t	Clock out control register
CLKOCRForcedBits	uint32_t	Clock out control register
CLKOCRForcedFlippedBits	uint32_t	Clock out control register
CLKOCRReadMask	uint32_t	Clock out control register
CLKOCRResetMask	uint32_t	Clock out control register
CLKOCRResetValue	uint32_t	Clock out control register
CLKOCRWriteMask	uint32_t	Clock out control register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
DDRCLKDR	uint32_t	DDR clock disable register
DDRCLKDRColdResetValue	uint32_t	DDR clock disable register
DDRCLKDRForcedBits	uint32_t	DDR clock disable register
DDRCLKDRForcedFlippedBits	uint32_t	DDR clock disable register
DDRCLKDRReadMask	uint32_t	DDR clock disable register
DDRCLKDRResetMask	uint32_t	DDR clock disable register
DDRCLKDRResetValue	uint32_t	DDR clock disable register
DDRCLKDRWriteMask	uint32_t	DDR clock disable register
DEVDISR	uint32_t	Device disable control register
DEVDISRColdResetValue	uint32_t	Device disable control register
DEVDISRForcedBits	uint32_t	Device disable control register
DEVDISRForcedFlippedBits	uint32_t	Device disable control register
DEVDISRReadMask	uint32_t	Device disable control register
DEVDISRResetMask	uint32_t	Device disable control register
DEVDISRResetValue	uint32_t	Device disable control register
DEVDISRWriteMask	uint32_t	Device disable control register
ECMCR	uint32_t	ECM control register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
ECMCRColdResetValue	uint32_t	ECM control register
ECMCRForcedBits	uint32_t	ECM control register
ECMCRForcedFlippedBits	uint32_t	ECM control register
ECMCRReadMask	uint32_t	ECM control register
ECMCRResetMask	uint32_t	ECM control register
ECMCRResetValue	uint32_t	ECM control register
ECMCRWriteMask	uint32_t	ECM control register
ECTRSTCR	uint32_t	Exception reset control register
ECTRSTCRColdResetValue	uint32_t	Exception reset control register
ECTRSTCRForcedBits	uint32_t	Exception reset control register
ECTRSTCRForcedFlippedBits	uint32_t	Exception reset control register
ECTRSTCRReadMask	uint32_t	Exception reset control register
ECTRSTCRResetMask	uint32_t	Exception reset control register
ECTRSTCRResetValue	uint32_t	Exception reset control register
ECTRSTCRWriteMask	uint32_t	Exception reset control register
GPPORCRColdResetValue	uint32_t	General-purpose POR configuration register
GPPORCRForcedBits	uint32_t	General-purpose POR configuration register
GPPORCRForcedFlippedBits	uint32_t	General-purpose POR configuration register
GPPORCRReadMask	uint32_t	General-purpose POR configuration register
GPPORCRResetMask	uint32_t	General-purpose POR configuration register
GPPORCRResetValue	uint32_t	General-purpose POR configuration register
GPPORCRWriteMask	uint32_t	General-purpose POR configuration register
IOVSELSR	uint32_t	IO voltage select status register
IOVSELSRColdResetValue	uint32_t	IO voltage select status register
IOVSELSRForcedBits	uint32_t	IO voltage select status register
IOVSELSRForcedFlippedBits	uint32_t	IO voltage select status register
IOVSELSRReadMask	uint32_t	IO voltage select status register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
IOVSELSRResetMask	uint32_t	IO voltage select status register
IOVSELSRResetValue	uint32_t	IO voltage select status register
IOVSELSRWriteMask	uint32_t	IO voltage select status register
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
MCPSUMR	uint32_t	Machine check summary register
MCPSUMRColdResetValue	uint32_t	Machine check summary register
MCPSUMRForcedBits	uint32_t	Machine check summary register
MCPSUMRForcedFlippedBits	uint32_t	Machine check summary register
MCPSUMRReadMask	uint32_t	Machine check summary register
MCPSUMRResetMask	uint32_t	Machine check summary register
MCPSUMRResetValue	uint32_t	Machine check summary register
MCPSUMRWriteMask	uint32_t	Machine check summary register
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
PMCDR	uint32_t	Power management clock disable register
PMCDRColdResetValue	uint32_t	Power management clock disable register
PMCDRForcedBits	uint32_t	Power management clock disable register
PMCDRForcedFlippedBits	uint32_t	Power management clock disable register
PMCDRReadMask	uint32_t	Power management clock disable register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
PMCDRResetMask	uint32_t	Power management clock disable register
PMCDRResetValue	uint32_t	Power management clock disable register
PMCDRWriteMask	uint32_t	Power management clock disable register
PMUXCR	uint32_t	Alternate function signal multiplex control register
PMUXCRColdResetValue	uint32_t	Alternate function signal multiplex control register
PMUXCRForcedBits	uint32_t	Alternate function signal multiplex control register
PMUXCRForcedFlippedBits	uint32_t	Alternate function signal multiplex control register
PMUXCRReadMask	uint32_t	Alternate function signal multiplex control register
PMUXCRResetMask	uint32_t	Alternate function signal multiplex control register
PMUXCRResetValue	uint32_t	Alternate function signal multiplex control register
PMUXCRWriteMask	uint32_t	Alternate function signal multiplex control register
PORBMSR	uint32_t	POR boot mode status register
PORBMSRColdResetValue	uint32_t	POR boot mode status register
PORBMSRForcedBits	uint32_t	POR boot mode status register
PORBMSRForcedFlippedBits	uint32_t	POR boot mode status register
PORBMSRReadMask	uint32_t	POR boot mode status register
PORBMSRResetMask	uint32_t	POR boot mode status register
PORBMSRResetValue	uint32_t	POR boot mode status register
PORBMSRWriteMask	uint32_t	POR boot mode status register
PORDBGMSR	uint32_t	POR debug mode status register
PORDBGMSRColdResetValue	uint32_t	POR debug mode status register
PORDBGMSRForcedBits	uint32_t	POR debug mode status register
PORDBGMSRForcedFlippedBits	uint32_t	POR debug mode status register
PORDBGMSRReadMask	uint32_t	POR debug mode status register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
PORDBGMSRResetMask	uint32_t	POR debug mode status register
PORDBGMSRResetValue	uint32_t	POR debug mode status register
PORDBGMSRWriteMask	uint32_t	POR debug mode status register
PORDEVSR	uint32_t	POR device status register
PORDEVSR2	uint32_t	POR device status register 2
PORDEVSR2ColdResetValue	uint32_t	POR device status register 2
PORDEVSR2ForcedBits	uint32_t	POR device status register 2
PORDEVSR2ForcedFlippedBits	uint32_t	POR device status register 2
PORDEVSR2ReadMask	uint32_t	POR device status register 2
PORDEVSR2ResetMask	uint32_t	POR device status register 2
PORDEVSR2ResetValue	uint32_t	POR device status register 2
PORDEVSR2WriteMask	uint32_t	POR device status register 2
PORDEVSRColdResetValue	uint32_t	POR device status register
PORDEVSRForcedBits	uint32_t	POR device status register
PORDEVSRForcedFlippedBits	uint32_t	POR device status register
PORDEVSRReadMask	uint32_t	POR device status register
PORDEVSRResetMask	uint32_t	POR device status register
PORDEVSRResetValue	uint32_t	POR device status register
PORDEVSRWriteMask	uint32_t	POR device status register
PORGPPORCR	uint32_t	General-purpose POR configuration register
PORPLLSR	uint32_t	POR PLL ratio status register
PORPLLSRColdResetValue	uint32_t	POR PLL ratio status register
PORPLLSRForcedBits	uint32_t	POR PLL ratio status register
PORPLLSRForcedFlippedBits	uint32_t	POR PLL ratio status register
PORPLLSRReadMask	uint32_t	POR PLL ratio status register
PORPLLSRResetMask	uint32_t	POR PLL ratio status register
PORPLLSRResetValue	uint32_t	POR PLL ratio status register
PORPLLSRWriteMask	uint32_t	POR PLL ratio status register
POWMGTCSR	uint32_t	Power management control and status register
POWMGTCSRColdResetValue	uint32_t	Power management control and status register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
POWMGTCSRForcedBits	uint32_t	Power management control and status register
POWMGTCSRForcedFlippedBits	uint32_t	Power management control and status register
POWMGTCSRReadMask	uint32_t	Power management control and status register
POWMGTCSRResetMask	uint32_t	Power management control and status register
POWMGTCSRResetValue	uint32_t	Power management control and status register
POWMGTCSRWriteMask	uint32_t	Power management control and status register
PVR	uint32_t	Processor version register
PVRColdResetValue	uint32_t	Processor version register
PVRForcedBits	uint32_t	Processor version register
PVRForcedFlippedBits	uint32_t	Processor version register
PVRReadMask	uint32_t	Processor version register
PVRResetMask	uint32_t	Processor version register
PVRResetValue	uint32_t	Processor version register
PVRWriteMask	uint32_t	Processor version register
RSTCR	uint32_t	Reset control register
RSTCRColdResetValue	uint32_t	Reset control register
RSTCRForcedBits	uint32_t	Reset control register
RSTCRForcedFlippedBits	uint32_t	Reset control register
RSTCRReadMask	uint32_t	Reset control register
RSTCRResetMask	uint32_t	Reset control register
RSTCRResetValue	uint32_t	Reset control register
RSTCRWriteMask	uint32_t	Reset control register
RSTRSCR	uint32_t	Reset request status and control register
RSTRSCRColdResetValue	uint32_t	Reset request status and control register
RSTRSCRForcedBits	uint32_t	Reset request status and control register

The use and/or disclosure,etc. of the contents of this document (or any part thereof) is subject to the restrictions referenced on the front page.

Name	Type	Description
RSTRSCRForcedFlippedBits	uint32_t	Reset request status and control register
RSTRSCRReadMask	uint32_t	Reset request status and control register
RSTRSCRResetMask	uint32_t	Reset request status and control register
RSTRSCRResetValue	uint32_t	Reset request status and control register
RSTRSCRWriteMask	uint32_t	Reset request status and control register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
SDHCDCR	uint32_t	SDHC debug control register
SDHCDCRColdResetValue	uint32_t	SDHC debug control register
SDHCDCRForcedBits	uint32_t	SDHC debug control register
SDHCDCRForcedFlippedBits	uint32_t	SDHC debug control register
SDHCDCRReadMask	uint32_t	SDHC debug control register
SDHCDCRResetMask	uint32_t	SDHC debug control register
SDHCDCRResetValue	uint32_t	SDHC debug control register
SDHCDCRWriteMask	uint32_t	SDHC debug control register
SRDSCR0	uint32_t	SRDS control register 0
SRDSCR0ColdResetValue	uint32_t	SRDS control register 0
SRDSCR0ForcedBits	uint32_t	SRDS control register 0
SRDSCR0ForcedFlippedBits	uint32_t	SRDS control register 0
SRDSCR0ReadMask	uint32_t	SRDS control register 0
SRDSCR0ResetMask	uint32_t	SRDS control register 0
SRDSCR0ResetValue	uint32_t	SRDS control register 0
SRDSCR0WriteMask	uint32_t	SRDS control register 0
SRDSCR1	uint32_t	SRDS control register 1
SRDSCR1ColdResetValue	uint32_t	SRDS control register 1
SRDSCR1ForcedBits	uint32_t	SRDS control register 1
SRDSCR1ForcedFlippedBits	uint32_t	SRDS control register 1
SRDSCR1ReadMask	uint32_t	SRDS control register 1
SRDSCR1ResetMask	uint32_t	SRDS control register 1

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Name	Type	Description
SRDSCR1ResetValue	uint32_t	SRDS control register 1
SRDSCR1WriteMask	uint32_t	SRDS control register 1
SRDSCR2	uint32_t	SRDS control register 2
SRDSCR2ColdResetValue	uint32_t	SRDS control register 2
SRDSCR2ForcedBits	uint32_t	SRDS control register 2
SRDSCR2ForcedFlippedBits	uint32_t	SRDS control register 2
SRDSCR2ReadMask	uint32_t	SRDS control register 2
SRDSCR2ResetMask	uint32_t	SRDS control register 2
SRDSCR2ResetValue	uint32_t	SRDS control register 2
SRDSCR2WriteMask	uint32_t	SRDS control register 2
SRDSCR4	uint32_t	SRDS control register 4
SRDSCR4ColdResetValue	uint32_t	SRDS control register 4
SRDSCR4ForcedBits	uint32_t	SRDS control register 4
SRDSCR4ForcedFlippedBits	uint32_t	SRDS control register 4
SRDSCR4ReadMask	uint32_t	SRDS control register 4
SRDSCR4ResetMask	uint32_t	SRDS control register 4
SRDSCR4ResetValue	uint32_t	SRDS control register 4
SRDSCR4WriteMask	uint32_t	SRDS control register 4
SRDSCR5	uint32_t	SRDS control register 5
SRDSCR5ColdResetValue	uint32_t	SRDS control register 5
SRDSCR5ForcedBits	uint32_t	SRDS control register 5
SRDSCR5ForcedFlippedBits	uint32_t	SRDS control register 5
SRDSCR5ReadMask	uint32_t	SRDS control register 5
SRDSCR5ResetMask	uint32_t	SRDS control register 5
SRDSCR5ResetValue	uint32_t	SRDS control register 5
SRDSCR5WriteMask	uint32_t	SRDS control register 5
SRDSCR6	uint32_t	SRDS control register 6
SRDSCR6ColdResetValue	uint32_t	SRDS control register 6
SRDSCR6ForcedBits	uint32_t	SRDS control register 6
SRDSCR6ForcedFlippedBits	uint32_t	SRDS control register 6
SRDSCR6ReadMask	uint32_t	SRDS control register 6
SRDSCR6ResetMask	uint32_t	SRDS control register 6

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Name	Type	Description
SRDSCR6ResetValue	uint32_t	SRDS control register 6
SRDSCR6WriteMask	uint32_t	SRDS control register 6
SVR	uint32_t	System version register
SVRColdResetValue	uint32_t	System version register
SVRForcedBits	uint32_t	System version register
SVRForcedFlippedBits	uint32_t	System version register
SVRReadMask	uint32_t	System version register
SVRResetMask	uint32_t	System version register
SVRResetValue	uint32_t	System version register
SVRWriteMask	uint32_t	System version register
TimeSource	*void	Time source object
resetTarget	temu_IfaceRef/ <unknown>	Reset target

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	Device Interface
MemAccessIface	MemAccessIface	Memory access interface
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	Reset Interface

Commands

Name	Description
delete	Dispose instance of GUTS

10.9.5. Limitations

10.10. PCIe

This section describes the P2020 PCIe controller model.

The PCI Express controller can function as either a root complex (RC) or an endpoint (EP) on the PCI Express link.

The PCI Express interface supports the following register types:

- Memory-mapped registers-these registers control PCI Express address translation, PCI error

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management, PCI Express configuration register access.

- PCI Express configuration registers contained within the PCI Express configuration space-these registers are specified by the PCI Express specification for every PCIExpress device.

PCIe Bus contains information about connected to it EP-devices and PCIe bridge (RC device). There are two configuration header types applicable to PCI Express. Type 0 headers are typically used by endpoints, Type 1 headers are used by root complexes and switches/bridges.

10.10.1. Loading the Plugin

```
import P2020
```

10.10.2. Configuration

Every RC or EP device should be connected to a bus PCIe devices array via PCIDevIface interface, buses should be connected via PCIeBusIface to PCIe model. All buses (exept the main upstream bus0) should have a pcie bridge as a parent device. Each PCIe device, including bridges, should point to the primary bus it is connected to, bridges should also point to the secondary bus immediately downstream of the bridge.

Listing 48. Setting PCIe buses and devices via API

```
// connect devices to buses
temu_connect(upstreamBus, "pcieDevices", pciebridge, "PCIDevIface");
temu_connect(downstreamBus, "pcieDevices", pciedev, "PCIDevIface");

// connect buses to the pcie model
temu_connect(pcie, "pcieBuses", upstreamBus, "PCIeBusIface");
temu_connect(pcie, "pcieBuses", downstreamBus, "PCIeBusIface");

// add upstream bridge to the bus model
temu_writeValue(downstreamBus, "parentBridge", temu_makePropObj(pciebridge), 0);

// set primary & secondary buses for devices
temu_writeValue(pciedev, "primaryBus", temu_makePropObj(downstreamBus), 0);
temu_writeValue(pciebridge, "primaryBus", temu_makePropObj(upstreamBus), 0);
temu_writeValue(pciebridge, "secondaryBus", temu_makePropObj(downstreamBus), 0);
```

Listing 49. Setting PCIe buses and devices via Command Line

```
# connect devices to buses
connect a=upstreamBus.pcieDevices b=pciebridge:PCIDevIface
connect a=downstreamBus.pcieDevices b=pciedev:PCIDevIface

# connect buses to the pcie model
connect a=pcie.pcieBuses b=upstreamBus:PCIeBusIface
```

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```
connect a=pcie.pcieBuses b=downstreamBus:PCIeBusIface

# add upstream bridge to the bus model
downbus.parentBridge = pciebridge

# set primary & secondary buses for devices
pciedev.primaryBus = downstreamBus
pciebridge.primaryBus = upstreamBus
pciebridge.secondaryBus = downstreamBus
```

The PCIe programmable registers that occupy memory-mapped space are named according to P2020 QorIQ integrated processor reference manual. All the PCIe registers are 4-byte wide.

Listing 50. Setting registers via API

```
// Write Status & Command Register register from Configuration Space (device 0, bus 0,
offset = 4) via CONFIG_ADDR/CONFIG_DATA registers
temu_writeValueU32(pcie, "PEX_CONFIG_ADDR", 0x80000004, 0);
temu_writeValueU32(pcie, "PEX_CONFIG_DATA", 0x02000000, 0);
// Value = 0x00000002 will be written to pcieConfigStatusCommand of the device0
```

Listing 51. Setting registers via Command Line

```
# Write Status & Command Register register from Configuration Space (device 0, bus 0,
offset = 4) via CONFIG_ADDR/CONFIG_DATA registers
pcie.PEX_CONFIG_ADDR = 0x80000004
pcie.PEX_CONFIG_DATA = 0x02000000
# Value = 0x00000002 will be written to pcieConfigStatusCommand of the device0
```

10.10.3. @PCIe Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name

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Name	Type	Description
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @PCIe
new	Create new instance of PCIe

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

10.10.4. PCIe Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
PEXITAR	[uint32_t; 3]	PCI Express inbound translation address register
PEXIWAR	[uint32_t; 3]	PCI Express inbound window attributes register
PEXIWBAR	[uint32_t; 3]	PCI Express inbound window base address register

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Name	Type	Description
PEXIWBEAR	[uint32_t; 3]	PCI Express inbound window base extended address register
PEXOTAR	[uint32_t; 5]	PCI Express outbound translation address register
PEXOTEAR	[uint32_t; 5]	PCI Express outbound translation extended address register
PEXOWAR	[uint32_t; 5]	PCI Express outbound window attributes register
PEXOWBAR	[uint32_t; 5]	PCI Express outbound window base address register
PEX_CONFIG	uint32_t	PCI Express configuration register
PEX_CONFIGColdResetValue	uint32_t	PCI Express configuration register
PEX_CONFIGForcedBits	uint32_t	PCI Express configuration register
PEX_CONFIGForcedFlippedBits	uint32_t	PCI Express configuration register
PEX_CONFIGReadMask	uint32_t	PCI Express configuration register
PEX_CONFIGResetMask	uint32_t	PCI Express configuration register
PEX_CONFIGResetValue	uint32_t	PCI Express configuration register
PEX_CONFIGWriteMask	uint32_t	PCI Express configuration register
PEX_CONFIG_ADDR	uint32_t	PCI Express configuration address register
PEX_CONFIG_ADDRColdResetValue	uint32_t	PCI Express configuration address register
PEX_CONFIG_ADDRForcedBits	uint32_t	PCI Express configuration address register
PEX_CONFIG_ADDRForcedFlippedBits	uint32_t	PCI Express configuration address register
PEX_CONFIG_ADDRReadMask	uint32_t	PCI Express configuration address register

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Name	Type	Description
PEX_CONFIG_ADDRResetMask	uint32_t	PCI Express configuration address register
PEX_CONFIG_ADDRResetValue	uint32_t	PCI Express configuration address register
PEX_CONFIG_ADDRWriteMask	uint32_t	PCI Express configuration address register
PEX_CONFIG_DATA	uint32_t	PCI Express configuration data register
PEX_CONFIG_DATAColdResetValue	uint32_t	PCI Express configuration data register
PEX_CONFIG_DATAForcedBits	uint32_t	PCI Express configuration data register
PEX_CONFIG_DATAForcedFlippedBits	uint32_t	PCI Express configuration data register
PEX_CONFIG_DATAReadMask	uint32_t	PCI Express configuration data register
PEX_CONFIG_DATAResetMask	uint32_t	PCI Express configuration data register
PEX_CONFIG_DATAResetValue	uint32_t	PCI Express configuration data register
PEX_CONFIG_DATAWriteMask	uint32_t	PCI Express configuration data register
PEX_CONF_RTY_TOR	uint32_t	PCI Express configuration retry timeout register
PEX_CONF_RTY_TORColdResetValue	uint32_t	PCI Express configuration retry timeout register
PEX_CONF_RTY_TORForcedBits	uint32_t	PCI Express configuration retry timeout register
PEX_CONF_RTY_TORForcedFlippedBits	uint32_t	PCI Express configuration retry timeout register
PEX_CONF_RTY_TORReadMask	uint32_t	PCI Express configuration retry timeout register
PEX_CONF_RTY_TORResetMask	uint32_t	PCI Express configuration retry timeout register
PEX_CONF_RTY_TORResetValue	uint32_t	PCI Express configuration retry timeout register

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Name	Type	Description
PEX_CONF_RTY_TORWriteMask	uint32_t	PCI Express configuration retry timeout register
PEX_ERR_CAP	[uint32_t; 4]	PCI Express error capture register
PEX_ERR_CAP_STAT	uint32_t	PCI Express error capture status register
PEX_ERR_CAP_STATColdResetValue	uint32_t	PCI Express error capture status register
PEX_ERR_CAP_STATForcedBits	uint32_t	PCI Express error capture status register
PEX_ERR_CAP_STATForcedFlippedBits	uint32_t	PCI Express error capture status register
PEX_ERR_CAP_STATReadMask	uint32_t	PCI Express error capture status register
PEX_ERR_CAP_STATResetMask	uint32_t	PCI Express error capture status register
PEX_ERR_CAP_STATResetValue	uint32_t	PCI Express error capture status register
PEX_ERR_CAP_STATWriteMask	uint32_t	PCI Express error capture status register
PEX_ERR_DISR	uint32_t	PCI Express error disable register
PEX_ERR_DISRColdResetValue	uint32_t	PCI Express error disable register
PEX_ERR_DISRForcedBits	uint32_t	PCI Express error disable register
PEX_ERR_DISRForcedFlippedBits	uint32_t	PCI Express error disable register
PEX_ERR_DISRReadMask	uint32_t	PCI Express error disable register
PEX_ERR_DISRResetMask	uint32_t	PCI Express error disable register
PEX_ERR_DISRResetValue	uint32_t	PCI Express error disable register
PEX_ERR_DISRWriteMask	uint32_t	PCI Express error disable register

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Name	Type	Description
PEX_ERR_DR	uint32_t	PCI Express error detect register
PEX_ERR_DRColdResetValue	uint32_t	PCI Express error detect register
PEX_ERR_DRForcedBits	uint32_t	PCI Express error detect register
PEX_ERR_DRForcedFlippedBits	uint32_t	PCI Express error detect register
PEX_ERR_DRReadMask	uint32_t	PCI Express error detect register
PEX_ERR_DRResetMask	uint32_t	PCI Express error detect register
PEX_ERR_DRResetValue	uint32_t	PCI Express error detect register
PEX_ERR_DRWriteMask	uint32_t	PCI Express error detect register
PEX_ERR_EN	uint32_t	PCI Express error interrupt enable register
PEX_ERR_ENColdResetValue	uint32_t	PCI Express error interrupt enable register
PEX_ERR_ENForcedBits	uint32_t	PCI Express error interrupt enable register
PEX_ERR_ENForcedFlippedBits	uint32_t	PCI Express error interrupt enable register
PEX_ERR_ENReadMask	uint32_t	PCI Express error interrupt enable register
PEX_ERR_ENResetMask	uint32_t	PCI Express error interrupt enable register
PEX_ERR_ENResetValue	uint32_t	PCI Express error interrupt enable register
PEX_ERR_ENWriteMask	uint32_t	PCI Express error interrupt enable register
PEX_IP_BLK_REV	[uint32_t; 2]	IP block revision register 1
PEX_OTB_CPL_TOR	uint32_t	PCI Express outbound completion timeout register
PEX_OTB_CPL_TORColdResetValue	uint32_t	PCI Express outbound completion timeout register

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Name	Type	Description
PEX_OTB_CPL_TORForcedBits	uint32_t	PCI Express outbound completion timeout register
PEX_OTB_CPL_TORForcedFlippedBits	uint32_t	PCI Express outbound completion timeout register
PEX_OTB_CPL_TORReadMask	uint32_t	PCI Express outbound completion timeout register
PEX_OTB_CPL_TORResetMask	uint32_t	PCI Express outbound completion timeout register
PEX_OTB_CPL_TORResetValue	uint32_t	PCI Express outbound completion timeout register
PEX_OTB_CPL_TORWriteMask	uint32_t	PCI Express outbound completion timeout register
PEX_PMCR	uint32_t	PCI Express power management command register
PEX_PMCRColdResetValue	uint32_t	PCI Express power management command register
PEX_PMCRForcedBits	uint32_t	PCI Express power management command register
PEX_PMCRForcedFlippedBits	uint32_t	PCI Express power management command register
PEX_PMCRReadMask	uint32_t	PCI Express power management command register
PEX_PMCRResetMask	uint32_t	PCI Express power management command register
PEX_PMCRResetValue	uint32_t	PCI Express power management command register
PEX_PMCRWriteMask	uint32_t	PCI Express power management command register
PEX_PME_MES_DISR	uint32_t	PCI Express PME and message disable register
PEX_PME_MES_DISRColdResetValue	uint32_t	PCI Express PME and message disable register
PEX_PME_MES_DISRForcedBits	uint32_t	PCI Express PME and message disable register
PEX_PME_MES_DISRForcedFlippedBits	uint32_t	PCI Express PME and message disable register

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Name	Type	Description
PEX_PME_MES_DISRReadMask	uint32_t	PCI Express PME and message disable register
PEX_PME_MES_DISRResetMask	uint32_t	PCI Express PME and message disable register
PEX_PME_MES_DISRResetValue	uint32_t	PCI Express PME and message disable register
PEX_PME_MES_DISRWriteMask	uint32_t	PCI Express PME and message disable register
PEX_PME_MES_DR	uint32_t	PCI Express PME and message detect register
PEX_PME_MES_DRColdResetValue	uint32_t	PCI Express PME and message detect register
PEX_PME_MES_DRForcedBits	uint32_t	PCI Express PME and message detect register
PEX_PME_MES_DRForcedFlippedBits	uint32_t	PCI Express PME and message detect register
PEX_PME_MES_DRReadMask	uint32_t	PCI Express PME and message detect register
PEX_PME_MES_DRResetMask	uint32_t	PCI Express PME and message detect register
PEX_PME_MES_DRResetValue	uint32_t	PCI Express PME and message detect register
PEX_PME_MES_DRWriteMask	uint32_t	PCI Express PME and message detect register
PEX_PME_MES_IER	uint32_t	PCI Express PME and message interrupt enable register
PEX_PME_MES_IERColdResetValue	uint32_t	PCI Express PME and message interrupt enable register
PEX_PME_MES_IERForcedBits	uint32_t	PCI Express PME and message interrupt enable register
PEX_PME_MES_IERForcedFlippedBits	uint32_t	PCI Express PME and message interrupt enable register
PEX_PME_MES_IERReadMask	uint32_t	PCI Express PME and message interrupt enable register
PEX_PME_MES_IERResetMask	uint32_t	PCI Express PME and message interrupt enable register

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Name	Type	Description
PEX_PME_MES_IERResetValue	uint32_t	PCI Express PME and message interrupt enable register
PEX_PME_MES_IERWriteMask	uint32_t	PCI Express PME and message interrupt enable register
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
config.externalInterrupt	uint8_t	External interrupt (used as base by legacy PCI interrupts)
config.internalInterrupt	uint8_t	Internal interrupt
config.machineCheckOnFailedTransaction	uint8_t	Raise a Machine Check Exception (MCE) on CPUs if outbound transactions fail.
config.mmioAtc	uint8_t	Let CPUs cache routes past the controller to the devices behind its outbound memory and I/O windows (MMIO ATC). Routed accesses skip the controller’s trace logging.
configSpace	[uint32_t; 1024]	Raw configuration space access
deviceIOAccess	temu_IfaceRef/ <unknown>	Access to the pcie’s io space from inbound windows
deviceMemAccess	temu_IfaceRef/ <unknown>	Access to the pcie’s memory space from inbound windows
extIrqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller (external interface)
ioMem	temu_IfaceRef/ <unknown>	PCIe i/o space object
irqCtrl	temu_IfaceRef/ <unknown>	Interrupt controller (internal interface)
isEPMode	uint8_t	
pciBridge	*void	PCIe rc bridge
pciMem	temu_IfaceRef/ <unknown>	PCIe memory space object
pcieBuses	temu_IfaceRefArray	PCI busses
processorMem	temu_IfaceRef/ <unknown>	Access to the processor’s memory space from inbound windows

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Interfaces

Name	Type	Description
DeviceIface	DeviceIface	Device Interface
InboundAccessIface	MemAccessIface	PCIe inbound access interfaceinterface.
IrqIface	IrqCtrlIface	PCI IRQ interface
MMIORouteBridgeIface	temu::MMIORouteBridgeIface	Routes past the controller (internal).
MemAccessIface	MemAccessIface	Memory access interface (registers)
OutboundMemAccessIface	MemAccessIface	PCIe outbound memory access interface.
PCIDevIface	temu::PCIDeviceIface	PCIe device interface
PCIExpressBridgeIface	temu::PCIExpressBridgeIface	PCIe bridge interface.
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	Reset Interface
WindowsAccessIface	MemAccessIface	PCIe windows and configuration access interface.

Commands

Name	Description
delete	Dispose instance of PCIe
inject-inbound	Send inbound transaction of 32 bit

Command inject-inbound Arguments

Name	Type	Required	Description
addr	int	yes	Address to unmap.
value	int	yes	Value to inject.

10.10.5. Limitations

- Target interface for inbound windows can be set to local memory space only, Serial Rapid IO is not implemented.

10.11. PIC

This section describes the P2020 Programmable Interrupt Controller.

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PIC implements two types of programmable interrupt outputs: critical interrupts (cint) and non-critical interrupts (int). Support for the following interrupt types:

- External — Off-chip signals (12 interrupts);
- Internal - On-chip sources from peripheral logic (64 interrupts);
- Global timers A (4 interrupts) and B (4 interrupts) internal to the PIC;
- Interprocessor interrupts (4 interrupts);
- Message registers, used for interprocessor communication (8 interrupts);
- Shared message signaled registers, used for cross-program communication (8 interrupts).

PIC has support for two processors, all interrups can be routed to processor core 0 or 1. Multi-cast delivery mode for interprocessor and global timer interrupts allowing these interrupts to be routed to either core 0 or 1, or both cores.

Each interrupt source routed to int is assigned a priority value (range from 0x00 to 0x0f. Therefore, setting int priority to zero inhibits that interrupt. Likewise, setting CTPR[TASKP] (task priority threshold) to 0x0f prevents the PIC from delivering interrupts to that core through the int signal. Note that this is the reset TASKP value, preventing the PIC from asserting int before the PIC is configured.

10.11.1. Loading the Plugin

```
import P2020
```

10.11.2. Configuration

config.nCpu

Number of processors supported (1 or 2).

config.CCBFrequency

CCB frequency in MHz (dafault 333 MHz), used for timer frequency reporting calculation.

config.RTCFrequency

RTC frequency in MHz (dafault 64 MHz), used for timer frequency reporting calculation.

config.logInterrupts

Additional logs with raised interrupts information.

The PIC programmable registers that occupy memory-mapped space are named according to P2020 QorIQ integrated processor reference manual. You can set resgisters value as follows:

Listing 52. Setting registers via Command Line

```
# Set mixed mode On. Interrupts are handled by the normal priority and delivery
```

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```
mechanisms of the PIC.
pic.GCR = 0x20000000

# Set min task priority = 1 (max = 0x0f) for processor core 0, interrupt priority must
exceed this value for the interrupt request to be serviced
pic.CTPR[0]=0x00000001

# Allow interrupts from DUART (default internal interrupt number for DUART is 26), set
its priority to max value = 0x0f
pic.IIVPR[26]=0x000F0000

# Mark DUART interrupts as non-critical(int) and set processor core 1 as a recipient
pic.IIDR[26]=0x00000001

# Mark DUART interrupts as critical(cint) and set processor core 1 as a recipient
pic.IIDR[26]=0x40000000
```

Listing 53. Setting registers via API

```
// Set mixed mode On. Interrupts are handled by the normal priority and delivery
mechanisms of the PIC.
temu_writeValueU32(pic, "GCR", 0x20000000, 0);

// Mark DUART interrupts as critical(cint) and set processor core 1 as a recipient
temu_writeValueU32(pic, "IIDR", 0x40000000, 26);
```

10.11.3. @PIC Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags

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Name	Type	Description
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @PIC
new	Create new instance of PIC

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

10.11.4. PIC Reference

Properties

Name	Type	Description
BRR1	uint32_t	Block revision register 1
BRR1ColdResetValue	uint32_t	Block revision register 1
BRR1ForcedBits	uint32_t	Block revision register 1
BRR1ForcedFlippedBits	uint32_t	Block revision register 1
BRR1ReadMask	uint32_t	Block revision register 1
BRR1ResetMask	uint32_t	Block revision register 1
BRR1ResetValue	uint32_t	Block revision register 1
BRR1WriteMask	uint32_t	Block revision register 1
BRR2	uint32_t	Block revision register 2
BRR2ColdResetValue	uint32_t	Block revision register 2
BRR2ForcedBits	uint32_t	Block revision register 2
BRR2ForcedFlippedBits	uint32_t	Block revision register 2
BRR2ReadMask	uint32_t	Block revision register 2
BRR2ResetMask	uint32_t	Block revision register 2
BRR2ResetValue	uint32_t	Block revision register 2
BRR2WriteMask	uint32_t	Block revision register 2
CISR0	uint32_t	Critical interrupt summary register 0

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Name	Type	Description
CISR0ColdResetValue	uint32_t	Critical interrupt summary register 0
CISR0ForcedBits	uint32_t	Critical interrupt summary register 0
CISR0ForcedFlippedBits	uint32_t	Critical interrupt summary register 0
CISR0ReadMask	uint32_t	Critical interrupt summary register 0
CISR0ResetMask	uint32_t	Critical interrupt summary register 0
CISR0ResetValue	uint32_t	Critical interrupt summary register 0
CISR0WriteMask	uint32_t	Critical interrupt summary register 0
CISR1	uint32_t	Critical interrupt summary register 1
CISR1ColdResetValue	uint32_t	Critical interrupt summary register 1
CISR1ForcedBits	uint32_t	Critical interrupt summary register 1
CISR1ForcedFlippedBits	uint32_t	Critical interrupt summary register 1
CISR1ReadMask	uint32_t	Critical interrupt summary register 1
CISR1ResetMask	uint32_t	Critical interrupt summary register 1
CISR1ResetValue	uint32_t	Critical interrupt summary register 1
CISR1WriteMask	uint32_t	Critical interrupt summary register 1
CISR2	uint32_t	Critical interrupt summary register 2
CISR2ColdResetValue	uint32_t	Critical interrupt summary register 2
CISR2ForcedBits	uint32_t	Critical interrupt summary register 2

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Name	Type	Description
CISR2ForcedFlippedBits	uint32_t	Critical interrupt summary register 2
CISR2ReadMask	uint32_t	Critical interrupt summary register 2
CISR2ResetMask	uint32_t	Critical interrupt summary register 2
CISR2ResetValue	uint32_t	Critical interrupt summary register 2
CISR2WriteMask	uint32_t	Critical interrupt summary register 2
CTPR	uint32_t	Current task priority register
CTPRColdResetValue	uint32_t	Current task priority register
CTPRForcedBits	uint32_t	Current task priority register
CTPRForcedFlippedBits	uint32_t	Current task priority register
CTPRReadMask	uint32_t	Current task priority register
CTPRResetMask	uint32_t	Current task priority register
CTPRResetValue	uint32_t	Current task priority register
CTPRWriteMask	uint32_t	Current task priority register
CTPR_CPU	[uint32_t; 2]	Processor core current task priority register
Class	*void	Class object
Component	*void	Pointer to component object if part of component
EIDR	[uint32_t; 12]	External interrupt destination register
EIVPR	[uint32_t; 12]	External interrupt vector/priority register
EOI	uint32_t	End of interrupt register
EOIColdResetValue	uint32_t	End of interrupt register
EOIForcedBits	uint32_t	End of interrupt register
EOIForcedFlippedBits	uint32_t	End of interrupt register
EOIReadMask	uint32_t	End of interrupt register
EOIResetMask	uint32_t	End of interrupt register
EOIResetValue	uint32_t	End of interrupt register

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Name	Type	Description
EOIWriteMask	uint32_t	End of interrupt register
EOI_CPU	[uint32_t; 2]	Processor core end of interrupt register
ERQSR	uint32_t	External interrupt summary register
ERQSRColdResetValue	uint32_t	External interrupt summary register
ERQSRForcedBits	uint32_t	External interrupt summary register
ERQSRForcedFlippedBits	uint32_t	External interrupt summary register
ERQSRReadMask	uint32_t	External interrupt summary register
ERQSRResetMask	uint32_t	External interrupt summary register
ERQSRResetValue	uint32_t	External interrupt summary register
ERQSRWriteMask	uint32_t	External interrupt summary register
FRR	uint32_t	Feature reporting register
FRRColdResetValue	uint32_t	Feature reporting register
FRRForcedBits	uint32_t	Feature reporting register
FRRForcedFlippedBits	uint32_t	Feature reporting register
FRRReadMask	uint32_t	Feature reporting register
FRRResetMask	uint32_t	Feature reporting register
FRRResetValue	uint32_t	Feature reporting register
FRRWriteMask	uint32_t	Feature reporting register
GCR	uint32_t	Global configuration register
GCRColdResetValue	uint32_t	Global configuration register
GCRForcedBits	uint32_t	Global configuration register
GCRForcedFlippedBits	uint32_t	Global configuration register
GCRReadMask	uint32_t	Global configuration register
GCRResetMask	uint32_t	Global configuration register
GCRResetValue	uint32_t	Global configuration register

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Name	Type	Description
GCRWriteMask	uint32_t	Global configuration register
GTBCR	[uint32_t; 8]	Global timer base count register
GTCCR	[uint32_t; 8]	Global timer current count register
GTDR	[uint32_t; 8]	Global timer destination register
GTVPR	[uint32_t; 8]	Global timer vector/priority register
IACK	uint32_t	Interrupt acknowledge register
IACKColdResetValue	uint32_t	Interrupt acknowledge register
IACKForcedBits	uint32_t	Interrupt acknowledge register
IACKForcedFlippedBits	uint32_t	Interrupt acknowledge register
IACKReadMask	uint32_t	Interrupt acknowledge register
IACKResetMask	uint32_t	Interrupt acknowledge register
IACKResetValue	uint32_t	Interrupt acknowledge register
IACKWriteMask	uint32_t	Interrupt acknowledge register
IACK_CPU	[uint32_t; 2]	Processor core interrupt acknowledge register
IIDR	[uint32_t; 64]	Internal interrupt destination register
IIVPR	[uint32_t; 64]	Internal interrupt vector/priority register
IPIDR	[uint32_t; 4]	Interprocessor interrupt dispatch register
IPIDR_CPU	[uint32_t; 8]	Processor core interprocessor dispatch register
IPIVPR	[uint32_t; 4]	Interprocessor interrupt vector/priority register
IPR	[uint64_t; 4]	Internal IPR registers (128 bit registers split in two parts each)
IRQSR0	uint32_t	IRQ_OUT_B summary register 0
IRQSR0ColdResetValue	uint32_t	IRQ_OUT_B summary register 0
IRQSR0ForcedBits	uint32_t	IRQ_OUT_B summary register 0
IRQSR0ForcedFlippedBits	uint32_t	IRQ_OUT_B summary register 0
IRQSR0ReadMask	uint32_t	IRQ_OUT_B summary register 0

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Name	Type	Description
IRQSR0ResetMask	uint32_t	IRQ_OUT_B summary register 0
IRQSR0ResetValue	uint32_t	IRQ_OUT_B summary register 0
IRQSR0WriteMask	uint32_t	IRQ_OUT_B summary register 0
IRQSR1	uint32_t	IRQ_OUT_B summary register 1
IRQSR1ColdResetValue	uint32_t	IRQ_OUT_B summary register 1
IRQSR1ForcedBits	uint32_t	IRQ_OUT_B summary register 1
IRQSR1ForcedFlippedBits	uint32_t	IRQ_OUT_B summary register 1
IRQSR1ReadMask	uint32_t	IRQ_OUT_B summary register 1
IRQSR1ResetMask	uint32_t	IRQ_OUT_B summary register 1
IRQSR1ResetValue	uint32_t	IRQ_OUT_B summary register 1
IRQSR1WriteMask	uint32_t	IRQ_OUT_B summary register 1
IRQSR2	uint32_t	IRQ_OUT_B summary register 2
IRQSR2ColdResetValue	uint32_t	IRQ_OUT_B summary register 2
IRQSR2ForcedBits	uint32_t	IRQ_OUT_B summary register 2
IRQSR2ForcedFlippedBits	uint32_t	IRQ_OUT_B summary register 2
IRQSR2ReadMask	uint32_t	IRQ_OUT_B summary register 2
IRQSR2ResetMask	uint32_t	IRQ_OUT_B summary register 2
IRQSR2ResetValue	uint32_t	IRQ_OUT_B summary register 2
IRQSR2WriteMask	uint32_t	IRQ_OUT_B summary register 2
IRR	[uint32_t; 2]	Interrupt request register with IRQ number of raised interrupt for each core
ISR	[uint64_t; 4]	Internal IPR registers (128 bit registers split in two parts each)
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
MER	[uint32_t; 2]	Message enable register
MIDR	[uint32_t; 8]	Messaging interrupt destination register
MIVPR	[uint32_t; 8]	Messaging interrupt vector/priority register

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Name	Type	Description
MSGR	[uint32_t; 8]	Message register
MSIDR	[uint32_t; 8]	Shared message signaled interrupt destination register
MSIIR	uint32_t	Shared message signaled interrupt index register
MSIIRColdResetValue	uint32_t	Shared message signaled interrupt index register
MSIIRForcedBits	uint32_t	Shared message signaled interrupt index register
MSIIRForcedFlippedBits	uint32_t	Shared message signaled interrupt index register
MSIIRReadMask	uint32_t	Shared message signaled interrupt index register
MSIIRResetMask	uint32_t	Shared message signaled interrupt index register
MSIIRResetValue	uint32_t	Shared message signaled interrupt index register
MSIIRWriteMask	uint32_t	Shared message signaled interrupt index register
MSIR	[uint32_t; 8]	Shared message signaled interrupt register
MSISR	uint32_t	Shared message signaled interrupt status register
MSISRColdResetValue	uint32_t	Shared message signaled interrupt status register
MSISRForcedBits	uint32_t	Shared message signaled interrupt status register
MSISRForcedFlippedBits	uint32_t	Shared message signaled interrupt status register
MSISRReadMask	uint32_t	Shared message signaled interrupt status register
MSISRResetMask	uint32_t	Shared message signaled interrupt status register
MSISRResetValue	uint32_t	Shared message signaled interrupt status register
MSISRWriteMask	uint32_t	Shared message signaled interrupt status register

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Name	Type	Description
MSIVPR	[uint32_t; 8]	Shared message signaled interrupt vector/priority register
MSR	[uint32_t; 2]	Message status register
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
PIR	uint32_t	Processor core initialization register
PIRColdResetValue	uint32_t	Processor core initialization register
PIRForcedBits	uint32_t	Processor core initialization register
PIRForcedFlippedBits	uint32_t	Processor core initialization register
PIRReadMask	uint32_t	Processor core initialization register
PIRResetMask	uint32_t	Processor core initialization register
PIRResetValue	uint32_t	Processor core initialization register
PIRWriteMask	uint32_t	Processor core initialization register
PMMR0	[uint32_t; 4]	Performance monitor mask register 0
PMMR1	[uint32_t; 4]	Performance monitor mask register 1
PMMR2	[uint32_t; 4]	Performance monitor mask register 2
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
SVR	uint32_t	Spurious vector register
SVRColdResetValue	uint32_t	Spurious vector register
SVRForcedBits	uint32_t	Spurious vector register
SVRForcedFlippedBits	uint32_t	Spurious vector register
SVRReadMask	uint32_t	Spurious vector register
SVRResetMask	uint32_t	Spurious vector register

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Name	Type	Description
SVRResetValue	uint32_t	Spurious vector register
SVRWriteMask	uint32_t	Spurious vector register
TCR	[uint32_t; 2]	Timer control register
TFRR	[uint32_t; 2]	Timer frequency reporting register
TimeSource	*void	Time source object
VIR	uint32_t	Vendor identification register
VIRColdResetValue	uint32_t	Vendor identification register
VIRForcedBits	uint32_t	Vendor identification register
VIRForcedFlippedBits	uint32_t	Vendor identification register
VIRReadMask	uint32_t	Vendor identification register
VIRResetMask	uint32_t	Vendor identification register
VIRResetValue	uint32_t	Vendor identification register
VIRWriteMask	uint32_t	Vendor identification register
WHOAMI	uint32_t	Who am I register
WHOAMIColdResetValue	uint32_t	Who am I register
WHOAMIForcedBits	uint32_t	Who am I register
WHOAMIForcedFlippedBits	uint32_t	Who am I register
WHOAMIReadMask	uint32_t	Who am I register
WHOAMIResetMask	uint32_t	Who am I register
WHOAMIResetValue	uint32_t	Who am I register
WHOAMIWriteMask	uint32_t	Who am I register
WHOAMI_CPU	[uint32_t; 2]	Processor core who am I register
config.CCBFrequency	uint32_t	CCB frequency in MHz
config.RTCFrequency	uint32_t	RTC frequency in MHz
config.logInterrupts	uint8_t	
config.nCpu	uint8_t	
config.traceReads	uint8_t	
config.traceWrites	uint8_t	
cpu	[temu_IfaceRef; 2]/ <unknown>	
currentCrit	uint8_t	

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Name	Type	Description
currentInt	uint8_t	
internal.IDR	[uint32_t; 104]	Internal state (re-syncs Regs mirror on restore)
internal.IVPR	[uint32_t; 104]	Internal state (rebuilds MASK/IRQ_PRIO on restore)
irqCtrl	[temu_IfaceRef; 2]/ <unknown>	
state.TimerStartCycle	[int64_t; 8]	Cycle at which each timer was last (re)scheduled
state.clockDivider	[int32_t; 2]	Cached timer clock divider per group

Interfaces

Name	Type	Description
DeviceIface	DeviceIface	
ExternalIrqIface	IrqCtrlIface	
InternalIrqIface	IrqCtrlIface	
IrqClientIface	IrqClientIface	uptree interrupt handlers (e.g. CPUs)
MemAccessIface	MemAccessIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Ports

Prop	Iface	Description
irqCtrl	IrqClientIface	irq port

Commands

Name	Description
ackIrq	Acknowledge interrupt
delete	Dispose instance of PIC
endOfIrq	End current interrupt
lowerExternalIrq	Lower external interrupt
pstat	Print status

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Name	Description
raiseExternalIrq	Raise external interrupt
raiseInternalIrq	Raise internally interrupt

Command ackIrq Arguments

Name	Type	Required	Description
cpu	int	yes	Processor number

Command endOfIrq Arguments

Name	Type	Required	Description
cpu	int	yes	Processor number

Command lowerExternalIrq Arguments

Name	Type	Required	Description
irq	int	yes	Interrupt number

Command raiseExternalIrq Arguments

Name	Type	Required	Description
irq	int	yes	Interrupt number

Command raiseInternalIrq Arguments

Name	Type	Required	Description
irq	int	yes	Interrupt number

10.11.5. Limitations

- External IRQ_OUT signal is not supported

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Chapter 11. RISC-V Peripherals

11.1. ACLINT

The Aclint device is part of the RISC-V models. It is available in `libTEMUAclint.so`.

11.1.1. Loading the Plugin

```
import Aclint
```

11.1.2. Configuration

11.1.3. @Aclint Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @Aclint
new	Create new instance of Aclint

Command new Arguments

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Name	Type	Required	Description
name	string	yes	Name of object to create

11.1.4. Aclint Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object
config.littleEndian	uint8_t	Endianess of memory interface.
config.logInterrupts	uint8_t	
config.traceEvents	uint8_t	
config.traceReads	uint8_t	
config.traceWrites	uint8_t	
cyclesLastMtimeUpdate	uint64_t	
irqCtrl	[temu_IfaceRef; 8]/ <unknown>	Upstream interrupt controllers (e.g. processor)
msip	[uint32_t; 8]	machine software interrupt pending register
mtime	[uint64_t; 8]	Machine-level time counter
mtimecmp	[uint64_t; 8]	HART index x machine-level time compare
pnp.bar	uint32_t	
pnp.config	uint32_t	

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Interfaces

Name	Type	Description
AclintCsrIface	temu::AclintCsrIface	
ApbIface	ApbIface	
DeviceIface	DeviceIface	
MemAccessIface	MemAccessIface	
ObjectIface	ObjectIface	
RegisterIface	temu::RegisterIface	Auto-generated Register Interface Impl.
ResetIface	ResetIface	

Commands

Name	Description
delete	Dispose instance of Aclint

11.1.5. Limitations

No limitations are documented at this point.

11.2. AIA

The AIA device is part of the RISC-V models. It is available in `libTEMUAIA.so`.

11.2.1. Loading the Plugin

```
import AIA
```

11.2.2. Configuration

11.2.3. @AIA Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)

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Name	Type	Description
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags
TimeSource	*void	Time source object

Commands

Name	Description
delete	Dispose instance of @AIA
new	Create new instance of AIA

Command new Arguments

Name	Type	Required	Description
name	string	yes	Name of object to create

11.2.4. AIA Reference

Properties

Name	Type	Description
Class	*void	Class object
Component	*void	Pointer to component object if part of component
LocalName	*char	Local name (in component, if applicable)
LogMessageFlags	uint64_t	Per-object log message suppression flags
LoggingFlags	uint64_t	Flags for logging info
Name	*char	Object name
ObjectID	uint64_t	Unique ObjectID.
ReplayLoggingFlags	uint64_t	Replay-time category logging flags

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Name	Type	Description
TimeSource	*void	Time source object
config.IMSICHartStride	uint32_t	
config.Trace	uint8_t	
irqCtrl	[temu_IfaceRef; 8]/ <unknown>	CPUs IrqCtrlIface references

Interfaces

Name	Type	Description
APLICMemAccessIface	MemAccessIface	APLIC Memory access interface.
AiaCsrIface	temu::AiaCsrIface	AIA CSR access interface for the CPUs
ApbIface	ApbIface	APB P&P interface.
DeviceIface	DeviceIface	Device interface.
IMSICMemAccessIface	MemAccessIface	IMSIC Memory access interface.
IrqClientIface	IrqClientIface	Interface for CPUs to ack/re-request interrupts
IrqIface	IrqCtrlIface	Interface for interrupt sources (e.g. UARTs etc)

Ports

Prop	Iface	Description
irqCtrl	IrqClientIface	AIA IrqClientIface <→ CPU IrqCtrlIface port

Commands

Name	Description
delete	Dispose instance of AIA
raiseExternalIrq	Raise a interrupt

Command raiseExternalIrq Arguments

Name	Type	Required	Description
srcidx	int	yes	Interrupt source

11.2.5. Limitations

No limitations are documented at this point.

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