

TEMU ***GRETH Model***

Mattias Holm

Version 1.0, 2020-01-15

Table of Contents

| | |
|------------------------------------|---|
| 1. Introduction | 1 |
| 2. Loading the Plugin | 1 |
| 3. Configuration | 1 |
| 4. Attributes | 1 |
| 4.1. Properties | 1 |
| 4.2. Interfaces | 2 |
| 4.3. Ports | 3 |
| 5. Registers | 3 |
| 5.1. Register Bank registers | 3 |
| 5.1.1. Register ETHCTR | 3 |
| 5.1.2. Register ETHSIS | 4 |
| 5.1.3. Register MACMSB | 4 |
| 5.1.4. Register MACLSB | 4 |
| 5.1.5. Register ETHMDC | 5 |
| 5.1.6. Register ETHTDP | 5 |
| 5.1.7. Register ETHRDP | 5 |
| 6. Limitations | 6 |

1. Introduction

The GRETH model is available in the GrEth plugin. The model needs to be combined with a MDIOBus, PHY and Ethernet model.

The GRETH model implements the behaviour of both **GRETH** and **GRETH_GBITH**.

2. Loading the Plugin

```
import BusModels
import GrEth
object-create class=GRETH name=greth0
object-create class=GenericPHY name=phy0
object-create class=EthernetLink name=eth0
connect a=greth0.phy b=phy0:PHYIface
connect a=greth0.mdioBus b=phy0:MDIOIface
connect a=apbctrl0.slaves b=greth0:ApbIface
object-prop-write prop=greth0.mac value="00:00:00:00:00:01"
connect a=phy0.macDevice b=greth0:MACIface
ethernet-connect link=eth0 device=phy0:PHYIface
```

3. Configuration

The **config.gbitVariant** property can be set to enable **GRETH_GBITH** extensions. The extensions includes:

- Gigabit speed.
- IP header checksum offloading
- TCP checksum offloading
- UDP checksum offloading
- Scatter / gather send lists.

4. Attributes

4.1. Properties

| Name | Type | Description |
|--------|----------|---|
| ETHCTR | uint32_t | Ethernet Control Register |
| ETHMDC | uint32_t | Ethernet MDIO Control and Status Register |

| Name | Type | Description |
|--------------------|------------------------|--|
| ETHRDP | uint32_t | Ethernet Receiver Descriptor Pointer Register |
| ETHSIS | uint32_t | Ethernet Status and Interrupt Source Register |
| ETHTDP | uint32_t | Ethernet Transmitter Descriptor Pointer Register |
| MACLSB | uint32_t | Ethernet MAC Address LSB |
| MACMSB | uint32_t | Ethernet MAC Address MSB |
| config.checkCrc | uint8_t | Enable ethernet frame CRC checking. |
| config.checkIpCrc | uint8_t | Enable IP header CRC checking. |
| config.checkTcpCrc | uint8_t | Enable TCP header CRC checking. |
| config.checkUdpCrc | uint8_t | Enable UDP header CRC checking. |
| config.gbitVariant | uint8_t | Enable GRETH_GBIT behaviour. |
| config.generateCrc | uint8_t | Enable ethernet frame CRC generation. |
| config.irq | uint8_t | IRQ |
| config.logTraffic | uint8_t | Enable traffic logging |
| irqCtrl | iref / IrqCtrlIface | IRQ controller |
| mac | cstring | Set MAC by string |
| mdioBus | iref / temu::MDIOIface | MDIO bus |
| memory | iref / MemoryIface | Memory |
| object.timeSource | object | Time source object (a cpu or machine object) |
| phy | iref / temu::PHYIface | PHY device |

4.2. Interfaces

| Name | Type | Description |
|----------------|----------------|----------------------|
| ApbIface | ApbIface | APB P&P interface |
| DeviceIface | DeviceIface | |
| MACIface | temu::MACIface | MAC interface |
| MemAccessIface | MemAccessIface | Mem access interface |

| Name | Type | Description |
|------------|------------|-------------|
| ResetIface | ResetIface | |

4.3. Ports

| Prop | Iface | Description |
|------|-------|-------------|
| - | - | - |

5. Registers



Register support is currently experimental!

5.1. Register Bank registers

5.1.1. Register ETHCTR

Ethernet Control Register

Cold reset value: 0x0

Warm reset value: 0x0

| Field | Mask | Cold | Warm | Description |
|-------|------------|------|------|-------------------------------|
| EA | 0x80000000 | 0x0 | 0x0 | EDCL available |
| BS | 0x70000000 | 0x0 | 0x0 | EDCL buffer size |
| GA | 0x8000000 | 0x0 | 0x0 | Gigabit MAC |
| MA | 0x4000000 | 0x0 | 0x0 | MDIO interrupts supported |
| MC | 0x2000000 | 0x0 | 0x0 | Multicast supported |
| SP | 0x80 | 0x0 | 0x0 | Speed |
| RS | 0x40 | 0x0 | 0x0 | Reset |
| PM | 0x20 | 0x0 | 0x0 | Open Packet Mode |
| FD | 0x10 | 0x0 | 0x0 | Full Duplex |
| RI | 0x8 | 0x0 | 0x0 | Enable Receiver Interrupts |
| TI | 0x4 | 0x0 | 0x0 | Enable Transmitter Interrupts |

| Field | Mask | Cold | Warm | Description |
|-------|------|------|------|-----------------|
| RE | 0x2 | 0x0 | 0x0 | Receive Enable |
| TE | 0x1 | 0x0 | 0x0 | Transmit Enable |

5.1.2. Register ETHSIS

Ethernet Status and Interrupt Source Register

Cold reset value: 0x0

Warm reset value: 0x0

| Field | Mask | Cold | Warm | Description |
|-------|------|------|------|-----------------------|
| IA | 0x80 | 0x0 | 0x0 | Invalid Address |
| TS | 0x40 | 0x0 | 0x0 | Too Small |
| TA | 0x20 | 0x0 | 0x0 | Transmitter AHB Error |
| RA | 0x10 | 0x0 | 0x0 | Receiver AHB Error |
| TI | 0x8 | 0x0 | 0x0 | Transmitter Interrupt |
| RI | 0x4 | 0x0 | 0x0 | Receiver Interrupt |
| TE | 0x2 | 0x0 | 0x0 | Transmitter Error |
| RE | 0x1 | 0x0 | 0x0 | Receiver Error |

5.1.3. Register MACMSB

Ethernet MAC Address MSB

Cold reset value: 0x0

Warm reset value: 0x0

| Field | Mask | Cold | Warm | Description |
|-------|--------|------|------|----------------|
| MSB | 0xffff | 0x0 | 0x0 | Two MSB of MAC |

5.1.4. Register MACLSB

Ethernet MAC Address LSB

Cold reset value: 0x0

Warm reset value: 0x0

| Field | Mask | Cold | Warm | Description |
|-------|------------|------|------|-----------------|
| LSB | 0xffffffff | 0x0 | 0x0 | Four LSB of MAC |

5.1.5. Register ETHMDC

Ethernet MDIO Control and Status Register

Cold reset value: 0x0

Warm reset value: 0x0

| Field | Mask | Cold | Warm | Description |
|----------|------------|------|------|---------------------------|
| Data | 0xffff0000 | 0x0 | 0x0 | Data for MMI read / write |
| PHY_ADDR | 0xf800 | 0x0 | 0x0 | PHY address |
| REG_ADDR | 0x7c0 | 0x0 | 0x0 | MII reg addr |
| NV | 0x10 | 0x0 | 0x0 | Not valid |
| BU | 0x8 | 0x0 | 0x0 | Busy |
| LF | 0x4 | 0x0 | 0x0 | Link fail |
| RD | 0x2 | 0x0 | 0x0 | Read |
| WR | 0x1 | 0x0 | 0x0 | Write |

5.1.6. Register ETHTDP

Ethernet Transmitter Descriptor Pointer Register

Cold reset value: 0x0

Warm reset value: 0x0

| Field | Mask | Cold | Warm | Description |
|-----------------------|------------|------|------|----------------------|
| TXDTRA | 0xfffff800 | 0x0 | 0x0 | Tx desc base address |
| TX_DESCRIPTOR_P TR | 0x3f8 | 0x0 | 0x0 | Tx desc offset |

5.1.7. Register ETHRDP

Ethernet Receiver Descriptor Pointer Register

Cold reset value: 0x0

Warm reset value: 0x0

| Field | Mask | Cold | Warm | Description |
|-----------------------|------------|------|------|----------------------|
| RXDTRA | 0xfffff800 | 0x0 | 0x0 | Rx desc base address |
| RX_DESCRIPTOR_P TR | 0x3f8 | 0x0 | 0x0 | Rx desc offset |

6. Limitations

- Multicast groups are not yet supported.
- ECDL mode is not supported.