TERMA

TEMU
LEON2 Device Model Manual

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Table 1. Record of Changes

Rev	Date	Author	Note
1.4	2019-02-18	MH	Signal interface support.
1.3	2016-09-29	MH	Use correct autogen tables.
1.2	2016-05-12	MH	Auto gen tables.
1.1	2015-09-17	MH	Describe cache support.
1.0	2015-03-01	MH	Initial version.

1. Introduction

The LEON2 model class implements a model of the LEON2 on chip devices (i.e. memory controller, interrupt controller, UARTs and timers). The model must be combined with a LEON2 CPU to be really useful.

2. Configuration

2.1. Interrupt Delivery

Set the irqControl property to point out the processor's irq interface. The model will deliver normal SPARC interrupts (1 up to 15). The LEON2 also exports the IrqCtrlIface as IrqIface. IrqClientIface should be wired from the CPU the LEON2 model is connected to.

The IrqIface enables the use of external interrupts using the raise and lower functions. The LEON2 has 8 external IRQs mapped according to the following table (the mappings cannot be customised at present):

Table 2. External to Internal IRQ Mapping

External	Internal (Sparc IRL)
0	4
1	5
2	6
3	7
4	10
5	12
6	13
7	15

The rules for IRQ raising is controlled by the GPIO IRQ config registers (it is also possible to raise IRQs by setting and lowering GPIO pins).

2.2. UART Connections

The UARTs are connected to the destination using the uarta and uartb properties. For the remote end points, these should be connected to UartAIface and UartBIface.

2.3. Infinite UART Speed

The UARTs can run either at infinite speed, or at simulated real-time speed. This can be configured using the infiniteUartSpeed property. Set this property to non-zero to enable infinite UART speed.

Note that this controls the speed of both UARTs.

When infinite speed is enabled, bytes are emitted to the destination serial device as soon as they have been written by the OBSW.

2.4. GPIO

The GPIO support in the LEON2 model supports interrupt generation using the GPIO interface instead of the IRQ controller interface. Model implements both the GpioClientIface and a property with a GpioBusIface reference (called gpioBus). The GPIO bus connection is not mandatory to set. If it is set, writes to the GPIO data register's out bits will be forwarded over the GPIO port. Note that the LEON2 only have 16 GPIO pins.

Both the legacy multipin GpioBusIface and the new single pin SignalIface are supported. The model will prioritise the legacy interface for backwards compatibility. If you wish to use the SignalIface interface you should not set the gpioBus property.

2.5. Caches

The LEON2 SoC can act as a cache controller. That means that a cache model can notify the SoC about when it starts an evict/flush operation. The controller will also notify any connected caches about enabling, disabling and freezing events happening.

The cache parameters in the cache control register and the product configuration register are set automatically when connecting the dCache and iCache interface references to conforming objects.

When connecting the cache references, make sure the caches are configured before they are connected.

The caches that these interface references are connected to should normally be compliant with the supported LEON2 cache parameters. That is, there is a limitation on the sizes, lines and ways.

While the model does a best effort in trying to report errors when a miss-configured cache model is supplied, take care to ensure that the model is correctly configured.

3. Attributes

3.1. Properties

Name	Type	Description
ahbfailaddr	uint32_t	Fail address register
ahbstat	uint32_t	Fail status register
behaviour	uint8_t	Set to 1 for COLE mode
cachectrl	uint32_t	Cache control register
cpu	iref / CpuIface	CPU to control with powerdown
dCache	iref / <unknown>	
gpioBus	iref / <unknown>	
gpioIrqLevel	uint32_t	
gpioIrqMask	uint32_t	
gpioIrqPolarity	uint32_t	
gpiodir	uint32_t	I/O port direction register
gpioinout	uint32_t	I/O port data register
gpioirqcfg	uint32_t	I/O port interrupt register 1
gpioirqcfg2	uint32_t	I/O port interrupt register 2
iCache	iref / <unknown>	
infiniteUartSpeed	uint32_t	
irqControl	iref / IrqCtrlIface	Next level IRQ controller object (e.g. CPU)
irqclear	uint32_t	Interrupt clear register
irqforce	uint32_t	Interrupt force register
irqmask	uint32_t	Interrupt mask and priority register
irqpend	uint32_t	Interrupt pending register
leoncfg	uint32_t	Product configuration register
memcfg1	uint32_t	Memory configration register 1
memcfg2	uint32_t	Memory configuration register 2
memcfg3	uint32_t	Memory configuration register 3
memcfg4	uint32_t	Memory configuration 4 (COLE)

Name	Type	Description
memcfg5	uint32_t	Memory configuration 5 (COLE)
mr	uint32_t	Map register (COLE)
object.timeSource	object	Time source object (a cpu or machine object)
outSignals	[8 x iref / SignalIface]	
powerdown	uint32_t	Idle register
presccntr	uint32_t	Prescaler counter register
prescrld	uint32_t	Prescaler reload register
timer1cntr	uint32_t	Timer 1 counter register
timer1ctrl	uint32_t	Timer 1 control register
timer1rld	uint32_t	Timer 1 reload register
timer2cntr	uint32_t	Timer 2 counter register
timer2ctrl	uint32_t	Timer 2 control register
timer2rld	uint32_t	Timer 2 reload register
uart1DatTxHold	uint32_t	UART1 data TX hold register
uart1DatTxShift	uint32_t	UART 1 data TX shift
uart1ctrl	uint32_t	UART 1 control register
uart1datrx	uint32_t	UART 1 RX data register
uart1scal	uint32_t	UART 1 scaler register
uart1stat	uint32_t	UART 1 status register
uart2DatTxHold	uint32_t	
uart2DatTxShift	uint32_t	
uart2ctrl	uint32_t	UART 2 control register
uart2datrx	uint32_t	UART 1 RX data register
uart2scal	uint32_t	UART 2 scaler register
uart2stat	uint32_t	UART 2 status register
uarta	iref / <unknown>	
uartb	iref / <unknown>	
watchdog	uint32_t	Watchdog register
writeprot1	uint32_t	Write protection register 1
writeprot2	uint32_t	Write protection register 2
writeprotstart1	uint32_t	Write protection start address 1

Name	Type	Description
writeprotstart2	uint32_t	Write protection start address 2
writeprotstop1	uint32_t	Write protection end address 1
writeprotstop2	uint32_t	Write protection end address 2

3.2. Interfaces

Name	Type	Description
DCacheCtrlIface	CacheCtrlIface	D-cache to control
DeviceIface	DeviceIface	
GpioClientIface	GpioClientIface	
ICacheCtrlIface	CacheCtrlIface	I-cache to control
IrqClientIface	IrqClientIface	IRQ acknowledgement (from CPU)
IrqIface	IrqCtrlIface	IRQ controller, post your IRQs here.
MemAccessIface	MemAccessIface	
ResetIface	ResetIface	
SignalIface	SignalIface	Incomming signals
UartAIface	SerialIface	UART A
UartBIface	SerialIface	UART B

3.3. Ports

Prop	Iface	Description
irqControl	IrqClientIface	Interrupt
uarta	UartAIface	uart a
uartb	UartBIface	uart b

4. Registers

Register support is currently experimental!

4.1. Register Bank registers

4.1.1. Register memcfg1

Memory configration register 1

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
pbrdy	0x40000000	0x0	0x0	PROM area bus-ready enable
abrdy	0x20000000	0x0	0x0	Asynchronous bus ready
iowdh	0x18000000	0x0	0x0	I/O bus width
iobrdy	0x4000000	0x0	0x0	I/O area bus ready enable
bexc	0x2000000	0x0	0x0	Bus error enable for RAM PROM and I/O access
iows	0xf00000	0x0	0x0	I/O waitstates
ioen	0x80000	0x0	0x0	I/O area enable
prwen	0x800	0x0	0x0	PROM write enable
prwdh	0x300	0x0	0x0	PROM width
prwws	0xf0	0x0	0x0	PROM write waitstates
prrws	0xf	0x0	0x0	PROM read waitstates

4.1.2. Register memcfg2

Memory configuration register 2

Cold reset value: 0x7

Warm reset value: 0x7

Field	Mask	Cold	Warm	Description
sdrref	0x80000000	0x0	0x0	SDRAM refresh
trp	0x40000000	0x1	0x1	SDRAM t_rp timing

Field	Mask	Cold	Warm	Description
trfc	0x38000000	0x7	0x7	SDRAM t_rfp timing
sdrcas	0x4000000	0x1	0x1	SDRAM CAS delay
sdrbs	0x3800000	0x0	0x0	SDRAM bank size
sdrcls	0x600000	0x2	0x2	SDRAM column size
sdrcmd	0x180000	0x0	0x0	SDRAM command
se	0x4000	0x0	0x0	SDRAM enable
si	0x2000	0x0	0x0	SDRAM disable
rambs	0x1e00	0x0	0x0	SRAM bank size
rambrdy	0x80	0x2	0x2	SRAM area bus ready enable
ramrmw	0x40	0x2	0x2	SRAM read-modify-write
ramwdh	0x30	0x2	0x2	SRAM bus width
ramwws	0xc	0x0	0x0	SRAM write waitstates
ramrws	0x3	0x0	0x0	SRAM read waitstates

4.1.3. Register memcfg3

Memory configuration register 3

Cold reset value: 0x3

Warm reset value: 0x3

Field	Mask	Cold	Warm	Description
rfc	0xc0000000	0x3	0x3	Register file checkbits
me	0x8000000	0x1	0x1	Memory EDAC
srcrv	0x7fff000	0x0	0x0	SDRAM refresh counter reload value
wb	0x800	0x0	0x0	EDAC diagnostic write bypass

Field	Mask	Cold	Warm	Description
rb	0x400	0x0	0x0	EDAC diagnostic read
re	0x200	0x0	0x0	RAM EDAC enable
pe	0x100	0x0	0x0	PROM EDAC enable
tcb	0xff	0x0	0x0	Test checkbits

4.1.4. Register ahbfailaddr

Fail address register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.5. Register ahbstat

Fail status register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
eed	0x200	0x0	0x0	EDAC-correctable error detected
hed	0x100	0x0	0x0	Hardware error detected
het	0x80	0x0	0x0	Hardware error type
hem	0x78	0x0	0x0	Hardware error module
hes	0x7	0x0	0x0	Hardware error size

4.1.6. Register cachectrl

Cache control register

Cold reset value: 0x3

Warm reset value: 0x3

Field	Mask	Cold	Warm	Description
drepl	0xc0000000	0x3	0x3	Data cache replacement policy
irepl	0x30000000	0x3	0x3	Instruction cache replacement policy
isets	0xc000000	0x3	0x3	Instruction cache associativity
dsets	0x1000000	0x1	0x1	Data cache associativity
ds	0x800000	0x0	0x0	Data cache snoop enable
fd	0x400000	0x0	0x0	Flush data cache
fi	0x200000	0x0	0x0	Flush instruction cache
cpc	0x180000	0x2	0x2	Cache parity bits
cptb	0x60000	0x3	0x3	Cache parity test bits
ib	0x10000	0x3	0x3	Instruction burst fetch
ip	0x8000	0x3	0x3	Instruction cache flush pending
dp	0x4000	0x0	0x0	Data cache flush pending
ite	0x3000	0x0	0x0	Instruction cache tag error counter
ide	0xc00	0x0	0x0	Instruction cache data error counter
dte	0x300	0x0	0x0	Data cache tag error counter
dde	0xc0	0x0	0x0	Data cache data error counter
df	0x20	0x0	0x0	Data cache freeze on interrupt

Field	Mask	Cold	Warm	Description
if	0x10	0x0	0x0	Instruction cache freeze on interrupt
dcs	0xc	0x0	0x0	Data cache state
ics	0x3	0x0	0x0	Instruction cache state

4.1.7. Register powerdown

Idle register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.8. Register writeprot1

Write protection register 1

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
en	0x80000000	0x0	0x0	Enable
bp	0x40000000	0x0	0x0	Block protect
tag	0x1fff8000	0x0	0x0	Address tag
mask	0x3fff	0x0	0x0	Address mask

4.1.9. Register writeprot2

Write protection register 2

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
en	0x80000000	0x0	0x0	Enable
bp	0x40000000	0x0	0x0	Block protect

Field	Mask	Cold	Warm	Description
tag	0x1fff8000	0x0	0x0	Address tag
mask	0x3fff	0x0	0x0	Address mask

4.1.10. Register writeprotstart1

Write protection start address 1

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
start	0x3ffffffc	0x0	0x0	Start address
bp	0x2	0x0	0x0	Block protect

4.1.11. Register writeprotstart2

Write protection start address 2

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
start	0x3ffffffc	0x0	0x0	Start address
bp	0x2	0x0	0x0	Block protect

4.1.12. Register writeprotstop1

Write protection end address 1

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
end	0x3ffffffc	0x0	0x0	End address
us	0x2	0x0	0x0	User mode
su	0x1	0x0	0x0	Supervisor mode

4.1.13. Register writeprotstop2

Write protection end address 2

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
end	0x3ffffffc	0x0	0x0	End address
us	0x2	0x0	0x0	User mode
su	0x1	0x0	0x0	Supervisor mode

4.1.14. Register leoncfg

Product configuration register

Cold reset value: 0x7

Warm reset value: 0x7

Field	Mask	Cold	Warm	Description
mmu	0x80000000	0x0	0x0	Memory management unit
dsu	0x40000000	0x1	0x1	Debug support unit
sdrctrl	0x20000000	0x1	0x1	SDRAM controller
wtpnb	0x1c000000	0x4	0x4	IU watchpoints
imac	0x2000000	0x0	0x0	UMAC/SMAC instructions
nwin	0x1f00000	0x7	0x7	IU register file windows
icsz	0xe0000	0x3	0x3	Instruction cache set size
ilsz	0x18000	0x3	0x3	Instruction cache line size
dcsz	0x7000	0x3	0x3	Data cache set size
dlsz	0xc00	0x2	0x2	Data cache line size
divinst	0x200	0x1	0x1	UDIV/SDIV instructions
mulinst	0x100	0x1	0x1	UMUL/SMUL instructions
wdog	0x80	0x1	0x1	Watchdog

Field	Mask	Cold	Warm	Description
memstat	0x40	0x1	0x1	Memory status and address failing register
fpu	0x30	0x1	0x1	FPU type
pci	0xc	0x1	0x1	PCI core type
wprt	0x3	0x1	0x1	Write protections

4.1.15. Register timer1cntr

Timer 1 counter register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.16. Register timer1rld

Timer 1 reload register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.17. Register timer1ctrl

Timer 1 control register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
ld	0x4	0x0	0x0	Load counter
rl	0x2	0x0	0x0	Reload counter
en	0x1	0x0	0x0	Enable counter

4.1.18. Register watchdog

Watchdog register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.19. Register timer2cntr

Timer 2 counter register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.20. Register timer2rld

Timer 2 reload register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.21. Register timer2ctrl

Timer 2 control register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
ld	0x4	0x0	0x0	Load counter
rl	0x2	0x0	0x0	Reload counter
en	0x1	0x0	0x0	Enable counter

4.1.22. Register presccntr

Prescaler counter register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
cnt	0x3ff	0x0	0x0	Prescaler counter value

4.1.23. Register prescrld

Prescaler reload register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
rv	0x3ff	0x0	0x0	Prescaler reload value

4.1.24. Register uart1datrx

UART 1 RX data register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
rtd	0xff	0x0	0x0	Received/transmit data

4.1.25. Register uart1stat

UART 1 status register

Cold reset value: 0x1

Warm reset value: 0x1

Field	Mask	Cold	Warm	Description
fe	0x40	0x0	0x0	Framing error
pe	0x20	0x0	0x0	Parity error

Field	Mask	Cold	Warm	Description
ov	0x10	0x0	0x0	Overrun
br	0x8	0x0	0x0	Break received
th	0x4	0x1	0x1	Transmitter hold register empty
ts	0x2	0x1	0x1	Transmitter shift register empty
dr	0x1	0x0	0x0	Data ready

4.1.26. Register uart1ctrl

UART 1 control register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
ec	0x100	0x0	0x0	External clock
lb	0x80	0x0	0x0	Loop back
fl	0x40	0x0	0x0	Flow control
pe	0x20	0x0	0x0	Parity enable
ps	0x10	0x0	0x0	Parity select
ti	0x8	0x0	0x0	Transmitter interrupt enable
ri	0x4	0x0	0x0	Receiver interrupt enable
te	0x2	0x0	0x0	Transmitter enable
re	0x1	0x0	0x0	Receiver enable

4.1.27. Register uart1scal

UART 1 scaler register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.28. Register uart2datrx

UART 1 RX data register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
rtd	0xff	0x0	0x0	Received/transmit data

4.1.29. Register uart2stat

UART 2 status register

Cold reset value: 0x1

Warm reset value: 0x1

Field	Mask	Cold	Warm	Description
fe	0x40	0x0	0x0	Framing error
pe	0x20	0x0	0x0	Parity error
ov	0x10	0x0	0x0	Overrun
br	0x8	0x0	0x0	Break received
th	0x4	0x1	0x1	Transmitter hold register empty
ts	0x2	0x1	0x1	Transmitter shift register empty
dr	0x1	0x0	0x0	Data ready

4.1.30. Register uart2ctrl

UART 2 control register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
ec	0x100	0x0	0x0	External clock
lb	0x80	0x0	0x0	Loop back
fl	0x40	0x0	0x0	Flow control

Field	Mask	Cold	Warm	Description
pe	0x20	0x0	0x0	Parity enable
ps	0x10	0x0	0x0	Parity select
ti	0x8	0x0	0x0	Transmitter interrupt enable
ri	0x4	0x0	0x0	Receiver interrupt enable
te	0x2	0x0	0x0	Transmitter enable
re	0x1	0x0	0x0	Receiver enable

4.1.31. Register uart2scal

UART 2 scaler register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.32. Register irqmask

Interrupt mask and priority register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
ilevel_io7	0x80000000	0x0	0x0	Interrupt level
ilevel_pci	0x40000000	0x0	0x0	Interrupt level
ilevel_io6	0x20000000	0x0	0x0	Interrupt level
ilevel_io5	0x10000000	0x0	0x0	Interrupt level
ilevel_dsu	0x8000000	0x0	0x0	Interrupt level
ilevel_io4	0x4000000	0x0	0x0	Interrupt level
ilevel_timer2	0x2000000	0x0	0x0	Interrupt level
ilevel_timer1	0x1000000	0x0	0x0	Interrupt level
ilevel_io3	0x800000	0x0	0x0	Interrupt level

Field	Mask	Cold	Warm	Description
ilevel_io2	0x400000	0x0	0x0	Interrupt level
ilevel_io1	0x200000	0x0	0x0	Interrupt level
ilevel_io0	0x100000	0x0	0x0	Interrupt level
ilevel_uart1	0x80000	0x0	0x0	Interrupt level
ilevel_uart2	0x40000	0x0	0x0	Interrupt level
ilevel_amba	0x20000	0x0	0x0	Interrupt level
imask_io7	0x80000000	0x0	0x0	Interrupt mask
imask_pci	0x40000000	0x0	0x0	Interrupt mask
imask_io6	0x20000000	0x0	0x0	Interrupt mask
imask_io5	0x10000000	0x0	0x0	Interrupt mask
imask_dsu	0x8000000	0x0	0x0	Interrupt mask
imask_io4	0x4000000	0x0	0x0	Interrupt mask
imask_timer2	0x2000000	0x0	0x0	Interrupt mask
imask_timer1	0x1000000	0x0	0x0	Interrupt mask
imask_io3	0x800000	0x0	0x0	Interrupt mask
imask_io2	0x400000	0x0	0x0	Interrupt mask
imask_io1	0x200000	0x0	0x0	Interrupt mask
imask_io0	0x100000	0x0	0x0	Interrupt mask
imask_uart1	0x80000	0x0	0x0	Interrupt mask
imask_uart2	0x40000	0x0	0x0	Interrupt mask
imask_amba	0x20000	0x0	0x0	Interrupt mask

4.1.33. Register irqpend

Interrupt pending register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.34. Register irqforce

Interrupt force register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.35. Register irqclear

Interrupt clear register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.36. Register gpioinout

I/O port data register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.37. Register gpiodir

I/O port direction register

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.38. Register gpioirqcfg

I/O port interrupt register 1

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

4.1.39. Register gpioirqcfg2

I/O port interrupt register 2

Cold reset value: 0x0

Warm reset value: 0x0

Field	Mask	Cold	Warm	Description
-	-	-	-	-

5. Limitations

The Leon2 Device model simulates the AT697F chip. There are some deviations to the AT697E chip (e.g. the size of the counters). If you need the AT697E behaviour, please contact us for more info.

The following deviations from real hardware are known to exist, if you need the correct behaviour (or simulation of it, contact us for more info):

- No support for Ethernet at present
- No support for PCI at present
- The UARTs do not support external clocks.
- The UARTs do not support parity, framing errors and break signals.
- GPIO pin configurations are ignored for UARTs, the UARTs are assumed to be on separate dedicated I/O pins. However, a warning will be issued if the UART pins do not have the correct GPIO configuration.
- GPIO databus control is not supported (i.e. meddat and lowdat fields).
- Write protection registers have no effect
- Timer values are lazily computed on reads, the content in the case a timer is disabled is estimated on disabling time. This is in principle correct. However, the prescaler counter write has no effect, only the reload value has an effect when written. This may cause an offset of 1024 cycles when re-enabling a timer.
- In general the MEMCFG registers are ignored